A 74.8-88.8 GHz Wideband CMOS LNA Achieving +4.73 dBm OP1dB and 6.39 dB Minimum NF

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***Abstract*— This paper presents a 74.8-88.8 GHz low-noise amplifier (LNA) in a 55-nm CMOS technology. The LNA employs one common-gate (CG) stage, one common-source (CS) stage, and two cascode stages. A hybrid broadband interstage network (HBIN) is developed to extend the amplifier bandwidth. An inductor-feedback common-gate-shorting (IFCGS) technique is proposed to improve the gain and output 1dB compression point (OP1dB). An out-of-phase-dual-coupling (OPDC) transformer structure is also developed to achieve g_m-boost and reduce the noise of the CG stage. Benefiting from the proposed techniques, the LNA achieves a measured -3dB bandwidth of 14 GHz, a 17.1 dB peak gain, a minimum noise figure of 6.39 dB, and 4.73 dBm OP1dB at 80 GHz while consuming 72.4 mW of power.**

***Keywords*— Low-noise amplifier (LNA), E-band, linearity, g_m-boosted, inductor feedback common-gate shorting (IFCGS), millimeter wave (mm wave), wideband.**

I. Introduction

With the demand of high-resolution radars and high-data-rate wireless communication systems and the rapid scaling of CMOS technology, millimeter-wave (mm-wave) CMOS circuits have received tremendous attention. Recently, the E-band spectrum (71-76 GHz and 81-86 GHz) has been actively investigated for high bandwidth multi-gigabit-per-second wireless communication and ultra-high capacity point-to-point back-haul link applications [1]. To realize the full potential of E-band wireless systems, a wideband receiver (RX) is indispensable. The low noise amplifier (LNA), as the first active block of the receiver front end, demands a wide bandwidth with high gain and low noise figure (NF) to improve the receiver sensitivity. In addition, the transmitter leakage and isolation between antennas require the LNA to have high linearity, i.e., the input/output-refereed 1dB compression points IP1dB/OP1dB [2].

Several techniques have been developed in designing wideband mm-wave CMOS LNAs. In [3], a distributed LNA achieves a GBW product of 1.5 THz but suffers from high power consumption. A wideband LNA based on cascode configuration with resistive feedback is developed in [4] operating at 1.6-28 GHz. However, the noise and gain reduction caused by the resistive load worsens at mm-wave frequencies. In [5], a wideband LNA employing transformer-based 4th-order interstage matching networks is developed realizing a 29.6 dB gain and a 28.3 GHz -3dB bandwidth. However, the high gain is achieved at the cost of poor linearity. A wideband LNA over 60-90 GHz with high linearity is reported in [6], where a double neutralization technique is proposed. However, the LNA only achieves a 12.7 dB peak gain and has a poor noise figure. It remains challenging to simultaneously achieve a high gain and high linearity while attaining a low NF and wide bandwidth in designing mm-wave CMOS LNAs.

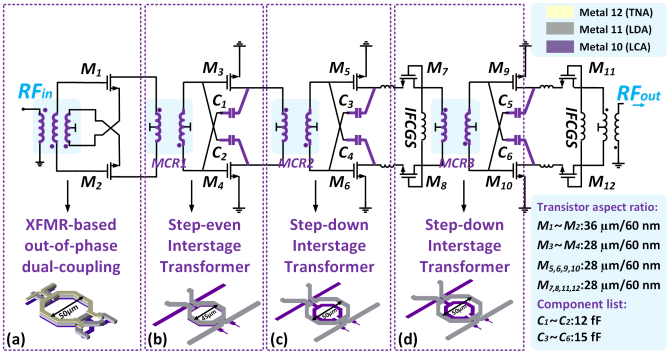


Fig. 1. Schematic of the proposed four-stage mm-wave LNA and the 3-D views of (a) the OPDC balun and (b)-(d) interstage transformers.

In this paper, a wideband 74.8-88.8 GHz LNA is designed in a 55-nm CMOS technology. The LNA employs one common-gate (CG) stage, one common-source (CS) stage, and two cascode stages. In order to achieve a wideband operation without adding additional power consumption, a hybrid broadband interstage network (HBIN) design approach is developed. To enhance the gain and the OP1dB of the cascode stage, an inductor-feedback common-gate-shorting (IFCGS) technique is proposed. Further, an out-of-phase-dual-coupling (OPDC) structure is exploited to compensate for the noise and boost the gain of the common-gate stage. The LNA achieves a measured peak gain of 17.1 dB, a 14 GHz -3dB bandwidth, a minimum NF of 6.39 dB, and +4.73 dBm OP1dB at 80 GHz.

II. Circuit Design

Fig. 1 shows the schematic of the proposed LNA. It adopts a differential structure and includes one CG stage, one CS stage, and two cascode stages. The first interstage magnetically-coupled-resonant (MCR) network is a step-even

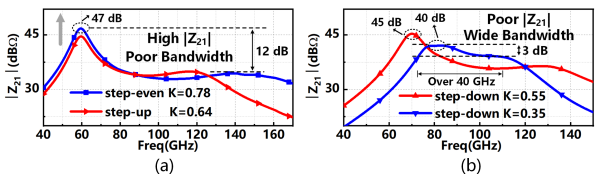


Fig. 2. The simulated $|Z_{21}|$ of (a) step-even/up transformer and (b) step-down transformer.

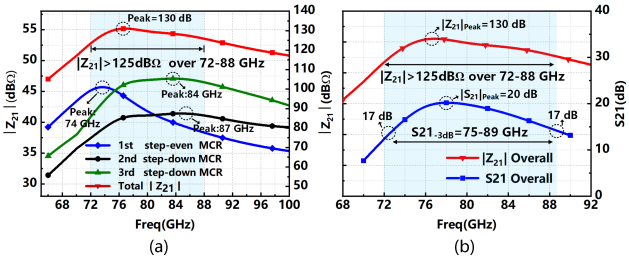


Fig. 3. (a) The simulated $|Z_{21}|$ of the first, the second, and the third-stage interstage coupling networks and the overall transimpedance response of the LNA, and (b) comparison of overall S_{21} and Z_{21}.

transformer, and the second and third transformers are implemented using a step-down structure, forming the HBIN network. In the cascode structure, the gate inductor employing the IFCGS technique eliminates the parasitic interstage capacitance. Further, in the CG stage, g_m-boost is realized by the proposed OPDC technique. All passive devices are designed using ADS Momentum, and their 3-D views and parameters are shown in Figs. 1(a)-(d), respectively.

A. HBIN for Wide Bandwidth

Using multiple step-down transformers and keeping them in low-k states have been previously developed to design wideband mm-wave LNAs. However, the wide bandwidth is achieved at the expense of a large die area and severe passive network loss. Different from the step-down transformer-only approach in [5], this work proposes a new hybrid broadband interstage network design approach, which takes advantage of both the step-even and step-down transformers to achieve wide bandwidth.

To obtain an optimal transformer design choice, the effect of the coupling coefficient k on the step-even, step-up, and step-down transformers' transimpedance responses is studied, and the results are shown in Figs. 2(a)-(b). As can be seen from the figure, the step-even and step-up transformers have similar transimpedance responses. The highest transimpedance gain occurs at the low-frequency pole ω_L, but there is a significant difference in transimpedance gain at ω_L and the high-frequency pole ω_H. It can also be noticed that with a decrease of the k value, the ω_L of the step-up transformer remains almost unchanged, but ω_H is much reduced. For the step-down transformer, the frequency separation between ω_H and ω_L is smaller and thus the transimpedance response is flatter. However, the transimpedance gain is decreased.

Based on the above observations, a step-even transformer with $k = 0.78$, a step-down transformer with $k = 0.35$, and a step-down transformer with $k = 0.31$ are adopted in the first, second, and the third interstage MCR networks,

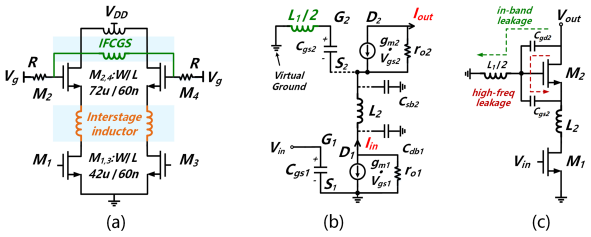


Fig. 4. (a) The schematic of the proposed cascode stage , (b) the half-side equivalent circuit of the proposed structure with IFCGS technique, and (c) analysis of the leakage on in-band and high frequency.

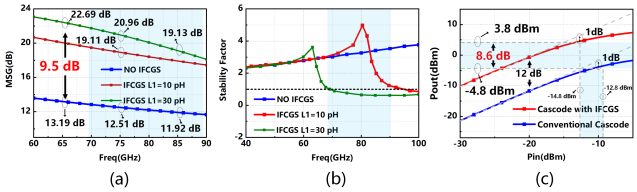


Fig. 5. The simulated (a) MSG, (b) stability factor of IFCGS with different inductor values, (c) comparison of IP1dB and OP1dB between the proposed and the conventional cascode structures.

respectively. The MCR1 works at low frequency and provides a high transimpedance gain, while MCR2 and MCR3 work at high frequencies and compensate for the transimpedance attenuation of MCR1, providing an overall flat transimpedance response. The overall $|Z_{21}|$ is shown in Fig. 3(a), which achieves a flat and larger than 125 dBΩ transimpedance gain over the 72-88 GHz frequency range. As shown in Fig. 3(b), the $|Z_{21}|$ correlated well with the simulated S_{21} -3dB bandwidth, demonstrating the effectiveness of the hybrid interstage network design approach.

B. IFCGS Technique for High Gain and High OP1dB

The cascode structure is adopted in the last two stages because of its excellent isolation characteristics at mm-wave frequencies. The cascode structure, however, suffers from gain reduction caused by stable resistance and parasitic interstage capacitance. Also, as the last gain stage, the linearity of the cascode stage is critical. It is highly desirable to attain a high gain while maintaining a high linearity for the cascode gain stage.

The linearity of the cascode stage can be improved by increasing the V_{ds} of the common-source transistor and reducing its load impedance [7]. In terms of gain, the gain reduction problem caused by stable resistance and parasitic interstage capacitance was previously addressed by a common-gate-short (CGS) technique [8]. However, the C_{sb2} and C_{gs2} capacitance still introduce leakage current. To address this issue, an inductor-feedback common-gate-shorting (IFCGS) technique is proposed. Fig. 4(b) shows the half-side equivalent circuit of the IFCGS technique. The L_1 inductor is introduced to absorb the C_{sb2} and C_{gs2} effect. The current gain of the common-gate stage with IFCGS can be derived as:

$$I_{out} \approx I_{in} \cdot \frac{g_m}{\left\{g_m + s\left[C_{sb2}\left(1-\omega^2 \frac{L_1}{2} C_{gs2}\right) + C_{gs2}\right]\right\}} \quad (1)$$

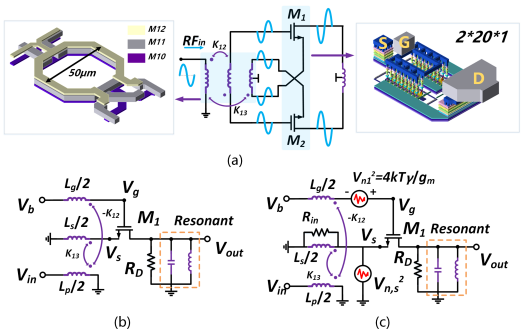


Fig. 6. (a) Schematic of the g_m-boosted OPDC circuit, (b) the half-side equivalent circuit of OPDC, and (c) the noise model of OPDC circuit.

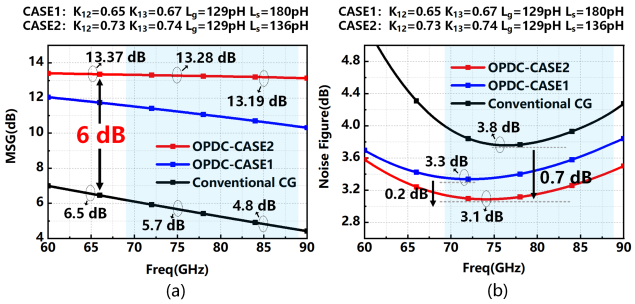


Fig. 7. (a) MSG and (b) NF with the proposed OPDC under different coupling coefficients and inductance values.

From the equation, by choosing a proper L_1 inductance value, the influence of C_{sb2} and C_{gs2} on the current gain can be avoided.

For stability, the added inductor at the gate of M_2 along with the C_{gd2} provides a low-impedance path for the signal at the output to ground, preventing it from leaking back to the input, as shown in Fig. 4(c). However, when the frequency goes higher than the resonant frequency, the gate of M_2 becomes a high impedance path,increasing the signal leaking back to the input.

Figs. 5(a)-(b) shows the simulated maximum stable gain (MSG) and stability factor of the cascode topology for the cases of without the IFCGS technology and with the IFCGS technology composed of various inductances. To compromise gain and stability, the final value of L_1 is 10 pH. And with the IFCGS technique, the OP1dB is improved by 8.6 dB in Fig. 5(c).

C. Coupling-Concerned OPDC for Low Noise and High Gain

In designing the LNA, the common-gate structure is used as the first gain stage because of its excellent linearity and matching characteristics. However, its noise is limited by the $1/g_m$ input matching requirement. To boost the g_m and improve the noise performance, a coupling-concerned out-of-phase-dual-coupling (OPDC) technique and a customized transistor are developed for the CG stage.

Different from the g_m-boosted CG design based on the coupling transformer in [9], the OPDC transformer structure is developed for the proposed LNA. Fig. 6(a) shows the 3-D diagram of the proposed OPDC input balun implemented with the top aluminum layer, the top copper layer and the sub-top copper layer. Fig. 6(b) shows its half-equivalent circuit. In the OPDC transformer, the transformer ratios are respectively $1:n_sk_{13}$ between V_{in} and V_s and $1:-n_gk_{12}$ between V_{in} and V_g, where $n_s=\sqrt{L_s/L_p}$, $n_g=\sqrt{L_g/L_p}$, and k_{13} and k_{12} denote the coupling coefficients between L_p and L_s and between L_p and L_g, respectively. The k_{23} is neglected because of the weak coupling between L_g and L_s. Consequently, $V_s=n_sk_{13}V_{in}$, $V_g=-n_gk_{12}V_{in}$, and with $g_m\Delta V_{gs}=-V_{out}/R_D$ the voltage gain can be obtained as:

$$\frac{V_{out}}{V_{in}}=\left(n_gK_{12}+n_sK_{13}\right)g_mR_D \tag{2}$$

Fig. 6(c) shows the noise model of the CG circuit with the proposed OPDC technique. The source noise voltage of the M_1 transistor can be expressed as $V_{n,s}=-V_{n,out}R_{in}/R_D$, where R_{in} is the equivalent resistance of R_s after impedance transformation and $R_{in}=\left(n_sK_{13}\right)^2R_s/2$. The $V_{n,s}$ is coupled to the gate of the M_1 transistor by the transformer. Therefore, the gate noise voltage of M_1 is $V_{n,g}=\left(\frac{V_{n,\text{out}}R_{in}}{R_D}\right)\cdot\left(\frac{n_gK_{12}}{n_sK_{13}}\right)+V_{n1}$, ${V_{n1}}^2=4KT\gamma/g_m$. From Fig. 6(c), the output noise voltage of M_1 is then obtained as:

$$V_{n,out}|_{M_1}=-\frac{g_mR_DV_{n1}}{1+g_mR_{in}\left(1+\frac{n_gK_{12}}{n_sK_{13}}\right)} \tag{3}$$

Under the input impedance matched condition, $R_{in}=1/\left[g_m\left(1+\frac{n_gK_{12}}{n_sK_{13}}\right)\right]$ and $A_v=\frac{(n_gK_{12}+n_sK_{13})g_mR_D}{2}$, then

$$\begin{aligned}NF&=1+\frac{\overline{V_{n,out}^2}\Big|_{M1}+4kTR_D}{4kTR_s\left(A_v\right)^2}\\&=1+\frac{\gamma}{\left(n_gK_{12}+n_sK_{13}\right)}+\frac{4}{\left(n_gK_{12}+n_sK_{13}\right)g_mR_D}\end{aligned} \tag{4}$$

Compared with the conventional CG structure where $NF=1+\gamma+\frac{4}{g_mR_D}$, the NF caused by M_1 is reduced by a factor of $(n_gk_{12}+n_sk_{13})$ by the proposed OPDC technique. It should be noted that the coil self-inductance will also affect the actual transformer design, and thus adjusting the parameters n_gk_{12} and n_sk_{13} is required. Fig. 7 shows the simulated MSG and NF of the CG circuit versus the coupling coefficient and inductance value. In designing the LNA, the values of k_{12}, k_{13}, Lg, and Ls are chosen as 0.73, 0.74, 129 pH, and 136 pH, respectively, to achieve an overall optimized MSG and NF performances.

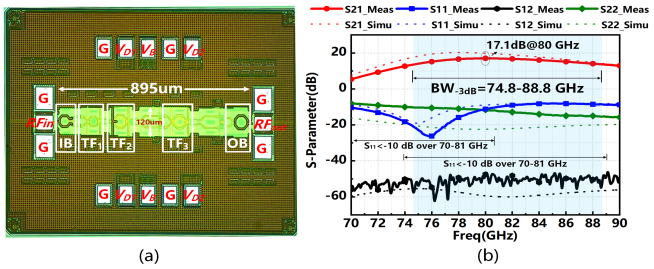
III. Measurement Results

Fig. 8(a) shows the die photo of the proposed wideband LNA fabricated in a 55-nm CMOS process. The core area is 895×120 μm^2 excluding the testing pads. The characterization is conducted on-wafer using a 100 μm GSG probe. The DC supply voltages AVDD1 (for the CS stage) and AVDD2 (for the cascode stage) are 1.2 and 2.0 V, respectively. The LNA consumes 72.4 mW of power, where the currents are 20 mA and 24.2 mA from the 1.2 V and 2 V supply, respectively.

Table 1. Performance Summary and Comparison with the State-of-the-art Wideband mm-wave LNAs.

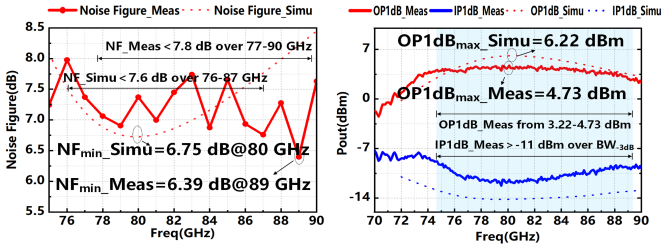
Reference	technique	Topology	Peak Gain (dB)	BW-3dB (GHz)	NFmin (dB)	IP1dB (dBm)	OP1dB (dBm)	Pdc (mW)	Area (mm^2)	FOM
[10] JSSC 2017	28nm CMOS	Differential 1-Stage CG + 4-Stage CS	29.6	28.3 (68.1-96.4)	6.4	-28.1	+1.5#	31.3	0.675	12.57
[11] TMTT 2020	22nm FDSOI CMOS	Single-ended 3-Stage CSCG	24	13 (70.5-83.5)	4.6	-26.8	-2.8#	16	0.35	14.28
[12] RFIC 2020	65nm CMOS	Differential 3-Stage CS	25	7.5 (53.5-61)	4.8	-22	+3.0#	47	0.26	8.86
[8] IMS2020	55nm CMOS	Differential 2-Stage CS + 1-Stage CSCG	15	7.6 (78.9-86.5)	5	-13.2	+1.8#	72.7	0.08	13.01
[13] MWCL2022	40nm CMOS	Differential 3-Stage CS	19	16.1 (76.5-92.6)	5.7	-19	0#	23.4	0.17	26.84
This Work	**55nm CMOS**	**Differential 1-Stage CG + 1-Stage CS + 2-Stage CSCG**	**17.1**	**14 (74.8-88.8)**	**6.39**	**-12.37**	**+4.73**	**72.4**	**0.107+**	**24.29**

Estimated values from papers + Area without including bondpads



(a) (b)

Fig. 8. (a) Die photo of the proposed wideband mm-wave LNA and (b) the measured S_{21}, S_{11}, S_{22}, S_{12}.



(a) (b)

Fig. 9. The measured (a) NF and (b) large signal gain and output power of the LNA from 74 to 90 GHz.

Fig. 8(b) shows the measured S-parameters. The LNA achieves a peak gain of 17.1 dB at 80 GHz and a 14 GHz -3dB bandwidth over 74.8-88.8 GHz. Fig. 9(a) shows the measured NF. The NF_{min} is 6.39 dB at 89 GHz, and the noise figures are less than 7.8 dB over 77 to 90 GHz. The measured OP1dB is shown in Fig. 9(b). The OP1dB is from +3.22 to +4.73 dBm over 74.8-88.8 GHz, and at 80 GHz, the OP1DB is +4.73 dBm. The measurement results correlate well with the simulation results. The performance of the LNA is summarized and compared with that of the state-of-the-art wideband mm-wave LNAs in Table 1. In the table, the LNA figure-of-merit (FOM) is calculated as:

$$FOM = \frac{\text{Gain[lin]} \cdot BW_{-3dB}[MHz] \cdot IP1dB[\text{lin}]}{P_{dc}[mW] \cdot (F[lin] - 1)} \quad (5)$$

IV. Conclusion

This paper proposes a 74.8-88.8 GHz LNA designed in a 55-nm CMOS technology. To enhance the bandwidth, a hybrid step-even and step-down interstage coupling network is developed. To achieve high gain with high linearity and a low NF, an inductor-feedback common-gate-shorting technique and an out-of-phase-dual-coupling input balun are developed. With the proposed techniques, the LNA achieves a measured -3dB bandwidth of 14 GHz, a 17.1 dB peak gain, a minimum NF of 6.39 dB, and a 4.73 dBm OP1dB at 80 GHz while consuming 72.4 mW power. The LNA demonstrates the best FOM compared with prior works.

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