A 26-44GHz 28nm CMOS FD-SOI Slow-Wave Tunable Hybrid Coupler for 5G Application

Gwennaël Diverrez#1, Eric Kerhervé#2, Magali De Matos#3, Andreia Cathelin$4
#IMS Laboratory, Bordeaux University, CNRS UMR 5218, Talence, France
$STMicroelectronics, Crolles, France
{[1]gwennael.diverrez, [2]eric.kerherve, [3]magali.dematos}@ims-bordeaux.fr, [4]andreia.cathelin@st.com

***Abstract*— This paper presents a 26-44GHz multi-band 90° twisted hybrid coupler exhibiting low insertion loss for 5G application. Using a tunable 3-bit slow-wave architecture, the hybrid coupler offers eight operating modes allowing it to select the desired center frequency and covers a bandwidth of more than 51% while minimizing its losses. The hybrid coupler achieves an insertion loss lower than 2.2dB with a minimum of 1.45dB at 26GHz and a phase shift between the two output paths of 95 ± 5°. The circuit is implemented in a CMOS 28nm FD-SOI process and occupies 0.00567 mm².**

***Keywords*— hybrid coupler, 90°, tunable, wideband, slow-wave, coupled lines, 5G, CMOS 28nm FD-SOI.**

I. Introduction

The versatility of hybrid quadrature (90°) couplers in microwave and millimeter wave architectures has made them a key component of RF architectures since their introduction. Today, the emergence of 5G offers new specifications for RF transceivers and especially for hybrid couplers. Indeed, they are based on beamforming antenna arrays which present significant impedance variations due to the coupling between antennas that strongly degrade the performances of power amplifiers (PA). Among the different VSWR protection techniques, the balanced architecture is the most used because hybrid couplers inherently protect the amplifier. In addition, broadband PA with linearity and efficiency up to deep power back-off (PBO) is of crucial interest for 5G. As a result, balanced [1], Doherty [2] and Load Modulated Balanced Amplifier (LMBA) [3] architectures using hybrid coupler-based structures are developed to meet 5G requirements (Fig. 1). In this context, hybrid couplers must exhibit low insertion losses to prevent degradation of the power amplifier's efficiency. Thus, compact hybrid couplers with low insertion losses and operating over wide frequency bands without affecting amplifier linearity are required for 5G.

Lange couplers and branch lines couplers [4] exhibit low insertion loss but at the expense of their compactness. In comparison, the transformer-based architecture [5] offers high compacity while exhibiting low insertion losses around 20 GHz. Nevertheless, this architecture presents higher losses when the frequency increases. The twisted architecture [6] provides better insertion losses for higher frequencies while being more compact. However, the bandwidth of the coupler is limited by the amplitude imbalance between its two output paths. In this context, the multi-band architecture [7] offers a high bandwidth thanks to a bank of capacitors. Indeed, the addition of a variable capacitive contribution modifies the center frequency of the coupler. However the internal resistance of the transistor switch strongly degrades the insertion losses of the coupler.

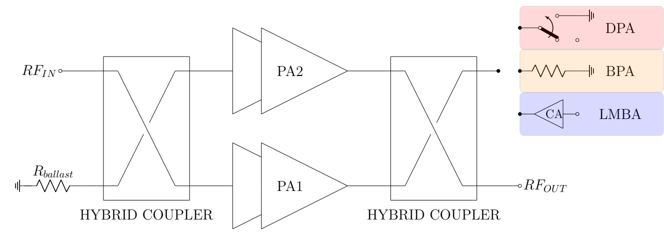


Fig. 1. Different types of quadrature coupler-based PAs (CA: control amplifier, DPA: Doherty PA, BPA : Balanced PA).

To address these challenges, this paper proposes an hybrid twisted coupler using a 3-bit tunable slow-wave structure. With this reconfiguration, the hybrid coupler exhibits a bandwidth of nearly 50% with low insertion losses. Unlike the architecture with capacitor bank, the proposed solution uses slow-wave lines to bring more or less capacitive contribution to the classical coupler structure. In section II, the design of the twisted hybrid coupler is detailed. Then, this paper describes the slow-wave theory applied to the twisted hybrid coupler architecture in section III. Section IV shows the measurements and a comparison with the state of the art.

II. Twisted Hybrid Coupler Design

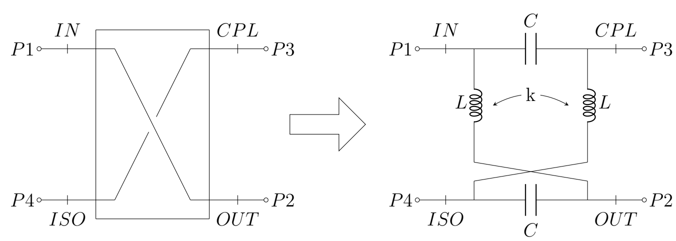


Fig. 2. Simplified schematic of the twisted hybrid coupler.

A. From specifications to L and C values

Starting from the specifications of a coupler (f_0, Z_0, k), the values of (L,C) of the electrical schematic (Fig. 2) are determined using equations (1) and (2) (for k $\geq$ 0.7) :

$$L = \frac{(2-k)Z_0}{\omega_0} \quad (1)$$

$$C = \frac{(2-k)}{2Z_0\omega_0} \quad (2)$$

B. *Twisted Hybrid Coupler Layout*

The twisted hybrid coupler is chosen for its wideband behavior, its low insertion losses and its compactness. It differs from other hybrid couplers by its design. Indeed, it is composed of coupled lines that are mainly inductive but still provide a capacitive contribution, and of a capacitive and moderately inductive twist (Fig. 3).

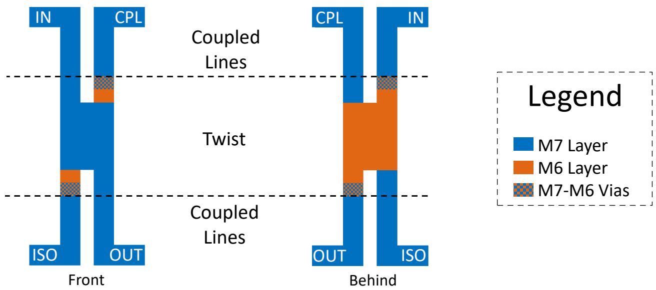


Fig. 3. Twisted hybrid coupler scheme.

C. *Coupler Sizing*

The width of the lines is set by the electromigration rules when the thickness of the metals is inherent to the technology. The spacing between the tracks is chosen to respect the minimum gap allowed by the DRC of the technology. Indeed, maximizing the coupling coefficient k allows to reduce the coupler size according to equations (1) and (2).

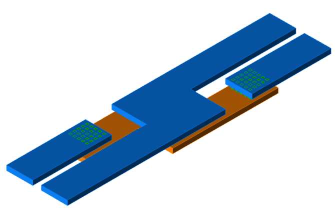


Fig. 4. Twist layout of the hybrid coupler.

D. *Inductives and capacitives contributions of the coupler*

A pre-dimensioning of the coupler is carried out by using the theoretical equations of the inductances and capacitances of the coupler elements. The self and mutual inductances [8] of rectangular metal bars (Fig. 5) are calculated with equations (3) and (4):

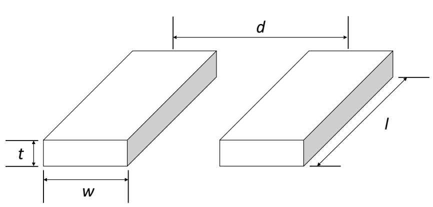


Fig. 5. Schematic of rectangular metal bars with their characteristic distances.

$$L_p = \frac{\mu_0 l}{2\pi}\left[ln\left[\frac{2l}{w+t}\right] + \frac{1}{2} + \frac{2}{9}\left(\frac{w+t}{l}\right)\right] \tag{3}$$

$$M = \frac{\mu_0 l}{2\pi}\left[ln\left[\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}}\right] - \sqrt{1+\frac{d^2}{l^2}} + \frac{d}{l}\right] \tag{4}$$

The parallel plate and fringe capacitances [9] between two bars (Fig. 6) are expressed by equations (5) and (6) :

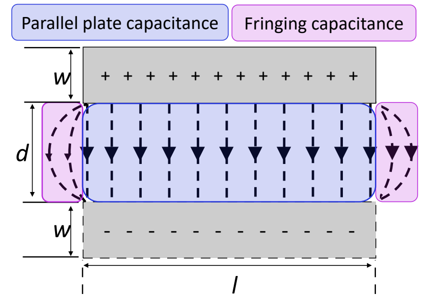


Fig. 6. Field lines for parallel plate and fringe capacitors.

$$C_{par} = \frac{\epsilon_0 \epsilon_r w t}{d} \tag{5}$$

$$C_{fring} = \frac{2\pi\epsilon_0\epsilon_r l}{ln\left(1 + \frac{2d}{t} + \sqrt{\frac{2d}{t}(\frac{2d}{t}+2)}\right)} \tag{6}$$

Finally, the inductive and capacitive contributions of the coupler are estimated by summing the equations together :

$$L = 2L_p - M \tag{7}$$

$$C = C_{par} + C_{fring} \tag{8}$$

However, these equations do not consider the coupling to the substrate of the coupler which leads to a slight deviation.

E. *Theoretical EM Model*

Fig. 7 shows the equivalent schematic of the proposed twisted hybrid coupler [9].

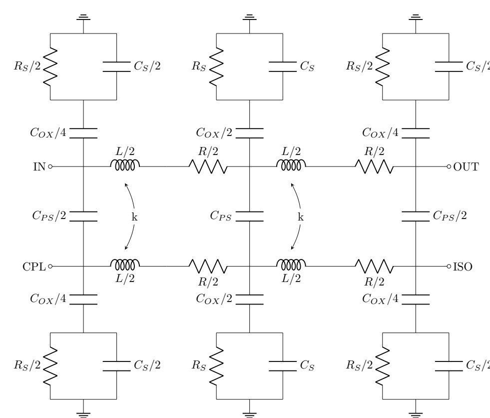


Fig. 7. Equivalent schematic of the hybrid coupler.

The hybrid coupler model considers the effect of the quality coefficient of the inductors (R_L) and the coupling to the substrate. The distributed values of the inductance L and the total capacitance C_{tot} taking into account the couplings to the substrate adjust the center frequency of the coupler f_0 :

$$f_0 = \frac{(2-k)}{2\pi\sqrt{2LC_{tot}}} \tag{9}$$

where $C_{tot} \simeq 2.C_{P_S}//(2.C_{OX} + 4.C_S)$.

III. Slow-Wave Frequency Tunability

A. *Slow-Wave Line Principle*

The slow-wave phenomenon is generally used to improve the performance of passive circuits. The objective is to decrease the phase velocity v_{ϕ} of the wave in order to reduce the guided wavelength λ_g (equation 10) and thus offer the possibility of miniaturizing the lines.

$$v_{\varphi} = \frac{c_0}{\sqrt{\epsilon_{eff}}} = \lambda_g . f = \frac{1}{\sqrt{C_{lin} . L_{lin}}} \qquad (10)$$

The slow-wave coplanar waveguide grounded (Fig. 8) is a way to achieve the miniaturization effect by introducing periodic variations along the transmission line. In this case, metal strips are placed orthogonally under the CPW strips, resulting in a distributed capacitive effect. The linear capacitance is thus increased, which leads to a decrease in propagation speed.

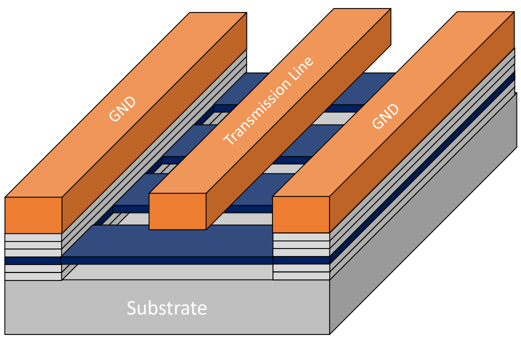


Fig. 8. Slow-wave coplanar waveguide grounded S-CPWG.

B. *Application to a tunable twisted hybrid coupler*

This principle is adopted (Fig. 9) to adjust the center frequency of the coupler. Indeed, an increase in the linear capacitance of the coupler's coupled lines allows to lower the center frequency as shown by equation 9.

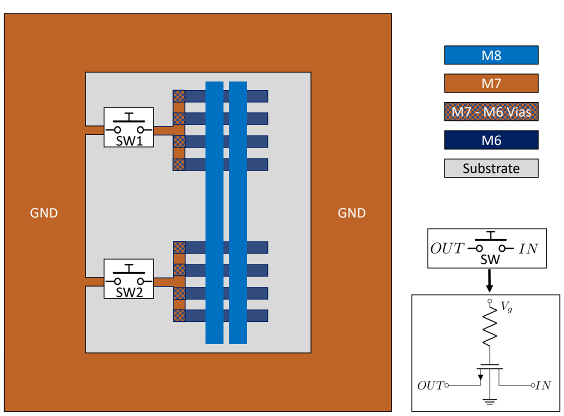


Fig. 9. Slow-wave tunable coupled lines.

In order to control the center frequency of the coupler, the *M6* bands are either kept floating or shorted to ground by CMOS switches. In the proposed example, two groups of metal strips connected by two switches allow to propose 4 different configurations.

C. *Layout Implementation*

The layout of the proposed solution (Fig. 10) shows a tunable architecture with 3 bits. Indeed, 3 groups of metal strips allow to obtain 8 different states for the transistor even if the symmetry of the coupler leads to similar states. The main component of the switch is an NMOS transistor, with 50 gate fingers of 1µm each. Indeed, the transistor is sized to minimize its internal resistance.

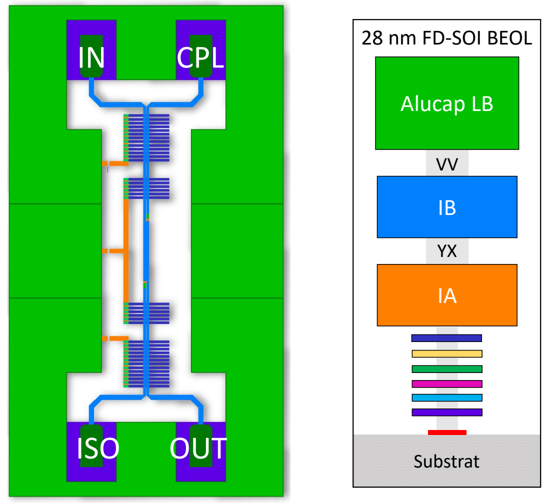


Fig. 10. Slow-wave hybrid coupler layout.

The coupled lines of the coupler are designed in *IB* layer and the twist in *IA* and *IB* layers. The metal strips placed under the coupled lines are made of *M6* layer. The closer the metal strips are to the coupled lines, the higher the linear capacitance provided. However, this implies a larger coupling and higher insertion losses. Thus, a trade-off must be found between the proximity of the tracks and the added capacitance.

IV. Measurement Results

The proposed 3-bits tunable twisted hybrid coupler (Fig. 11) is implemented in a 28nm FD-SOI CMOS 8ML process with a core area of 0.00567mm².

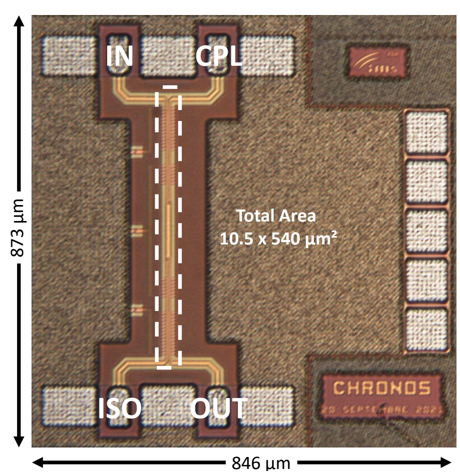
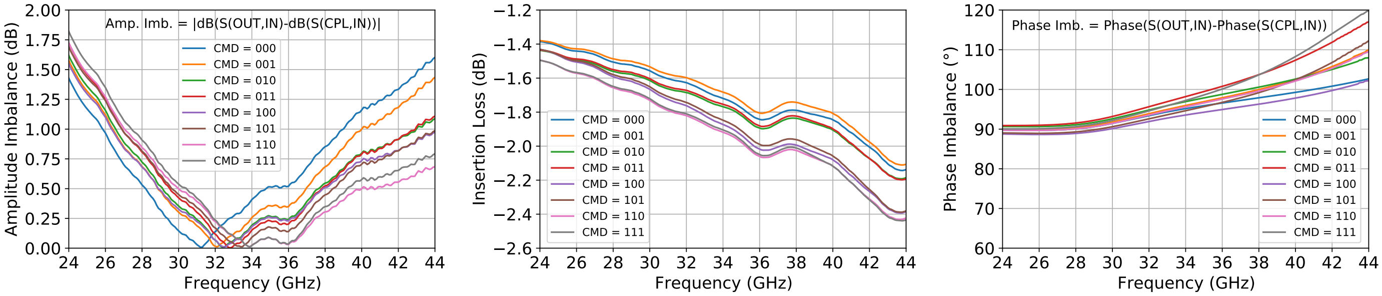


Fig. 11. Die micrograph of the proposed 28nm FD-SOI CMOS hybrid coupler.



(a) (b) (c)

Fig. 12. Slow-wave hybrid coupler performances: (a) amplitude imbalance; (b) insertion loss; (c) phase imbalance.

Table 1. Result summary of the frequency tunable quadrature hybrid coupler.

Code	000	001	010	011	100	101	110	111
f_0 (GHz)	31	32	32.5	33	32.5	34	35	35
Loss (dB)	1.6	1.68	1.65	1.7	1.8	1.85	1.95	1.97
Phase Imb. (°)	92.5	94	95	97	93	94	96	98

Table 1 summarizes the performances of the hybrid coupler (Fig. 12) as a function of the binary code used.

A. Amplitude Imbalance

The hybrid coupler achieves a frequency tunability range of 4GHz. Indeed, the center frequency can be modified from 31 to 35GHz thanks to the different binary codes. Moreover, the amplitude imbalance at 1dB reaches a bandwidth of 18GHz from 26GHz to 44GHz.

B. Insertion Loss

The coupler insertion losses remain below 2.4dB with a minimum of 1.45dB at 26GHz (code 000). However, as presented earlier, many binary codes provide identical center frequencies. Therefore, many cases are not used due to their high losses. For example, the maximum losses at 44GHz are 2.2dB with code 011 rather than 2.4dB for codes 110 and 111. These measurements are made with long access tracks which bring additional losses to the coupler (Fig. 12). These losses are estimated after de-embedding at 0.5dB. In the case of implementation with a PA, these losses should be eliminated.

C. Phase Imbalance

The phase imbalance between the two paths OUT and CPL is between 90° and 120° on the 26-44GHz band. This discrepancy is due to the inclusion of PADs (large capacitances) that deteriorate the phase imbalance. By taking the codes 000 and 100, the phase remains between 90° and 100° covering the whole frequency band of the coupler.

D. Comparison with the state of the art

Table 2 provides a comparison between the realized coupler and the state of the art of hybrid couplers. The slow-wave hybrid coupler has the highest relative bandwidth at 1dB amplitude imbalance. Unlike the reconfigurable architecture with capacitor bank, this coupler has much lower insertion losses. Its phase imbalance is finally more important than the other architectures but this result is due to the taking into account of the PADs.

Table 2. Comparison with the state of the art of CMOS hybrid couplers.

Reference	This Work	[4]	[5]	[6]	[7]
Technology	28nm FD-SOI	130nm BiCMOS	130nm BiCMOS	28nm FD-SOI	28nm FD-SOI
Tunability	Slow Wave	No	No	No	Capa. Banks
Frequency (GHz)	26	28	18.75	29.2	30
BW_{1dB} (%)	51	10	17	33	40
Amp. Imbalance (dB)	1	1	2	1	1
Insertion Loss (dB)	1.45	5.1	0.5	0.62	3.23
Phase Imb. (°)	95±5	89.3 ±5	91±1	93.7±1	85±3
Circuit Area (μm^2)	5670	258752	14400	5200	15264

V. Conclusion

A new CMOS quadrature-twisted hybrid coupler using an innovative tunable topology based on the slow-wave principle is presented in this paper. Thanks to slow-wave metal strips placed under the tracks of the coupler to increase the linear capacitance of its coupled lines, the coupler presents a wideband behavior with a relative bandwidth at 1dB of amplitude imbalance of 51% and low insertion losses below 2.2dB. In addition, the coupler exhibits the smallest dimensions in the state of the art thanks to its twisted structure.

Acknowledgment

The authors would like to thank STMicroelectronics for chip fabrication and Rohde & Schwarz for measurements.

References

[1] G. Diverrez *et al.*, "A 24-31GHz 28nm FD-SOI CMOS Balanced Power Amplifier Robust to 3:1 VSWR for 5G Application," EuMC, 2022.
[2] N. S. Mannem *et al.*, "A Reconfigurable Series/Parallel Quadrature Coupler Based Doherty PA in CMOS SOI with VSWR Resilient Linearity and Back-Off PAE for 5G MIMO Arrays," ISSCC, 2020.
[3] V. Qunaj and P. Reynaert, "A Doherty-Like Load-Modulated Balanced Power Amplifier Achieving 15.5dBm Average Pout and 20% Average PAE at a Data Rate of 18Gb/s in 28nm CMOS," ISSCC, 2021.
[4] M. G. Bautista *et al.*, "Design of on-chip quadrature hybrid (3dB) branch-line couplers in 0.13-μm SiGe technology for millimetre-wave applications," ISCIT, 2017, pp. 1–5.
[5] M. Potereau *et al.*, "Ultra-Compact Low-Loss Integrated Transformer Based Ku-Band Quadrature Hybrid Coupler," EuMIC, 2018.
[6] B. Moret *et al.*, "A 28GHz self-contained power amplifier for 5G applications in 28nm FD-SOI CMOS," LASCAS, 2017.
[7] V. Knopik *et al.*, "Integrated scalable and tunable RF CMOS SOI quadrature hybrid coupler," EuMIC, 2017.
[8] F. Grover, "Inductance Calculations: Working Formulas and Tables," Dover, New York , 1962.
[9] B. Leite, "Design and modeling of mm-wave integrated transformers in BiCMOS technologies," 2011.