A W-Band Phase-Shifter-Embedded PA in 40-nm CMOS for 6G Applications

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***Abstract*—A phase-shifter-embedded (Δφ-embedded) power amplifier (PA) incorporating multifunctional Δφ-embedded impedance matching networks (IMN) is proposed for 6G applications. The Δφ-embedded IMN can realize impedance transformation, execute a single-ended to differential conversion, and simultaneously provide a phase shift without requiring additional circuits. Hence, the insertion loss, occupied chip area, and power dissipation can be reduced. Realized in a 40-nm digital CMOS process, the proposed PA can provide a maximum saturated output power of 10.2 dBm and a phase-shifting range wider than 90° from 75 to 89 GHz. The power consumption is 151 mW from a 1.1-V supply.**

***Keywords*—CMOS, coupled resonators, W-band, phase shifter, 6G.**

I. Introduction

Terahertz (THz) science and technology have attracted significant attention recently. It has been considered a strong candidate for the sixth-generation (6G) high-speed wireless communication system to supply a data rate higher than 100 Gb/s [1]. To tackle the problem of high path loss at THz frequencies, phased-array technology is a must. The signals radiated and accepted by regularly-deployed transmitters and receivers, respectively, are combined in the desired directions, increasing the phased array's equivalent isotropically-radiated power and signal-to-noise ratio.

LO-phase-shifting architectures are usually adopted for sub-THz/THz phased-array transceivers [2]. The required LO signals for frequency up-/down-conversion are generated by an amplifier-frequency-multiplier chain (AMC) whose first stage is a phase shifter for controlling the signal's phase. However, the frequency multiplication ratio N of the prior AMC works is large, for instance, N= 8 in [2] and N= 9 in [3], which occupies a large chip area and dissipates a high dc power due to the cascade of many phase shifters, power amplifiers (PA), and frequency multipliers. Moreover, the phase resolution and phase noise of the generated LO signals are degraded by N and 20Log$N$, respectively. In this work, a phase-shifter-embedded (Δφ-embedded) W-band PA incorporating multifunctional Δφ-embedded impedance matching networks (IMN) is proposed for sub-THz/THz phased-array applications. The proposed Δφ-embedded IMN can use a single circuit to realize versatile functions of impedance transformation, single-ended to differential conversion, and phase shifts simultaneously. Therefore, the proposed W-band PA not only occupies a small chip area but can also be exploited to generate a phase-controlled sub-THz/THz LO signal with high output power and fine phase resolution. Realized in a 40-nm digital CMOS process without ultra-thick metal (UTM) layers available, the proposed PA can deliver a maximum saturated output power of 10.2 dBm and simultaneously provide a phase-shifting range Δφ wider than 90° from 75 to 89 GHz. The proposed PA could be integrated with a frequency quadrupler to realize a 300-356-GHz LO signal with a full 360° continuously-tuned Δφ for the 6G applications. The following sections will explain the design details of the proposed Δφ-embedded W-band PA.

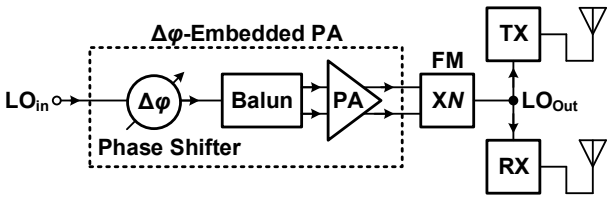


Fig. 1. LO-phase-shifting phased-array transceiver with the proposed Δφ embedded PA for the LO generation.

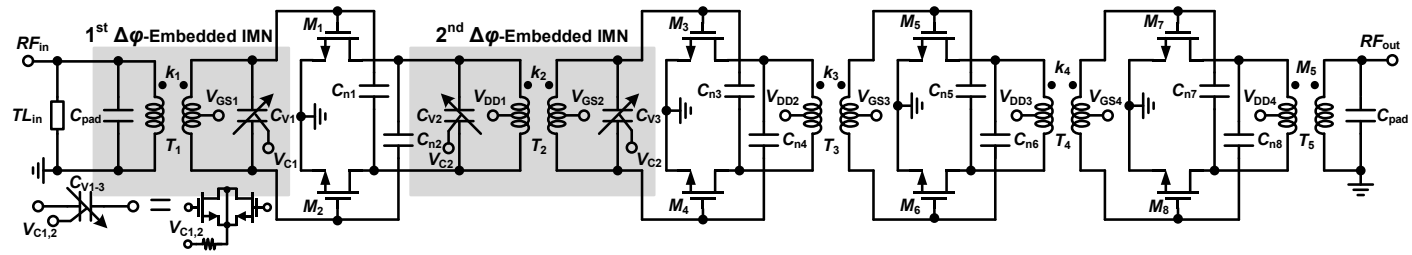
II. Proposed Δφ-Embedded W-Band PA

A. LO-Phase-Shifting Phased-Array Architecture

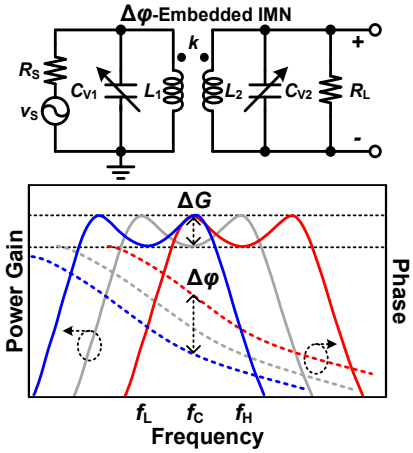
Fig. 1 shows a typical architecture of LO-phase-shifting phased-array transceivers for sub-THz/THz applications. The phase-shifting function is implemented on the LO path by an AMC which cascades a phase shifter, a balun for a single-ended to differential conversion, a PA, and a frequency multiplier (FM) with a frequency multiplication ratio of N. In this work, a small number of 3 and 4 can be chosen for N to generate the required sub-THz/THz LO signals, implying that the chip area, power dissipation, and degradation of the phase resolution and phase noise can be reduced. Moreover, the functions of phase shifts, impedance transformation, and balun can be realized using a single Δφ-embedded PA circuit whose design target is to provide high output power and a phase-shifting range wider than 90°. Thus, as the proposed PA is integrated with a ×4 FM, a THz LO signal with a full 360° continuously phase-shifting range can be obtained.

B. Δφ-embedded PA

Fig. 2(a) illustrates the proposed Δφ-embedded W-band PA realized in a 40-nm digital CMOS without UTM layers available. The distance from the 0.85-μm thick top metal layer to the lossy silicon substrate is only 4.1 μm, leading to the passive components with much higher loss than that of an RF process with UTM layers. The proposed PA biased in a class-

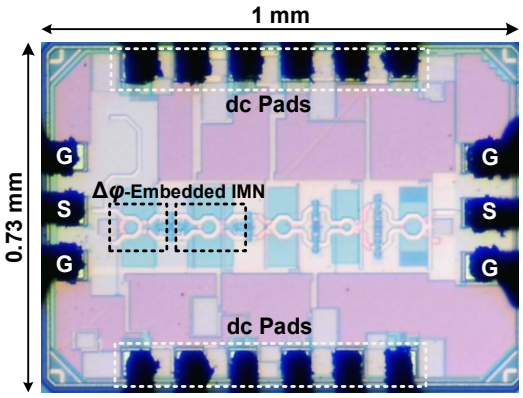


(a)



(b)

$M_{1\text{-}4}$'s (W/L)	$M_{5,6}$'s (W/L)	$M_{7,8}$'s (W/L)
28/0.04	56/0.04	128/0.04
k_1	L_{T1} (pH)	k_2
0.46	90	0.57
k_4	L_{T4} (pH)	k_5
0.48	31.4	0.69
$C_{n1\text{-}4}$ (fF)	$C_{n5,6}$ (fF)	$C_{n7,8}$ (fF)
9	17	31
C_{V1}'s (W/L)	C_{V2}'s (W/L)	C_{V3}'s (W/L)
32/0.13	13/0.13	21/0.13
L_{T2} (pH)	k_3	L_{T3} (pH)
82	0.68	51
L_{T5} (pH)	$R_{B1\text{-}4}$ (kΩ)	TL_{in} (μm)
61.2	4	70
C_{pad} (fF)	$V_{DD1\text{-}4}$ (V)	$V_{GS1\text{-}4}$ (V)
40	0.9	0.7



(c)

Fig. 2. (a) Proposed Δφ-embedded W-band PA. (b) Proposed multifunctional Δφ-embedded IMN. (c) Chip photo of the proposed Δφ-embedded W-band PA.

A region comprises four amplifier stages whose transistor size is designed to have a ratio of roughly $M_{1\text{-}2}$:$M_{3\text{-}4}$:$M_{5\text{-}6}$:$M_{7\text{-}8}$= 1:1:2:4 to deliver a high output power as well as high gain. $M_{7\text{-}8}$ can provide an ideal saturated output power of 13 dBm as the power-matched condition is fulfilled. Neutralization capacitors $C_{n1\text{-}8}$ are added to increase the PA's gain and stability. The interstage impedance matchings between the second and third and third and fourth stages are achieved by transformers T_3 and T_4, respectively. The output transformer T_5 is employed to transform a 50-Ω load to the optimal impedance Z_{opt} of 9.2+14.4j Ω to obtain the maximum output power. T_5 also works as a balun to convert a differential output to a single-ended one. The simulated amplitude and phase imbalances of the T_5 balun are smaller than 1 dB and 5°, respectively, from 75 to 99 GHz. The proposed multifunctional Δφ-embedded impedance matching networks, 1st and 2nd Δφ-embedded IMNs, are utilized to achieve the impedance-matched conditions at the input and between the first and second stages and simultaneously provide phase shifts, respectively. Moreover, the 1st Δφ-embedded IMN can also function as a balun.

The operation principle of the proposed Δφ-embedded IMN can be explained in Fig. 2(b). It comprises two LC resonators coupled magnetically, i.e., inductively-coupled resonators. A transformer is used to realize the coupled inductors, which implies that the ICR can also work as a balun. The capacitors C_{V1} and C_{V2} are implemented by varactors whose capacitance values can be tuned by a control voltage V_C. R_S and R_L model the source and load resistances, respectively. The typical power gain and phase frequency responses of an ICR are shown in Fig. 2(b). The ICR possesses two resonance frequencies, f_L and f_H, leading to a broadband frequency response [4]. As the conditions of L_1C_{V1}= L_2C_{V2} and n^2= R_S/R_L are satisfied, the ICR can conduct an impedance transformation from R_S to R_L with the lowest insertion loss at f_L and f_H simultaneously. The gain flatness ΔG between f_L and f_H is determined by the coupling coefficient k of the transformer and the quality factor Q defined as $R_S\omega_0C_{V1}$= $R_L\omega_0C_{V2}$ where ω_0 is $1/\sqrt{L_1C_{V1}(1-k^2)}$ = $1/\sqrt{L_2C_{V2}(1-k^2)}$ [4]. As C_{V1} and C_{V2} are tuned by V_C, f_L and f_H are changed accordingly, resulting in the frequency shift of the gain peaks and the change of the signal phase. As indicated in Fig. 2(b), f_L and f_H are designed to keep the operation frequency f_C between f_L and f_H as C_{V1} and C_{V2} are varied. By doing this, the ICR can provide a phase shift Δφ with a gain variation ΔG. Therefore, the proposed Δφ-embedded IMN can simultaneously realize a single-ended to differential conversion, impedance transformation, and phase shifts without requiring additional circuits.

In this work, the 1st and 2nd Δφ-embedded IMNs are designed to contribute phase shifts Δφ_1 and Δφ_2 larger than 45° at 85 GHz, respectively, leading to a total phase shift wider than 90°. For the 1st Δφ-embedded IMN design, since the primary coil of T_1 is connected to the input pad where the signal is single-ended, the advantage of a virtual-short condition cannot be employed. Adding a varactor here will require many lossy dc-blocking capacitors to bias the varactor, greatly increasing insertion loss. Hence, only the capacitor on the secondary coil of T_1 is replaced by a variable capacitor C_{V1}. To achieve the required Δφ_1 of 45°, C_{V1} shall be varied from 36 to 56 fF to tune f_L and f_H from 81 to 85 GHz and 85 to 89 GHz, respectively. Fortunately, the parasitic capacitances from the input of the first stage, the probing pads, and the transformer itself can be

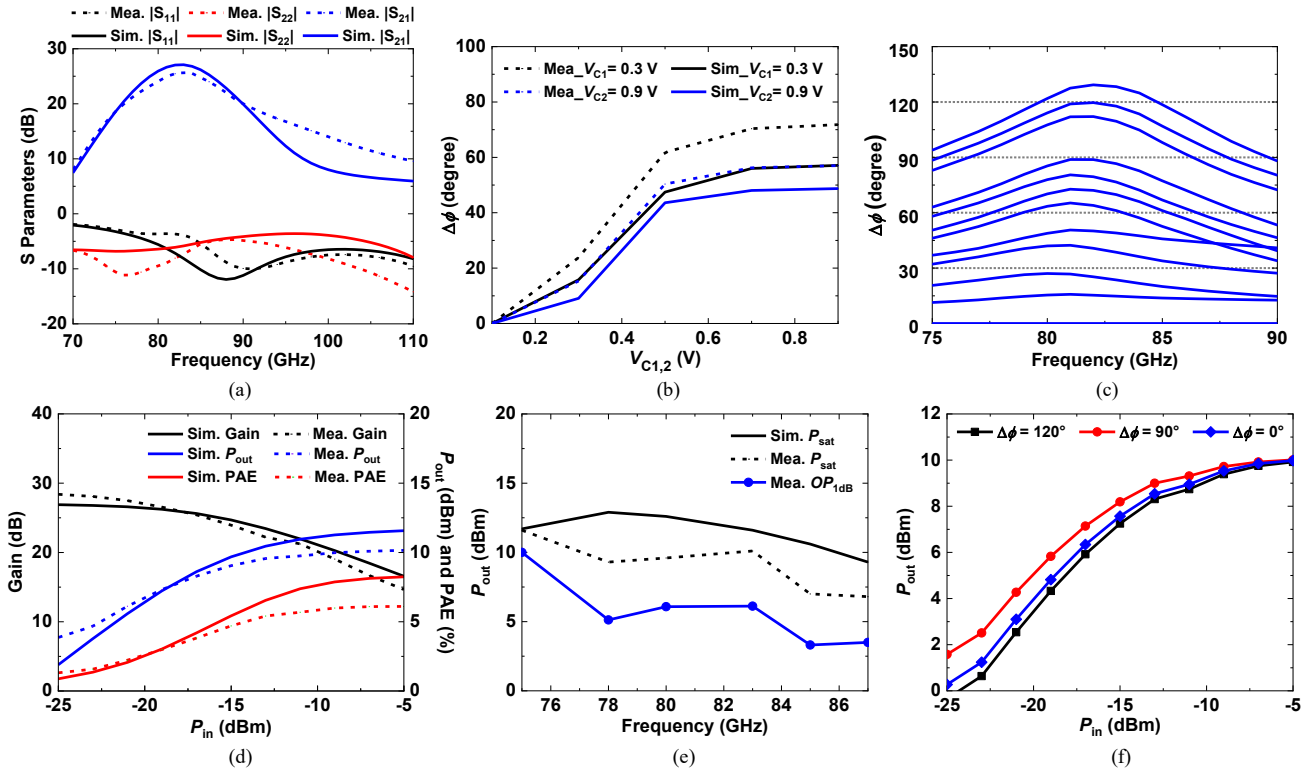


Fig. 3. (a) Measured S parameters. (b) Measured output phase as V_{C1} and V_{C2} are changed. (c) Measured frequency response of the output phase. (d) Measured gain, P_{out}, and PAE versus the input power P_{in}. (e) Measured frequency response of P_{sat} and OP_{1dB}. (f) Measured P_{out} versus P_{in} under different phase states.

absorbed into the ICR design. Therefore, C_{V1} only needs to change from 14 to 34 fF. NMOS transistors are employed to realize the varactors. The width and length of the transistor for realizing C_{V1} are designed at 32 and 0.13 μm, respectively. The simulated $\Delta\varphi_1$, ΔG, and the minimum insertion loss of the 1st $\Delta\varphi$-embedded IMN are 47°, 2.2 dB, and 7.2 dB at 85 GHz, respectively, as V_{C1} is varied from 0.1 to 0.9 V and V_{GS1} is 0.7 V. The simulated amplitude and phase imbalances of the 1st $\Delta\varphi$-embedded IMN's differential output are smaller than 1 dB and 5°, respectively, from 75 to 110 GHz. For the 2nd $\Delta\varphi$-embedded IMN design, the varactors C_{V2} and C_{V3} shall be varied from 26 to 39 fF to achieve $\Delta\varphi_2$ of 55°. Note that $\Delta\varphi_2$ is designed 10° wider than the required 45° to have enough phase-shifting margin since the 1st $\Delta\varphi$-embedded IMN only has a single tuning varactor. C_{V2} and C_{V3} only need to change from 7 to 16 fF after taking the parasitic capacitances from the transformer and the output and input of the first and second stages into the ICR design. Since the common-mode dc voltages of V_{DD1} and V_{GS2} on the primary and secondary coils of T_2 are 0.9 and 0.7 V, respectively, the tuning ranges of C_{V2} and C_{V3} with the same control voltage V_{C2} are different. To obtain the same capacitance tuning range, the width and length of the transistors for realizing C_{V2} and C_{V3} are designed at 13 and 0.13 μm and 21 and 0.13 μm, respectively. The simulated $\Delta\varphi_2$, ΔG, and the minimum insertion loss of the 2nd $\Delta\varphi$-embedded IMN are 57°, 3.4 dB, and 5.5 dB at 85 GHz, respectively, as V_{C2} is varied from 0.1 to 0.9 V and V_{GS1} is fixed at 0.7 V, which meets the requirement. Finally, a transmission line TL_{in} with a length of 70 μm is added to minimize the parasitic effect caused by the probing pads. With the proposed $\Delta\varphi$-embedded IMNs, the proposed $\Delta\varphi$-embedded W-band PA can provide a simulated small signal gain of 27.1 dB, an output 1-dB compression point OP_{1dB} of 8 dBm, a saturated output power P_{sat} of 11.6 dBm, and a phase-shifting range larger than 90° from 74 to 86 GHz.

III. Experimental Results

The proposed $\Delta\varphi$-embedded W-band PA is realized in a 40-nm digital CMOS process without UTM layers available. The chip photo is shown in Fig. 2(c). The measurement is conducted by an on-wafer setup where the input and output high-frequency signals RF_{in} and RF_{out} are applied and acquired through GSG probes, respectively, while dc biases are given by PGPPGP dc probes. The proposed W-band PA consumes 151 mW from a 1.1-V supply.

The measured S parameters are illustrated in Fig. 3(a). The proposed PA can provide a peak $|S_{21}|$ of 25.7 dB at 83 GHz with a 3-dB bandwidth from 79 to 87 GHz as $V_{DD1\text{-}4}$ and $V_{GS1\text{-}4}$ are 0.9 and 0.7 V, respectively. As shown in Fig. 3(b), the measured $\Delta\varphi_1$ and $\Delta\varphi_2$ at 83 GHz as V_{C1} and V_{C2} are varied from 0.1 to 0.9 V, and V_{GS1} is changed to 0.8 V are 57.1 and 71.8°, respectively, resulting in a maximum $\Delta\varphi$ of 128.9° with ΔG of 4.2 dB. The measured $\Delta\varphi$ is larger than the simulated one due to the capacitance variation of the varactors. It is found that each varactor roughly contributes an 8° difference. The measured frequency response of the phase shift is depicted in Fig. 3(c). A maximum $\Delta\varphi$ of 128.9° is measured at 83 GHz while keeping $\Delta\varphi$ wider than 90° from 75 to 89 GHz when V_{C1} and V_{C2} are changed from 0.1 to 0.9 V, respectively. The phase

Table 1. Performance Summary and Comparison with Prior Works

Reference	JSSC'22 [5]	TMTT'21 [6]	MWCL'20 [7]	MWCL'20 [8]	TMTT'15 [9]	This work
CMOS Technology	65 nm	28-nm SOI	40 nm	65 nm	40 nm	**40-nm**
UTM Available	Yes	Yes	Yes	Yes	Yes	**No**
Topology	8-way diff.[(a)] CS	1-way diff. CS	2-way Cascode	2-way CS	4-way diff. CS	**1-way diff. CS**
V_{DD} (V)	1.2	1	1.8	1.2	0.9	**1.1**
f_o (GHz)	84	77	110	77	70.3-85.5	**83**
G_P (dB)	29.3	26.5	25.5	26.4	18.1	**25.7[(c)]**
OP_{1dB} (dBm)	16.2	10	10.3	11.5	17.8	**6.1**
P_{sat} (dBm)	19.1	13.5	12.2	15.8	20.9	**10.2**
Estimated $P_{sat,1\text{-}way,wi\text{-}PS}$ [(b)] (dBm)	3.1	6.5	-0.8	5.8	7.9	**10.2**
PAE (%)	8.6	14.5	8.5	15.9	22.3	**6.6**
$\Delta\varphi/\Delta G$ (°/dB)	0	0	0	0	0	**128.9/4.2**
P_{dc} (W)	0.582	0.15	-	0.24	0.375	**0.151**
Chip Area (mm2)	0.72	0.14	0.24	0.14	0.57	**0.73**

(a) Differential. (b) Estimated 1-way P_{sat} with a phase shifter $P_{sat,1\text{-}way,wi\text{-}PS} = P_{sat} - 10\text{Log}N_C - 6$ dB, where N_C is the number of the power-combining ways assuming the power-combing network is lossless, and 6 dB is the insertion loss of a 90° phase shifter reported in [10]. (c) V_{DD4}= 0.9 V.

can be continuously tuned by V_{C1} and V_{C2} within the 128.9° phase-shifting range. Note that with the measured $\Delta\varphi$ wider than the simulated one, the proposed $\Delta\varphi$-embedded W-band PA can also be integrated with a ×3 FM to generate a 225-267-GHz sub-THz LO signal with a full 360° continuously phase-shifting range. The measured OP_{1dB} and the power-added efficiency (PAE) at 83 GHz are depicted in Fig. 3(d) as V_{DD4} is changed to 1.1 V. The proposed PA can provide P_{sat} of 10.2 dBm and OP_{1dB} of 6.6 dBm with a peak PAE of 6.6%. Fig. 3(e) depicts the measured frequency responses of P_{sat} and OP_{1dB}. P_{sat} has a peak value of 11.6 dBm at 75 GHz and decreases to 6.8 dBm at 87 GHz. The measured P_{out} versus the input power P_{in} under the phase states of 0, 90, and 120° is indicated in Fig. 3(f). The variation of P_{sat} is only 0.1 dB within a 120° phase-shifting range. The performance of the proposed $\Delta\varphi$-embedded PA and its comparison with prior works are summarized in Table 1. The proposed PA without UTM layers available can provide a compatible output power while providing a phase shift of 128.9° at 83 GHz with a $\Delta\varphi$ wider than 90° from 75 to 89 GHz. To the best of the authors' knowledge, the proposed PA is the first work that can provide an additional phase-shifting function reported thus far. With the advantageous phase-shifting function, the proposed PA can be a strong candidate to realize a phase-controllable LO signal for 6G LO-phase-shifting phased-array transceivers.

IV. Conclusion

A phase-shifter-embedded ($\Delta\varphi$-embedded) W-band PA is proposed and successfully verified by experimental results. The phase-shifting function is enabled by integrating the proposed multifunctional $\Delta\varphi$-embedded impedance matching networks, which can simultaneously realize a single-ended to differential conversion, impedance matching, and phase shifts without requiring additional c. Realized in a 40-nm digital CMOS process, the proposed PA can deliver a saturated output power of 10.2 dBm and a maximum phase-shifting range $\Delta\varphi$ of 128.9° at 83 GHz while maintaining $\Delta\varphi$ wider than 90° from 75 to 89 GHz.

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