H-Band Differential Cascode Power Amplifier Achieving 9.5-dBm OP1dB at 260 GHz in 250-nm InP DHBT Process

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***Abstract*—We present a 260-GHz differential cascode power amplifier in the 250-nm InP DHBT process. For the on-wafer measurement or waveguide packaging, on-chip baluns or dipole waveguide transitions were monolithically integrated. From the on-wafer measurement, the peak small signal gain (S21) and 3-dB bandwidth are 19.5 dB at 260 GHz and 25 GHz in the range of 254.2–279.2 GHz, respectively. The maximum output power, OP1dB, and PAE_{MAX} are 10.2 dBm, 9.5 dBm, and 3.1%, respectively, at 260 GHz.**

***Keywords*— THz wave, power amplifier, cascode, InP DHBT, on-chip Balun, on-chip transition.**

I. Introduction

The challenges in the terahertz (THz) frequency band above 100 GHz are to produce high-power signal and to detect weak signal with high sensitivity. Thanks to recent advances in semiconductor electronic device technologies such as III-V heterojunction bipolar transistors (HBTs) [1] and high-electron mobility-transistors (HEMTs) [2], solid-state power and low-noise amplifiers at THz frequencies have become available. In addition, various THz applications, including wireless communications systems, have been successfully demonstrated with promising performance over huge bandwidth (BW) [3].

Here, we present an H-band three-stage differential power amplifier (PA) with an optimized cascode (CC) unit cell in 250-nm InP HBT technologies. The PA was integrated with on-chip differential dipole waveguide transitions for a WR3.4 split-block waveguide module.

II. Amplifier Design

A. Unit cell for Drive and Power Stages

Though maximum oscillation frequency (f_{max}) of recent state-of-the art III-V transistors exceeds 1 THz, achievable gain at, for instance, 250 GHz, is actually quite low due to parasitics of core transistors and resistive loss associated with passive elements. Therefore, for THz amplifiers with considerable gain and output power, it is essential to optimize the amplifier core for reduced parasitics and increased gain. In this study, a CC structure that provides high reverse isolation, excellent power gain, and more output power than a single common-emitter (CE) or common-base (CB) structure was employed as the PA unit cell [1]. Low-loss and high-gain cores enable us to decrease the number of stages and reduce the fatal matching loss associated with passive elements, finally resulting in large power density and potentially high output power. A compact layout and small chip are other advantages for additional power boosting in circuits and/or packages [4].

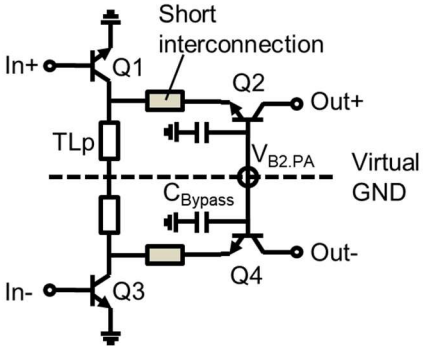


Fig. 1. Schematic diagram of CC unit cell using shunt transmission line for inter-device matching.

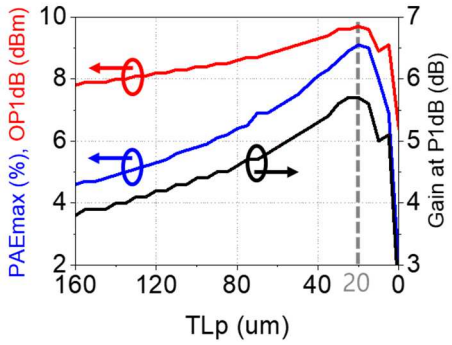


Fig. 2. Simulated PAE_{MAX}, OP1dB, and gain performance for TLp change in half circuit of CC unit cell.

In the H-band frequency range, CC topology may not provide sufficient output power due to parasitic capacitance between CE and CB stages, and a suitable inter-device matching network (IDMN) can help to compensate for the parasitic capacitances [5].

Fig. 1 shows a schematic diagram of the differential CC unit cell with a shunt transmission line (TLp) as the IDMN. Note that the short interconnection between CE and CB transistors is electrically non-negligible at THz frequencies and thus should be considered for the IDMN design. Assuming a three-finger 6-μm HBT as a unit transistor, the maximum PAE (PAE_{MAX}), output power at 1-dB compression point (OP1dB), and power gain at the OP1dB in the half-circuit of the CC unit cell were evaluated from load-pull simulation with respect to TLp length in the range of 160–0 μm. As can be seen in Fig. 2, at TLp = 20 um, the core exhibited the best performance in power gain, OP1dB, and PAE_{MAX}. Therefore, a 20-μm TLp was selected for configuring the PA core in this work.

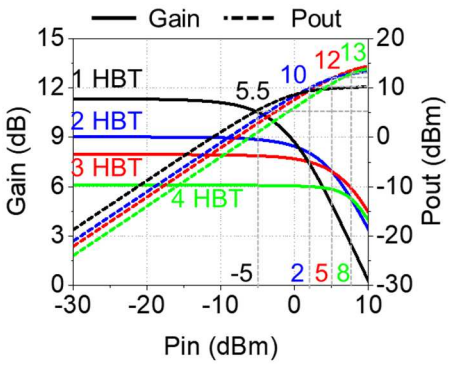
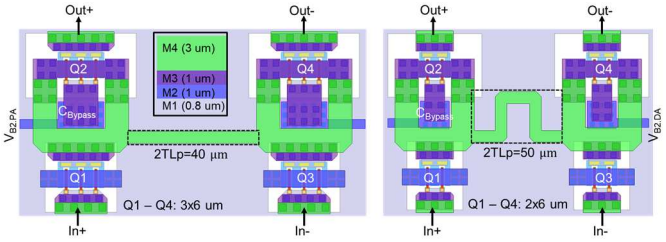


Fig. 3. Simulated gain and output power according to the number of transistors constituting the unit cell.



(a) (b)

Fig. 4. Layout of the CC (a) power stage and (b) drive stage with compensation transmission.

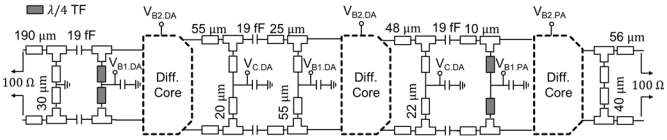
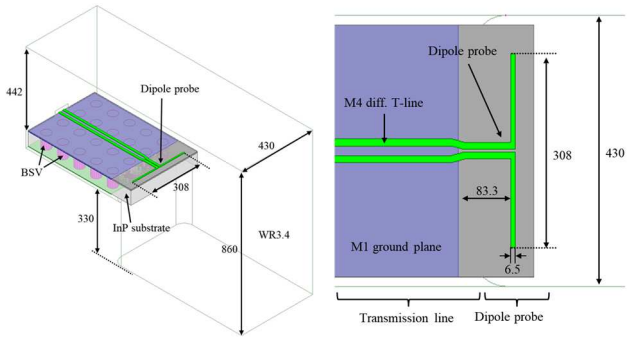


Fig. 5. Schematic diagram of proposed three-stage PA.

Device size (or the number of fingers) for each stage should be carefully selected for maximum output power from the output stage without signal saturation in the driving stages. Fig. 3 shows the gain and output power of multi-finger HBT CC cores at various input powers from the load-pull simulations. Note that the optimum IDMN and conjugated input matching were used for each case. As can be seen, as the number of fingers increases, Pout increases but gain decreases due to parasitics. The differential CC cell with three or four fingers offers large output power of more than 10 dBm, but also requires large enough input power from the prior stage due to the low gain. Considering additional loss from the inter-stage and output stage matching, gain lower than 6 dB from the output stage should be avoided; for instance, assuming 2-dB loss from the inter-stage matching and a 2-dB margin for linearity, 13-dBm OP1dB from the four-finger cell requires 11 dBm or more from the prior stage. From this perspective, we used two fingers for the first stage and second stage of the PA, and three fingers for the third stage. Fig. 4 illustrates the final layout of the differential CC cores for the driving and output stages. The input and output ports and TLp for the capacitor compensation were constructed using the top metal layer for low loss. Short series transmission lines were added at the



(a) (b)

Fig. 6. Schematic diagrams of the dipole coupler for the transition from chip to WG. (a) Three-dimensional view; (b) top view.

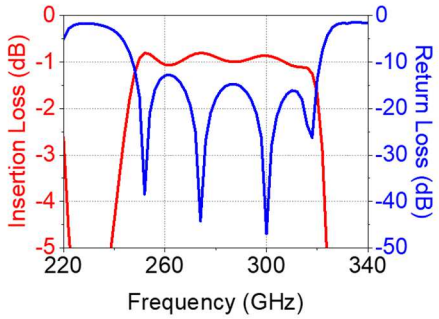


Fig. 7. Simulated S-parameter results for dipole coupler with BtoB structure.

emitter of the CB stage to secure a small area for the base capacitor of the CB stage.

B. Differential Power Amplifier

Differential RF circuits serve several advantages; biases can be simply applied through common nodes without additional large bypass capacitors of which the Q-factor is quite limited at high frequencies. Similarly, shunt stubs can be implemented through common nodes. In addition, the output power of the PA can be increased by combining the output power through output baluns.

Fig. 5 shows a schematic of the H-band three-stage PA in this work. Inter-stage matching was designed based on the capacitively coupled resonator (CCR) scheme, which provides the fourth-order filter response over a wide bandwidth with flat in-band gain performance [6]. In detail, both the conjugate impedance and the load-pull impedance were considered, and the inter-stage matching network was optimized to make DAs deliver high enough power to the core in the next stage. Output matching converts the 50-ohm impedance of a coupler and balun to a load pull impedance of $4 + j34$ ohms, taking into account high output power and high PAE.

C. On-Chip Balun and Coupler Design

In this work, the PA was designed in two versions: one with on-chip baluns for the single-ended to differential signal conversion (and vice versa) and the other with on-chip dipole couplers for the waveguide transition. In order to minimize the occupied area for the rat race coupler, the folded rat-race

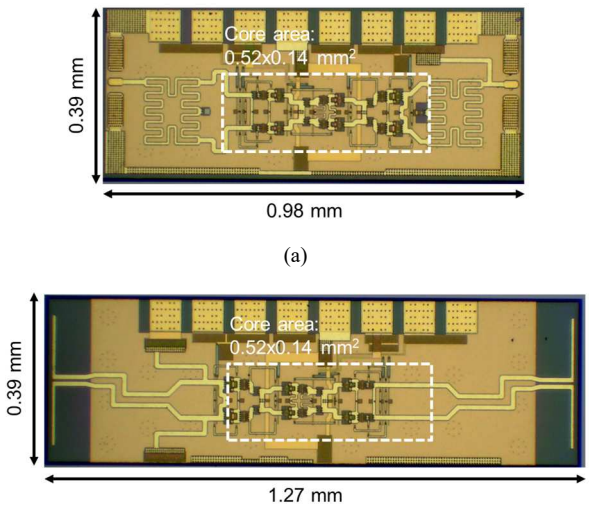


Fig. 8. Micrograph of fabricated PAs: (a) with balun for on-chip measurement; (b) with on-chip dipole coupler for module measurement.

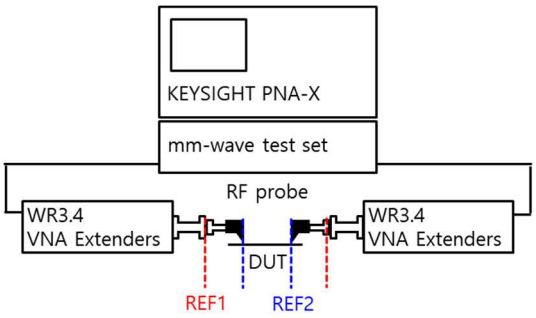


Fig. 9. Block diagram of measurements setup.

coupler was employed [7]. It occupies one-tenth of the area compared to the conventional circular layout. The EM simulated insertion loss of the balun is less than 0.7 dB in the design frequency, and the return loss at each port is better than 15 dB. The simulated phase difference and amplitude imbalance between the differential ports were 10 degrees or less and 1 dB or less, respectively.

The detailed dimensions of the designed dipole coupler are shown in Fig. 6. The coupler is designed on a 75-μm-thick InP substrate with a 6.6-μm-thick benzocyclobutene (BCB) layer. The ground plane and dipole couplers were formed with M1 and M4 layers, respectively. In order to suppress the parasitic modes propagating in the substrate, backside vias (BSVs) were densely placed at the edge of the ground plane. Fig. 7 shows the EM simulation results for the back-to-back (BtoB) structure (i.e., 490-μm-long differential microstrip line–dipole coupler–WR3.4 waveguide–dipole coupler–490-μm-long differential microstrip line). In the 250–320 GHz band, the S21 of the BtoB structure was around -1 dB or slightly lower, implying the single on-chip transition loss would be around 0.5 dB or less, which is quite compatible with similar prior work [8].

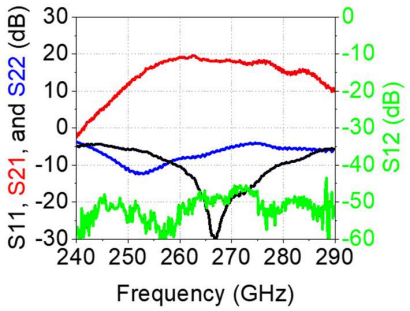


Fig. 10. Measured S-parameters.

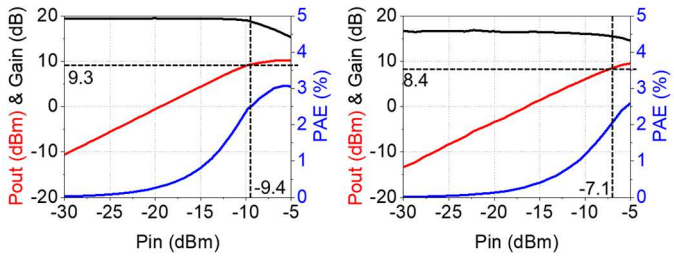


Fig. 11. Measured Pout, gain, and PAE at (a) 260 GHz and (b) 275 GHz.

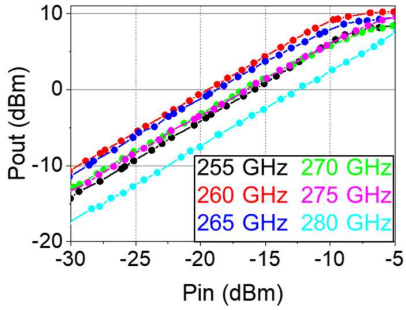


Fig. 12. Measured output power versus input power at various frequencies.

III. Measurement Results

The three-stage PA was fabricated in the 250-nm InP DHBT process. Fig. 8 shows a microphotograph of the fabricated PAs. Both amplifiers have a core area of 0.52 × 0.14 mm^2, and the total chip areas are 0.98 × 0.39 mm^2 and 1.27 × 0.39 mm^2 for the on-chip balun and coupler versions, respectively. The height of the chip was limited to 0.39 mm for a smooth mode transition between the on-chip coupler and WR3.4 waveguide in the E-plane. As depicted in Fig. 9, the fabricated PAs with the baluns were measured with a Keysight network analyzer (PNA-X N5247B), mm-wave testset (N5292A), VDI's WR3.4 VNAX frequency extenders, and cascade waveguide infinity probes (I325-T-GSG-50-BT). The amplifier was biased by DC probes at $I_{C.PA}$ = 39.2 mA and $I_{C.DA}$ = 42 mA. The amplifier consumes total dc power of 330 mW under the small signal condition.

For S-parameter measurements, VNA was calibrated with a source power of -30 dBm. Fig. 10 shows the measured S-parameter of the PA. The measured peak small signal gain (S21) is 19.5 dB at 260 GHz, and the 3dB-BW is 25 GHz in the range of 254.2–279.2 GHz.

Table 1. Performance comparison with H-band PAs

Ref.	Tech.	Freq. (GHz)	Topology	S21 (dB)	BW_{3dB} (GHz)	OP1dB (dBm)	Psat (dBm)	PAE (%)	P_{DC} (mW)	Area (mm^2)	Psat/Area (mW/mm2)
[9]	130-nm SiGe	252	2-way Comb. 3-stage CC	21.5	11	-3.7	0>	0.3	149	0.17	NA
[10]	250-nm InP	270	4-way Comb. 4-stage CB	20.5	48	10.5#	14-16.8	2.2–4	1090	0.83	57.6
[11]	130-nm SiGe	290	4-way Comb. 4-stage CC	15	67	3.3	5	1.19	267	0.58	5.44
[12]	35-nm InGaAs	300	4-way Comb. 5-stage CS	19	57	3.8#	8	2.97	202	1.5	4.2
[13]	250-nm InP	232	2-way Comb. 2-stage CC	20.8	51	4.8#	9.4	NA	124	0.244	35.6
[14]	130-nm InP	325	2-way Comb. 2-stage CC	16.6	9	8.5#	11.3	1.1	1120	0.98	13.9
[15]	130-nm SiGe	254	2-way Comb. 3-stage CC	20.1	63	5.2	8.2	1.38	360	0.26	27.2
This work	**250-nm InP**	**260**	**2-way Comb. 3-stage CC**	**19.5**	**25**	**9.5**	**10.2**	**3.1**	**330**	**0.38**	**27.6**

#graphical estimation

For the large signal measurements, the port power calibration was performed with a power meter (PM5) at the end of the waveguide ports (REF1), and the reference planes were then move to the end of the on-wafer probes (REF2) by embedding the on-wafer probes. Note that the measurement procedure in this work ensured that harmonics and noise power from the PA would not be counted in the measured power level. Fig. 11(a) and (b) show the measured large signal performance at 260 and 275 GHz, respectively. The measured maximum output power, OP1dB, and PAE_{MAX} were 10.2 dBm, 9.5 dBm, and 3.1%, respectively, at 260 GHz. Similarly, at 275 GHz, 9.6-dBm maximum output power and 8.4-dBm OP1dB, and 2.6% PAE_{MAX} were measured. Fig. 12 shows the output power versus input power from 255 to 280 GHz. In the frequency range of interest, the PA exhibits a maximum output power of 7.7–10.2 dBm. Meanwhile, in the same frequency range, the PAE_{MAX} and PAE at OP1dB were measured as 1.7–3.1% and 0.5–2.5%, respectively.

Table I summarizes the performance of state-of-the art H-band PAs using compound semiconductors.

IV. Conclusion

An H-band three-stage differential PA with high output power has been proposed. For high output power and PAE, an IDMN using a shunt transmission line was applied to the CC unit cell. The amplifier, fabricated in the 250-nm InP DHBT process, provides a peak small-signal gain of 19.5 dB at 260 GHz and a bandwidth of 25 GHz, with power consumption of 330 mW in the range of 255−280 GHz. The amplifier has a maximum output power of 10.2 dBm at 260 GHz, an OP1dB of 9.5 dBm, and a maximum PAE of 3.1 %. It also exhibits a maximum output power of 7.7–10.2 dBm, an OP1dB of 2.5–9.5 dBm, and a PAE_{MAX} of 1.7–3.1% within the 3 dB bandwidth of the amplifier. In future work, a WR3.4 amplifier module will be tested.

Acknowledgment

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