A 21 Gb/s Arbitrary Binary Sequence Generator for PMCW Radar based on a TSPC Serializer in 22 nm FDSOI

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***Abstract* — This work presents an arbitrarily programmable pseudo-random binary sequence (PRBS) generator for phase-modulated continuous-wave (PMCW) radar transmitters. It incorporates a mixed-signal architecture with a digitally implemented shift register connected to a novel serializer architecture based on true single-phase-clock (TSPC) flip-flops. Unlike static, non-configurable linear-feedback shift registers (LFSRs), this circuit can generate more complex sequences, like the almost perfect auto-correlation sequence (APAS), that exhibit a better radar performance. The circuit is realized on a 22 nm fully-depleted silicon on insulator (FDSOI) technology and consumes a total chip area of $600 \times 530\,\mu m^2$. On-wafer measurements show a maximum chip rate of 21 Gb/s at a 16.9 mW power consumption. To the best of the authors' knowledge, the proposed circuit marks the first programmable PRBS generator operating at this high chip rate. It paves the way for on-chip generation of complex broadband sequences for millimeter-wave digital MIMO radar systems for consumer or automotive applications.**

***Keywords* — Almost perfect auto-correlation sequences (APAS), fully-depleted silicon on insulator (FDSOI), phase-modulated continuous-wave (PMCW) radar, pseudo-random binary sequence (PRBS) generator, true single-phase-clock (TSPC) flip-flop.**

I. Introduction

There exist numerous potential applications of radar systems, ranging from highly automated driving (HAD) over gesture recognition to data transmission. In this context, the demand for research into innovative radar concepts is an essential part of millimeter-wave (mmWave) circuit and system design. The most commonly used radar waveform is frequency-modulated continuous-wave (FMCW), which exhibits a simple architecture but lacks a modulation to encode communication data [1]. In contrast, phase-modulated continuous-wave (PMCW) radar systems represent a viable alternative, which recently has become an interest of research [2], [3]. The PMCW system's simplified block diagram in Fig. 1 shows that a carrier frequency is modulated using binary phase-shift keying (BPSK) with a pseudo-random binary sequence (PRBS). The radar signal's time of flight can be determined by correlating the down-converted receive signal with the time-shifted PRBS, generating a range bin for each bit of the sequence used. The most significant advantage of PMCW radar is that the binary sequences can easily be used to generate MIMO systems [4], [5], allow data transmission in the form of joint radar-communication (RadCom) systems [6], or share the radio frequency (RF) bandwidth with other radar systems utilizing code-division multiple access (CDMA). Also, compared to FMCW systems, no high-linear frequency synthesizer is needed, and the tuning range of the local oscillator decreases.

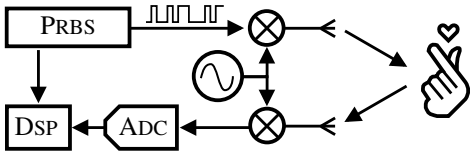


Fig. 1. Simplified block diagram of a PMCW radar system.

Existing PMCW radar systems utilize the frequency band around 79 GHz [3]. However, bandwidth limitations reduce the achievable range resolution $\Delta R = c_0/(2R_C)$, as the PRBS's chip rate R_C equals half the modulated RF bandwidth. The range resolution can be significantly increased at higher frequencies with greater available bandwidth, like the D- or Y-Band. Additionally, the transceiver modules become much smaller, so several can be integrated into one chip. The challenging design of integrated circuits at these frequencies requires state-of-the-art semiconductor technologies. An appropriate option is 22 nm fully-depleted silicon on insulator (FDSOI), which can be used to build high-speed digital circuits as well as competitive mmWave building blocks [7].

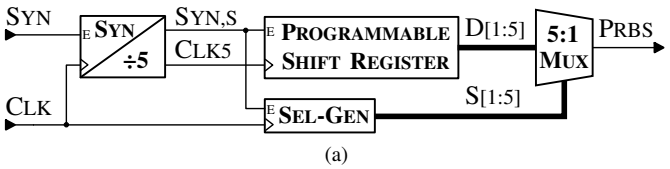
An essential component of PMCW radar transmitters is the PRBS generator, which can be realized through two different approaches. One of them is based on linear-feedback shift registers (LFSRs), which are very efficient regarding chip area and power consumption. By specific feedback and logical connection of the flip-flops (FFs) outputs, this architecture can generate m-sequences whose sequence length $L_C = 2^N - 1$ is at maximum compared to N, the number of flip-flops used [8]. One implementation of this topology is presented in [9] and is well-suited to be used in PMCW radars.

However, other sequences, like the almost perfect auto-correlation sequence (APAS) [10] or the zero correlation zone (ZCZ) sequence [11], outperform the m-sequence in terms of low sidelobes and robustness to Doppler shifts [12], [13]. Nevertheless, circuit-level generation of these sequences requires a different, more complicated mixed-signal hardware approach, where the desired PRBS is stored in a digitally implemented circuit. Existing publications rely on an all-digital variant of this circuitry [3], which is not applicable at

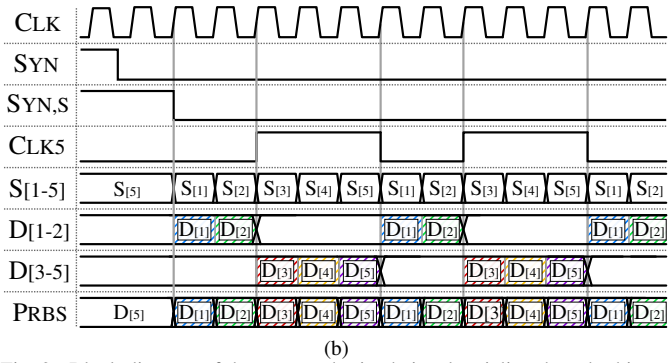
the targeted chip rates above 10 Gb/s. Instead, this paper proposes a mixed-signal, high-speed circuitry with a low power consumption and maximum sequence flexibility to be used in an ultra-wide bandwidth PMCW gesture recognition radar.

II. System and Timing Description

Figure 2 shows the block diagram of the programmable binary sequence generator and the timing relations of its most important signals. The circuit has two input signals, the clock signal CLK which determines the system's chip rate R_C and the SYN signal, responsible for the synchronization. The most important building block is the digitally implemented programmable shift register, which stores the desired PRBS. It has five parallel outputs D[1-5], of which the first two change on the rising edge and the others at the falling edge of each digital clock CLK5. The synchronized falling edge of SYN starts the shift register. Its outputs are connected to a serializer consisting of a multiplexer and a select signal generator. The latter creates the select signal S[1-5], only one of which is a logic high at a time, which connects the respective data lines D[1-5] to the system's PRBS output. The clock division and synchronization are performed in the input circuitry represented by the left building block in Fig. 2a. The division by five, resulting in a 5:1 serializer architecture, is chosen, as it proves to be a good compromise between the complexity of the RF building blocks and the resulting digital clock frequency. Apart from the shown high-speed in- and outputs, the circuit provides a digital interface for programming the desired sequence and its length, which is not shown.



(a)

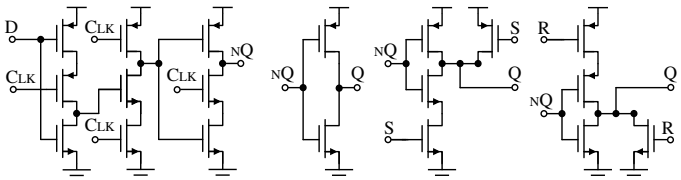


(b)

Fig. 2. Block diagram of the proposed mixed-signal serializer-based arbitrary binary sequence generator in (a) and its timing diagram in (b).

III. Circuit Realization

The circuit is implemented on a 22 nm FDSOI technology, and solely super-low-threshold-voltage (SLVT) transistors are used as they incorporate the maximum timing performance. It has been shown that this technology is excellent for implementing true single-phase-clock (TSPC) FFs [9], whose core circuit is shown in Fig. 3a. Its output signal NQ is connected to the circuits in Fig. 3b to 3d to form a common, settable, and resettable FF, respectively. TSPC FFs belong to the dynamic topology and combine low power consumption and time delay, making them an ideal choice for the desired application.



(a) (b) (c) (d)

Fig. 3. Core circuit of a TSPC FF, which is connected to (b)-(d) to generate a common, settable, and resettable D-FF.

Figure 4 presents the used building blocks' hardware implementation, where an external connection is marked by a rectangle and an internal by a circle. The input circuit is shown in Fig. 4a, which generates the digital clock, synchronizes the SYN signal, and also contains an inverter-based input buffer for the clock. The clock divider is realized through digital standard cells connected in a custom layout, and the TSPC-FFs described above synchronize its in- and outputs. These FFs are also the critical component in the select signal generator in Fig. 4b. It is implemented as a ring oscillator that is synchronously started by the SYN,S signal. Together with the three-stage inverter-based multiplexer pictured in Fig. 4c, they form the serializer. To the best of the authors' knowledge, this architecture has not yet been reported in the literature. The data input for the serializer is generated in the digitally implemented, programmable shift register shown in Fig. 4d. As it is clocked at one-fifth of the PRBS's chip rate, there are five parallel lanes that can be programmed freely with the desired sequence. Variable feedback allows the sequence length to be configured individually, with a maximum adjustable length of 1024. The serializer's output is connected to an inverter buffer, which increases its drive strength to measure the circuit.

The micrograph in Fig. 5 shows the breakout circuit with a chip size of $600 \times 530\,\mu m^2$ and illustrates the ratio between the digital part and the custom-built RF part with a size of $180 \times 120\,\mu m^2$ and $55 \times 22\,\mu m^2$, respectively. The circuit contains an SPI interface for external programming.

IV. Measurement Results

The circuit is measured using a wafer-prober, whereas an *E9275D* PSG analog signal generator supplies the clock signal, and a *UXR0254A* high-speed oscilloscope captures the circuit's output signal at a sampling rate of 128 GS/s. An *N6705B* power analyzer provides the supply voltage and the synchronization signal and measures the circuit's power consumption.

The measurement results in Fig. 6 show the maximum chip rate R_{Cmax} and the corresponding power consumption

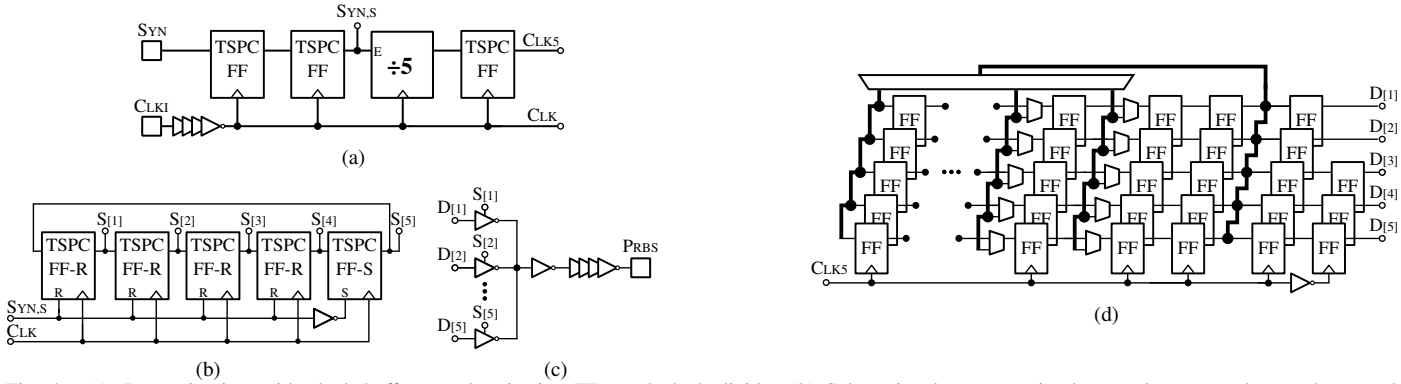


Fig. 4. (a): Input circuitry with clock buffer, synchronization FFs, and clock divider. (b) Select signal generator implemented as a synchronously started TSPC-based ring oscillator used to control the MUX shown in (c). (d) Digitally implemented, programmable parallel shift register with variable feedback to adjust the sequence length.

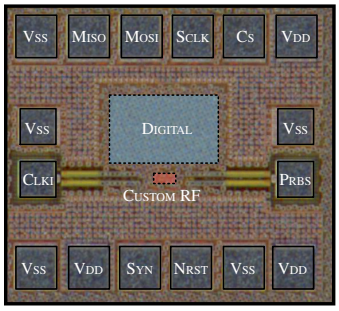


Fig. 5. Micrograph of the realized $600 \times 530\,\mu\text{m}^2$ chip.

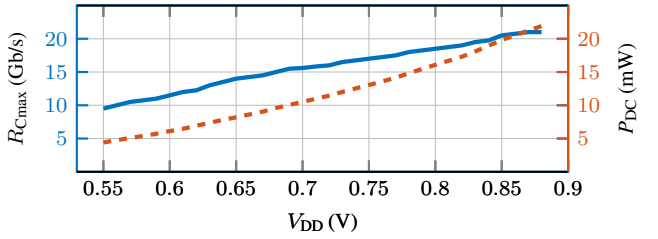
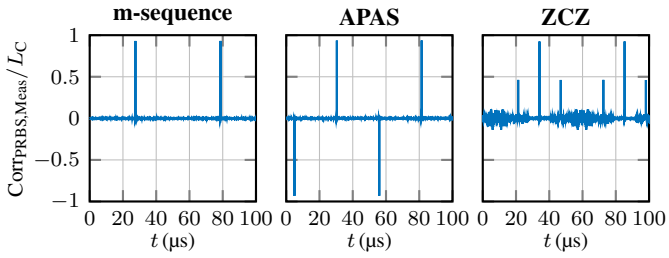


Fig. 6. Measured maximum chip rate $R_{C\max}$ as a function of the supply voltage V_{DD} (solid) and corresponding power consumption (dashed).



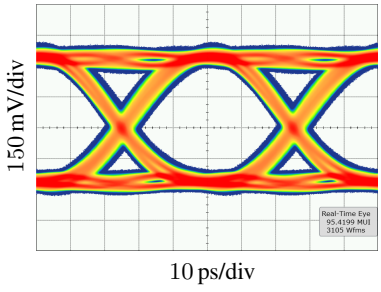


Fig. 7. (a): Correlation of the measured signal with the programmed PRBS using an m-sequence, APAS, and ZCZ at $R_C = 20\,\text{Gb/s}$ and $V_{DD} = 0.88\,\text{V}$. (b): Corresponding measured on-die output eye diagram of the PRBS signal.

as a function of the supply voltage. This value is determined by offline signal processing, where the system's output signal captured at the oscilloscope's maximum data rate is correlated in the time domain with the programmed PRBS interpolated at the same data rate. When the timing constraints in the digital circuit and serializer are met, the correlation signal shows characteristic peaks with a time difference of $\Delta T = R_C L_C$, where L_C equals the programmed sequence length. The supply voltage is swept in $10\,\text{mV}$ steps between $0.55\,\text{V}$, the minimal supply voltage of the digital part, and $0.88\,\text{V}$, the maximally allowed supply voltage of the technology. $R_{C\max}$ is determined at a $0.5\,\text{Gb/s}$ resolution. The circuit's maximum chip rate of $21\,\text{Gb/s}$ can be generated at $V_{DD} = 0.87\,\text{V}$ with a power consumption of $21.2\,\text{mW}$. However, this power includes the output buffer driving the $50\,\Omega$ input of the oscilloscope. In an integrated radar transmitter, the PRBS generator would be connected to a modulator's high-impedance input. Therefore, a second power measurement is performed, where the circuit's output is not probed, resulting in $16.9\,\text{mW}$.

The proposed mixed-signal circuit can be used to generate sequences more complex than a simple m-sequence, unlike classical LFSR-based topologies [9]. For illustration, Fig. 7a pictures the characteristic correlation results of an APAS and a ZCZ next to an m-sequence, which were obtained as described above. The corresponding eye diagram can be seen in Fig. 7b, exhibiting an eye height, peak-to-peak jitter, and RMS jitter of $500\,\text{mV}$, $25\,\text{ps}$, and $2.4\,\text{ps}$, respectively. Both measurements were created at a $20\,\text{Gb/s}$ chip rate and a supply voltage of $0.88\,\text{V}$.

Table 1. State-of-the-art PRBS generators.

		[9]	[15]	[16]	**This work**
Process	–	22 nm CMOS	40 nm CMOS	130 nm SiGe	22 nm CMOS
$\mathbf{f_T}$ / $\mathbf{f_{max}}$	GHz	350/370	260/–	300/500	350/370
$\mathbf{R_{Cmax}}$	Gb/s	33	15	80	21
$\mathbf{L_C}$	–	$2^{11}-1$	$2^{31}-1$	$2^{15}-1$	$\leq 2^{10}$
$\mathbf{V_{DD}}$	V	0.88	1.1	4	0.87
$\mathbf{P_{DC,Core}}$	mW	3.1	8.8	1200	16.9
Area	μm^2	42	3700	$1.38 \cdot 10^6$	22 810
FoM	$^{fJ}/_{Bit}$	8	42	1000	80
Prog. Sequence	–	No	No	No	Yes

V. Conclusion and discussion

In the literature, [14] is the only publication found by the authors presenting an arbitrarily programmable PRBS generator. However, this work was implemented on a field-programmable gate array (FPGA) and only reached a chip rate of 5 Gb/s with unknown power consumption. This makes a comparison of this work to the state of the art difficult. Nevertheless, Table 1 shows a comparison of the presented circuit to recently published LFSR-based PRBS generators, representing the closest topology. It uses the common figure of merit (FoM) as the power consumption divided by the word length times the bit rate in $^{fJ}/_{Bit}$. The increased circuit complexity translates into an increase in chip area and degradation in FoM to $80\,^{fJ}/_{Bit}$. However, it must be emphasized that the compared publications can only generate a single sequence with non-optimal radar performance. This additional degree of freedom justifies an increased area and power consumption.

This work presented the first arbitrarily programmable integrated PRBS generator based on a novel TSPC FF serializer architecture reaching a chip rate of 21 Gb/s. When used in a PMCW radar transmitter, advanced sequences with ideal correlation properties and a good Doppler shift tolerance can be generated, making the resulting system superior to systems using an LFSR for sequence generation.

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