A 56-67 GHz CMOS Phased-Array Transmit Beamformer with 26.2 dB Peak Gain, 15 dBm P_{SAT}, and 20% PAE

Kyung Pil Jung[#1], Joon Hyung Kim[$], Geon Ho Park[#], Chul Soon Park[#]
[#]School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Republic of Korea
[$] School of Electronics Engineering, Kunsan National University, Republic of Korea
[1]kpchung94@kaist.ac.kr

***Abstract*— This paper presents a 60-GHz CMOS phased-array transmit beamformer using analog linearizer in 65-nm process. The beamformer is implemented with input and output (I/O) V_{DD} and ground planes completely separated on chip, and achieves high stability with reverse isolation of > 60 dB. The measured peak gain is 26.2 dB, while 3-dB bandwidth is 56–67 GHz. The linearized beamformer delivers P_{SAT} of 13.6–15 dBm, P_{1dB} of 12–12.8 dBm and PAE_{Max} of 16.8–20% and PAE at P_{1dB} (PAE_{1dB}) of 12.7–15 % in 3-dB bandwidth. Under the 2-tone test, the beamformer provides a linear output power up to 7 dBm satisfying IMD3 of <-30 dBc. In addition, the measured root-mean-square (RMS) gain and phase error of <0.56 dB and <4.8° are yielded during 360° phase shift with 11.25° resolution in 3-dB bandwidth, respectively, while controlling gain range of 18 dB.**

***Keywords*— Analog linearizer, CMOS, P_{1dB}, power-added efficiency (PAE), phased-array transmit beamformer.**

I. Introduction

The unlicensed 60-GHz band based on IEEE 802.11ay is expected to support data rates of up to 100 Gb/s using wideband spectrum [1]. To widen the coverage and capacity, fine beam-scanning technologies using large-scale phased arrays have been developed in 60 GHz [2]-[3]. However, it presents challenges in implementing RF front-ends covering wide bonding channels up to 8.64 GHz. In addition, the large power consumption of several phased elements in transmitter (TX) directly affects the reducing the operating time for mobile applications, so that the Tx must provide the sufficient output power while ensuring the high efficiency. In addition, the unwanted errors during phase and gain control should be low enough for avoiding degradation in both directivity and side lobe level.

This paper presents a 60-GHz CMOS phased-array transmit beamformer. To expand linear output-power-range without phase distortion, the analog amplitude and phase pre-distorter previously discussed in [6] are integrated in the beamformer. In this work, the impedance matching scheme that allows the linearized beamformer to have constant linearity within the frequency band are additionally introduced. In addition, active circuits capable of phase shift and gain control are stably integrated for extensive utilization in phased arrays.

II. Design and Implementation of Beamformer

Fig. 1 shows chip photo of the transmit beamformer channel. The beamformer is designed with a 4-stage fully differential topology and consists of a power amplifier (PA), a driver amplifier (DA), a variable gain amplifier (VGA), and a vector-sum based active phase shifter (VSPS). To avoid

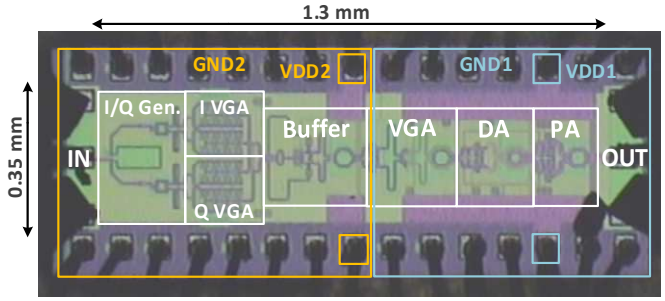


Fig. 1. Chip photo of phased-array transmit beamformer channel in 65-nm CMOS process.

stability degradation due to return current flowing through the integrated ground plane, the input/output (I/O) V_{DD} and ground planes of the beamformer were completely isolated in chip. The beamformer was fabricated using the 1.2-V 65-nm 1P9M CMOS process and the chip core-area is 0.46 mm^2.

Fig. 2 shows the schematic of the proposed phased-array transmit beamformer and summarizes design parameters. The VSPS was integrated by reconstructing the phase shifter proposed in [7] into a 5-bit digital logic to simplify the I/Q G_m-cell control. The impedance-invariant phase shift with 11.25° resolution is realized by individually controlling gain of the I/Q VGA and output signal is amplified by C_{gd}-neutralized the current-reuse buffer without an additional power consumption. The simulated DC power consumption of phase shifter is only 10.8 mW. In addition, the 1-stage cascode differential complementary-G_m compensated (CGC) VGA is proposed for high gain-control range with low phase variation. The two differential pairs of transistors M_3 and M_4 are cross-connected in source. The amount of currents flowing through them were varied by adjusting the gate control bias V_{VGA} of M_4, while the M_3 gate bias is fixed to V_{DD}. Thus, the gain is adjusted linearly in proportion to G_{m3}-G_{m4} controlled by V_{VGA}. The proposed CGC structure has the control range up to 18 dB with low phase variation, while the conventional current steering VGA has gain control of only up to ~3 dB. The VGA DC power consumption is 15.8 mW.

The 2-stage common source differential PA and DA with analog linearizer are integrated in the output stage. The linearizer is implemented by an amplitude (M_A) and a phase linearizer (M_P) act as variable resistor and capacitor respectively, is connected in parallel to the differential PA input. The details of the linearizer are described in [6]. Fig. 3 shows the proposed matching networks of inter and output

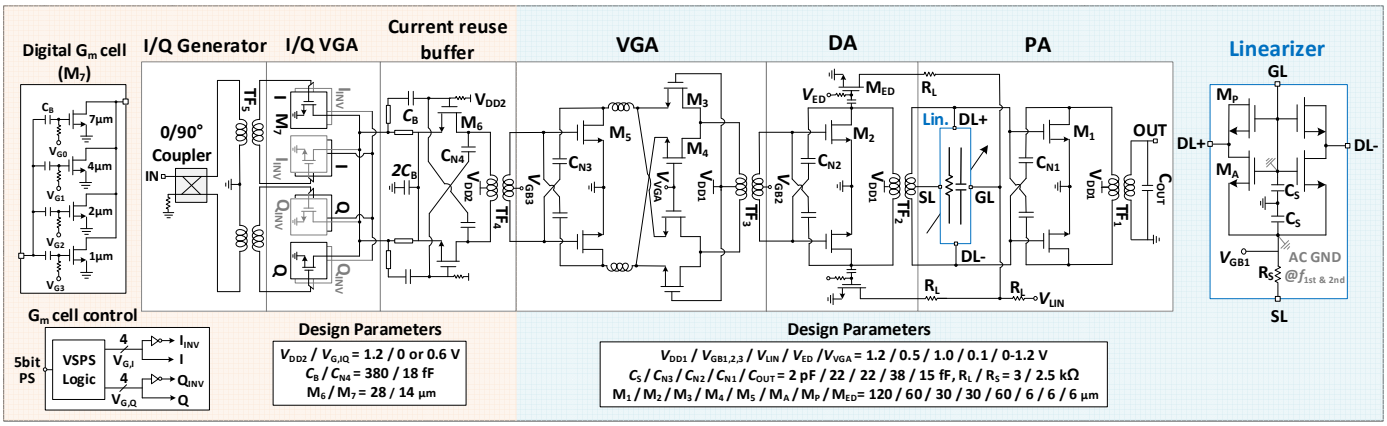
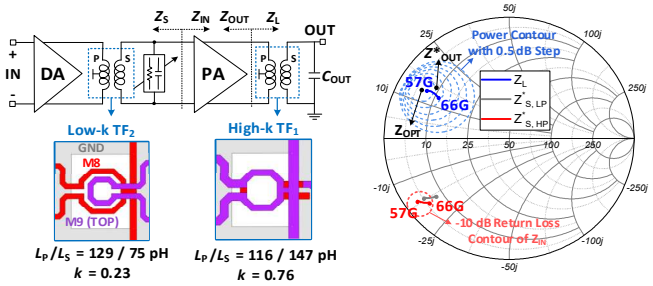
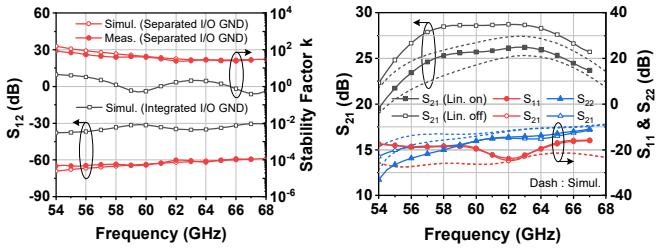


Fig. 2. Schematic of proposed phased-array transmit beamformer.



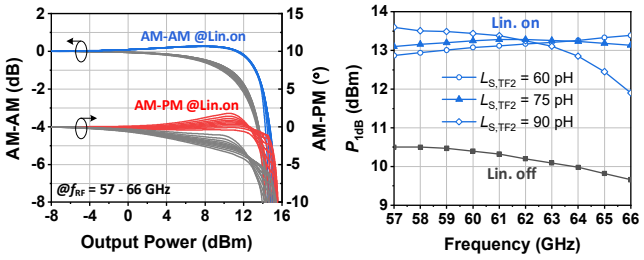
(a) (b)

Fig. 3. (a) Inter-stage and output matching networks, (b) simulated Z-smith chart with load and source impedance of PA within frequency band.



(a) (b)

Fig. 5. Simulated and measured (a) reverse isolation (S_{12}) and stability factor k, (b) S-parameter.



(a) (b)

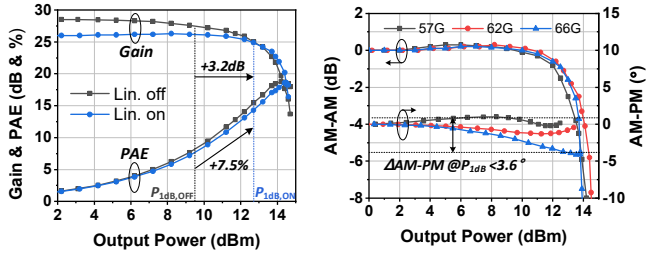
Fig. 4. Simulated (a) AM-AM and AM-PM distortion at from 57 to 66 GHz, (b) P_{1dB} of 2-stage PA versus frequency.

stage along with the simulated Z-smith chart of the PA from 57 to 66 GHz. To closely match the load impedance (Z_L) to both the power-optimum impedance (Z_{OPT}) and the output conjugate impedance (Z^*_{OUT}), the output matching network is implemented by a transformer (TF_1) with high coupling coefficient (k) and an output capacitor (C_{OUT}) of 15 fF as shown in Fig. 3 (a). The load impedance Z_L is matched to the Z_{OPT} at the lower frequency resulting in output power drop of ~1 dB at the higher frequency, while the output matching loss of only -1.2 dB. To achieve the constant linearity of the linearized beamformer within frequency while boosting AM-AM linearization, a low-k transformer (TF_2) implemented with a diameter offset between primary inductor (L_P) and secondary inductor (L_S) is used as an inter-stage matching network as shown in Fig. 3 (a). As the linearizer impedance is changed as a function of the input power by the envelope detector (ED), the source impedance including the linearizer and the TF_2 has the higher Q factor at the high-power region ($Z_{S,HP}$) compared to the low-power region ($Z_{S,LP}$). As shown in Fig. 3 (b), $Z^*_{S,HP}$ is well matched to Z_{IN} within the frequency band, so that the PA delivers maximally linearized gain at high power range. Consequently, as shown in Fig. 4 (a), the linearized PA has good AM-AM and AM-PM distortion of <2° up to extended P_{1dB} within the frequency range. As shown in Fig. 4 (b), the trend of the P_{1dB} enhancement versus frequency is mainly affected by the value of L_S of TF_2 under the similar k. When the L_S is 75 pH, the linearized PA gives nearly constant P_{1dB} of 13.1–13.3 dBm in the frequency range from 57 to 66 GHz. The DC quiescent power consumption of the PA and the DA are 51.6 mW and 25.6 mW, respectively.

III. Measurement

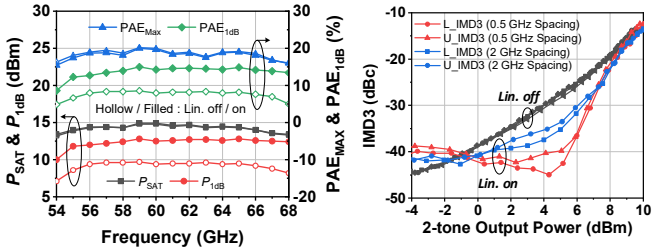
Under the on-wafer probing test, the S-parameters of the IC were measured using the Keysight E8361A vector network analyzer. Fig. 5 (a) shows the measured and simulated reverse isolation (S_{12}). In the simulation, the separated I/O ground structure provides significant improvement of the reverse isolation and stability compared to using the integrated I/O ground, the measured beamformer has the reverse isolation of below -60 dB with the sufficiently high stability factor. As shown in Fig. 5 (b), the measured peak gain of the linearized beamformer is 26.2 dB including a linearizer loss of 2.5 dB, while 3-dB bandwidth is from 56 to 67 GHz.

Fig. 6 (a) exhibits the measured gain and PAE at 62 GHz. The beamformer with the linearizer on delivers P_{1dB} of 12.7 dBm and PAE at P_{1dB} (PAE_{1dB}) of 14.6 %. Although an



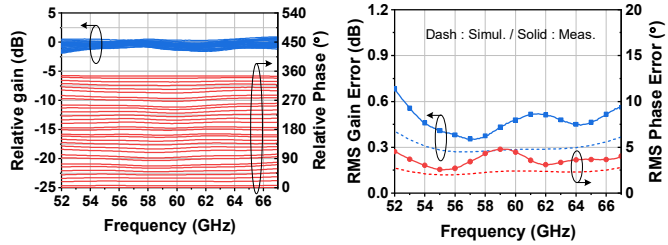
(a) (b)

Fig. 6. Measured (a) gain and PAE versus output power at 62 GHz, (b) AM-AM and AM-PM distortion when linearizer on at 57, 62, and 66 GHz.



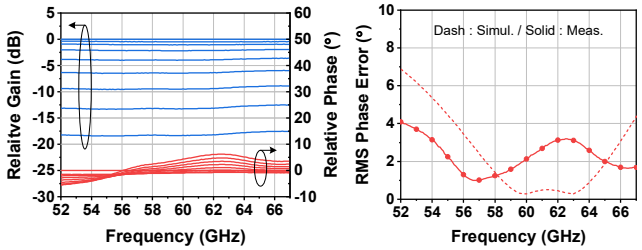
(a) (b)

Fig. 7. Measured (a) P_{SAT}, P_{1dB}, PAE_{Max} and PAE at P_{1dB} (PAE_{1dB}), (b) IMD3 versus 2-tone output power at 2-tone spacing of 0.5 and 2 GHz.



(a) (b)

Fig. 8. Measured (a) relative gain and phase during phase shift, (b) RMS gain and phase error versus frequency.



(a) (b)

Fig. 9. Measured (a) relative gain and phase error during gain control, (b) RMS phase error versus frequency.

insertion loss of 2.5 dB occurred, the proposed linearizer improves the $P_{1\,dB}$ by 3.2 dB. This P_{1dB} enhancement leads to 7.5% improvement in PAE at P_{1dB}. The beamformer when linearizer on also achieves the P_{SAT} of 14.6 dBm and the PAE_{max} of 18.6%. Fig. 6 (b) indicates that the measured AM-AM and AM-PM are good within frequency band, resulting in the AM-PM distortion up to P_{1dB} of below 3.6°. Fig. 7 (a) shows the plots of measured P_{SAT}, P_{1dB}, PAE_{Max} and PAE_{1dB} versus frequency. Within the 3-dB bandwidth, P_{SAT}, P_{1dB}, PAE_{Max} and PAE_{1dB} were observed as 13.6–15 dBm, 12–12.8 dBm, 16.8–20%, and 12.7–15%, respectively. In addition, as shown in Fig. 7 (b), under the 2-tone test at center frequency of 62 GHz, the linearized beamformer achieved a linear output power of up to 7 dBm while satisfying IMD3 below -30 dBc.

Fig. 8 shows the measured relative gain and phase versus frequency during 360° phase shift with 11.25° resolution. As shown in Fig. 8 (b), the measured RMS gain and phase error of are <0.56 dB and <4.8°, respectively for the 3-dB bandwidth. Fig. 9 (a) shows the measured relative gain and phase during gain control. As shown in Fig. 9 (a) and (b), the RMS phase error of <3.2° are achieved in the 3-dB bandwidth, while controlling gain range of 18 dB. Table 1 summarizes the performance comparison of 60-GHz phased-array transmit beamformers.

IV. Conclusion

This study investigated a 60-GHz phased-array transmit beamformer with analog linearizer in the 65-nm CMOS process. The measured peak gain is 26.2 dB, while 3-dB bandwidth is 56–67 GHz. The linearized beamformer delivers P_{SAT} of 13.6–15 dBm, P_{1dB} of 12–12.8 dBm and PAE_{Max} of 16.8–20% and PAE_{1dB} of 12.7–15% in the 3-dB bandwidth. Consequently, the linearized beamformer not only has sufficient gain, but also provides good linearity and high PAE over a wide bandwidth, so it is expected to provide sufficiently linear output power in mm-wave phased arrays without external control.

Table 1. Comparison of 60-GHz phased-array transmit beamformers

Reference	TMTT'16 [2]	TMTT'19 [4]	TMTT'20 [5]	This work
Process	0.18μm SiGe	65 nm CMOS	45 nm SOI	65 nm CMOS
Freq. @BW_{3dB} [GHz]	56 – 67	57 – 66	57.5 – 65.5	56 – 67
P_{SAT} / ele. [dBm]	2.5 – 3*	N/A	5 – 11.5*	13.6 – 15
P_{1dB} / ele. [dBm]	-0.5 – 0*	7.1**	3 – 10.5*	12 – 12.8
PAE / ele. [%]	N/A	8.7*/** @P_{1dB}	13.2–17.4*@Max 10.8–14.5*@P_{1dB}	16.8–20 @Max 12.7–15 @P_{1dB}
Peak gain / ele. [dB]	18	8.8***	22	26.2
Phase resolution [°]	11.25	22.5	11.25	11.25
RMS gain error [dB]	<1.2	<0.53	<0.7	<0.56
RMS phase error [°]	<12	<8.8	<5	<4.8
Gain control [dB]	10*	7	14	18

*Estimated from figure, **At single frequency, ***Including dividing loss

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