A *Ka*-band 35-dBm $P_{0.1dB}$ Low-loss Monolithic SPDT Switch using Anti-series Diode Connection

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***Abstract*—In this paper, a *Ka*-band monolithic high-power low-loss single-port double-throw (SPDT) switch is proposed using a GaAs PIN process. The switch is designed using an innovative anti-series diode connection to significantly enhance 1-dB compression point, since the turned-on issue of the diode can be effectively resolved under high-power driving. Between 25 and 30 GHz, the proposed SPDT switch features a measured insertion loss of within 1.2 dB, an isolation of higher than 20 dB, and an input 0.1-dB compression point ($P_{0.1dB}$) of higher than 35 dBm. As compared with prior art, this work is suitable for high-power applications in microwave and millimeter-wave bands due to its superior performance and compact chip size.**

***Keywords*— Diode, GaAs, microwave and millimeter-wave (mm-wave), PIN, switch.**

I. Introduction

Demand of the modern wireless communications, a high-power low-loss high-isolation switch is crucial for the transceiver, especially for millimeter-wave (mm-wave) 5G mobile applications [1]. Several circuit topologies, including traveling-wave [2]-[5], series-shunt [6]-[8], absorptive-type [9], quarter-wavelength (1/λ) shunt [10], and impedance transformation [11], can be employed to achieve low insertion loss and high isolation up to mm-wave bands. The active device can be based on high electron-mobility transistors (HEMTs) [2], [4]-[6], [11], CMOS [3], and PIN diodes [7]-[10]. A single-pole double-throw (SPDT) switch is usually connected among the antenna, transmitter, and receiver, for the time-division multiplexing, and the 1-dB or 0.1-dB compression point (P_{1dB} or $P_{0.1dB}$) of the switch is a key specification for the transmitting operation since it limits the maximum RF output power. The input P_{1dB} of the GaAs HEMT or CMOS switch is usually lower than 30 dBm due to the device characteristic, and the SiGe- or GaAs-based PIN-diode switch is also limited due to the rectified dc current with RF power driving.

To further enhance the P_{1dB}, a switch using stacked transistors with sub-design rule channel length in floated p-wells was proposed in [13], but the maximum power handling would be limited by an abrupt output drop. A switch using stacked FETs with feed-forward capacitors in floated well was proposed to achieve a power handling of up to 33 dBm at 1.8 GHz [14], and it would be limited for mm-wave design due to the parasitic effect. The P_{1dB} can also be enhanced using a negative body bias technique [3], but the maximum power handling is still limited. In this paper, a *Ka*-band monolithic SPDT switch is proposed using a GaAs PIN diode process. With an innovative anti-series diode connection, the proposed switch features a measured insertion loss of within 1.2 dB, an isolation of higher than 20 dB, and an input $P_{0.1dB}$ of higher than 35 dBm between 25 and 30 GHz. As compared with the previously reported monolithic PIN-diode switches, the power handling of the switch can be significantly enhanced due to the cancellation of the rectified dc current under high-power driving.

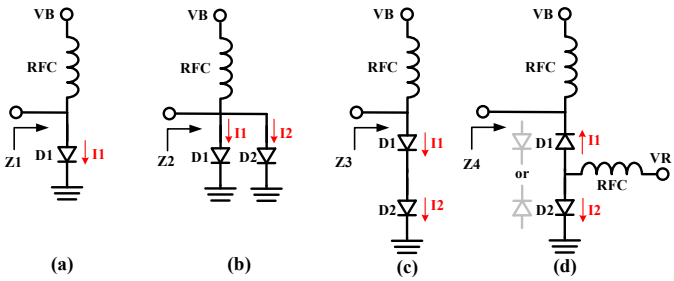

Fig. 1. Circuit topologies for the load impedance of the switch, (a) single diode, (b) parallel diodes, (c) series diodes, and (d) proposed anti-series diodes.

II. Circuit Design and Analysis

The GaAs PIN diode process provided by WIN Semiconductors Corporation, Taiwan is adopted for designing the proposed SPDT switch. When the diode size is 10×10 μm^2, the turn-on resistance and turn-off capacitance are 3 Ω and 25 fF, respectively. In general, the diode can be a series or shunt element for the switch design. The diode is turned on and off with and without dc bias current, respectively. For the series connection, the insertion loss increases with increasing the turn-on resistance, and the isolation decreases with increasing the turn-off capacitance. For the shunt connection, the insertion loss increases with increasing the turn-off capacitance, and the isolation decreases with increasing the turn-on resistance.

Under the small-signal condition, the input impedance of the diode would be very high when the diode is turned off without dc bias current. With increasing the RF input power, the input impedance decreases due to the rectification, therefore, the insertion loss (or P_{1dB}) and isolation are both degraded under the high-power condition. Four circuit topologies, including single diode, parallel diodes, series diodes, and proposed anti-series diodes, are shown in Fig. 1 for the load impedance of the switch, where I1 and I2 are the rectified dc currents of D1 and D2, respectively. When the dc bias VB is 0 V, the simulated input impedance for the single diode significantly decreases with increasing the RF power up to 30 dBm. The turn-on effect of the diode can be suppressed with reversed dc bias (VB = -6 V). The simulated results of the parallel diodes and series

diodes are similar to the single diode, and the simulated impedances of the parallel diodes and the series diodes are lower and higher than the single diode, respectively, under the high power condition. The simulated impedances of the proposed anti-series diodes still decreases with increasing the RF power and the simulated results is similar to the series diodes. To further suppress the turn-on effect, the diodes D1 and D2 can be biased both in the revised dc condition, such as VB = 0 V and VR = -6 V. The rectified dc currents I1 and I2 would be suppressed by decreasing VR to negative voltage, and therefore, the D1 and D2 could be kept in the turn-off condition under the high-power driving. Also, the high input impedance can be maintained well with a floating VR due to the cancellation of I1 and I2.

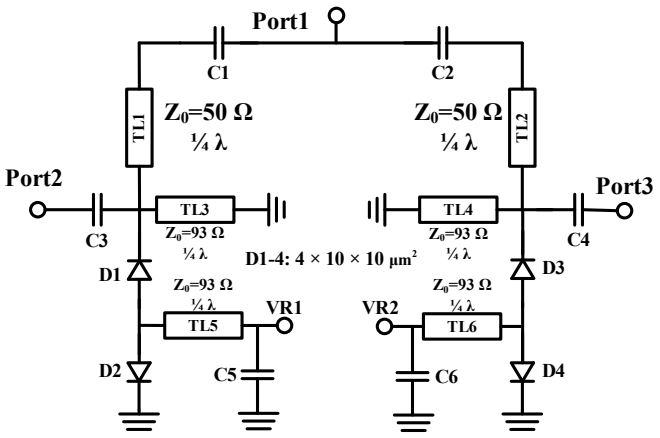

Fig. 2. Schematic of the proposed SPDT switch.

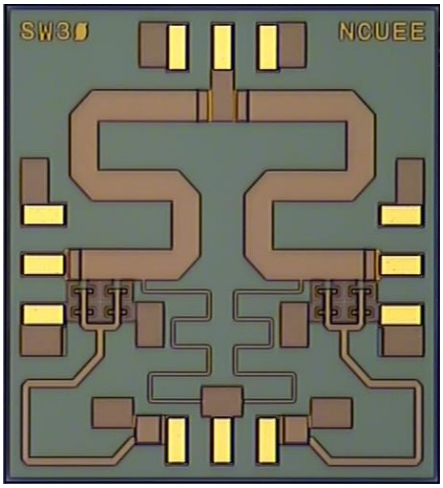

Fig. 3. Chip photo of the proposed SPDT switch with a chip size of 1×1 mm^2.

The schematic of the proposed SPDT switch is shown in Fig. 2, and the circuit is based on the quarter-wavelength shunt topology with the anti-series diodes D1-4 to minimize the insertion loss. The quarter-wavelength transmission lines TL1-2 perform the impedance transformation, and the transmission lines TL3-6 perform the RF choke and the dc bias networks. The capacitors C1-C4 and C5-6 perform the dc block and RF bypass networks, respectively. When the path between Port1 and Port2 (Port3) is turned on (off), the dc biases VR1 and VR2 are low state (≦0 V) and high state (>1.3 V), and the diodes D1-2 and D3-4 are off- and on-state, respectively. The simulated input P_{1dB} and third-order intercept point (IP3) versus low-state voltage VR of the proposed SPDT switch at 28 GHz can be further enhanced by lowering the low-state voltage VR1 (or VR2). The chip photo of the proposed SPDT switch is shown Fig. 3 with a chip size of 1×1mm^2.

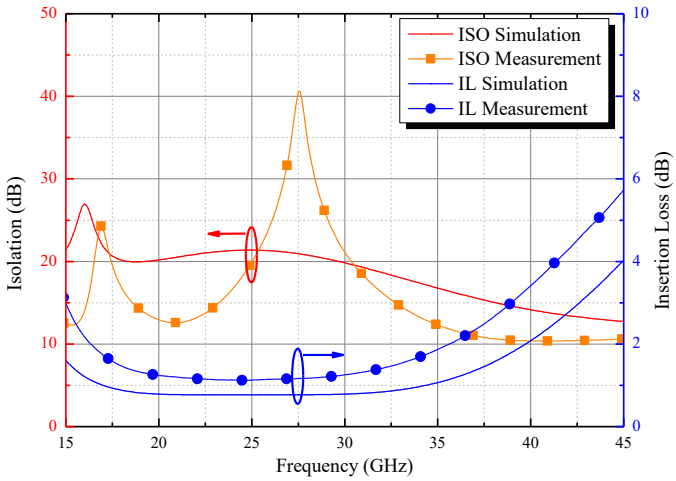

Fig. 4. Simulated and measured insertion losses (IL) and isolations (ISO) of the proposed SPDT switch.

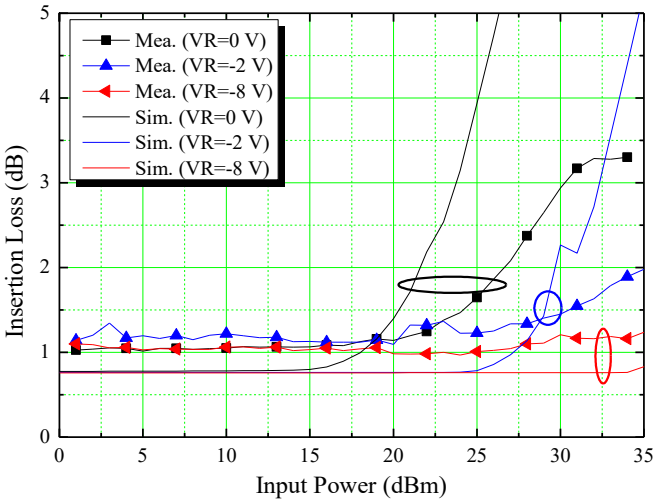

Fig. 5. Simulated and measured insertion losses versus input power with various VR at 28 GHz for the proposed SPDT switch.

III. Experimental Results and Discussions

The proposed SPDT switch is characterized via on-wafer probing. For the small-signal *S*-parameters measurement, a Keysight N5227A vector network analyzer is adopted. When VR1 and VR2 are 0 and 1.3 V, respectively, the simulated and measured insertion losses between Port1 and Port 2, and isolations between Port1 and Port 3 are plotted in Fig. 4. From 25 to 30 GHz, the proposed SPDT switch features a measured insertion loss of within 1.2 dB and a measured isolation of better than 20 dB. When VR1 is varying from 0 to -8 V, the measured insertion loss and isolation are almost the same. For

Table 1. Performance comparison of the prior art and this work

Ref.	Process	Topology	Freq. (GHz)	IL (dB)	ISO (dB)	P_{1dB} (dBm)	P_{DC} (mW)	Chip size (mm^2)
[4]	InGaAs mHEMT	SPST Traveling-wave	DC – 30	<5.5	>32	>20	0	0.85 × 1.8
[5]	InGaAs PIN	Traveling-wave	25 – 95	<3.2	>40	N/A	144	1.05 × 0.58
[6]	GaN HEMT	Series-shunt	2 – 18	< 2.1	> 30	33		1.5 × 1.1
[7]	SiGe PIN	Series-shunt	38 – 67	2.0	>23	22	7.5	0.066
[8]	GaAs PIN	Series-shunt	0.01 – 70	<2	20@38 GHz	25.5@2 GHz		0.74 × 0.57
[9]	GaN PIN	Absorptive-type	20 – 27	< 3.4	> 12.5	N/A	90	2.57 × 1.03
[10]	SiGe PIN	1/4λ shunt	73 – 113	<2	19 – 22	>24	10.2	0.14
[14]	65nm CMOS	Series-shunt	25 – 30	RX: 0.74-1.16	>16.4	5.2	0	0.14 × 0.31
				TX: 0.96-1.1	>27.0	31.8		
[15]	GaN HEMT	1/4λ shunt	110 – 170	1.8-2.3	29-38	>33		1.5 × 1
[16]	InGaAs mHEMT	1/4λ shunt	50 – 75	1-1.6	31.6-32.8	>22	0	1.5 × 1
This work	GaAs PIN	1/4λ TL with anti-series PIN	25 – 30	<1.2	> 20	>35 ($P_{0.1dB}$)	91.7	1 × 1

the large-signal characterization, a Keysight E8257D signal generator with a power amplifier is adopted as the input signal, and an Agilent E4448A spectrum analyzer with an attenuator is employed for receiving the output power. The simulated and measured insertion losses versus input power with various VR at 28 GHz are plotted in Fig. 5 for the proposed SPDT switch. When VR is 0 V, the measured insertion loss increases with increasing the input power, and the measured P_{1dB} is 28 dBm. The measured P_{1dB} is significantly enhanced by decreasing VR to -8V, and it is higher than 35 dBm. Due to the limitation of the power amplifier, the power handling is only evaluated up to 35 dBm. The simulated and measured input P_{1dB} versus frequency is plotted in Fig. 6 with various VR, and the measured $P_{0.1dB}$ is higher than 35 dBm over the frequency. Due to the limitation of the instruments, the linearity of the proposed SPDT cannot be measured. The performance comparison of the prior art and this work is summarized in Table 1, and all the works are designed using compound semiconductors. This work has the lowest insertion loss, highest P_{1dB} among all the reported microwave and mm-wave monolithic switches.

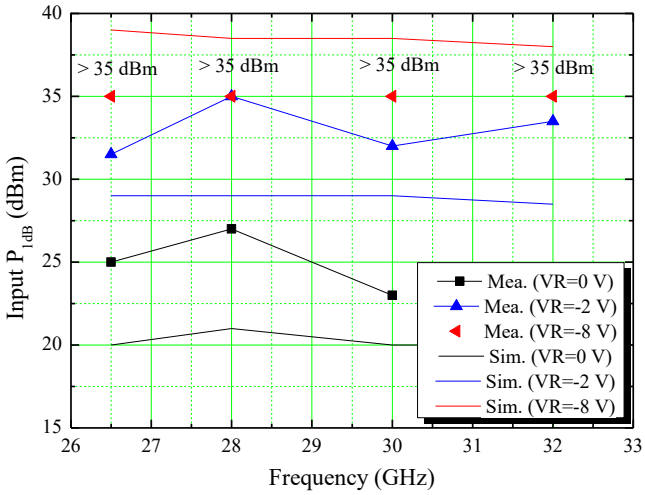

Fig. 6. Simulated and measured input P_{1dB} versus frequency with various VR.

IV. Conclusion

A *Ka*-band monolithic high-power low-loss SPDT switch is successfully developed using a GaAs PIN diode process. Based on the proposed anti-series diode connection, the P_{1dB} of the switch is significantly enhanced since the rectified dc current of the diodes can be suppressed under the high RF power driving. The proposed circuit topology is also suitable for other semiconductor processes. The demonstrated SPDT switch has the lowest insertion loss and the highest P_{1dB} as compared with prior art, and it can be applied for some advanced transceiver applications due to its superior performance.

Acknowledgment

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