A Multi-stage 19.2-dBm, 30.4%-PAE D-band Power Amplifier in a 250-nm InP HBT Process

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***Abstract* — In this paper, we demonstrate results for 2 and 3-stage power amplifiers in 250-nm InP HBT technology that offer the highest combination of peak power added efficiency (PAE) and saturated output power (Psat) published to date. The 2- and 3-stage designs achieve a PAE of 30.4% and 23.8% and Psat of 19.2 dBm and 17.1 dBm, respectively. Both designs offer high gain with up to 14.7 dB of gain for the 2-stage and 18.5 dB for the 3-stage as well as compact area for high-density applications such as phased arrays.**

***Keywords* — power amplifier, millimeter-wave, d-band, high efficiency, Indium Phosphide, HBT**

I. Introduction

Communication and radar systems in upper millimeter-wave frequencies such as D-band (110-170 GHz) have gain much attention due to higher data rates and finer resolution imaging. In D-band arrays, high power components are packed into 1 mm spacing which introduces thermal management issues and space constraints. To alleviate thermal loading and spacing requirements, there is a need to have compact high-efficiency power amplifiers (PAs). However, as we transition to higher frequency bands, device scaling becomes an important issue as more stages are needed to provided high overall gain in the PA. Highly scaled devices with high f_{max} provide more gain, at the cost of lower breakdown voltages, and thus output power. The InP technology offers f_{max}/f_T of 600/350 GHz at a bias current of 2 mA/um with about 15 dBm output power and close to 50 Ohm loadline impedance[1].

In previous work, a recent SiGe PA utilizing a 4-way slotline combiner with cascode cells achieved a PAE of 12.4% with 18.1 dBm output power and 30.7 dB small signal gain at 161 GHz [2]. Other GaN PAs have also shown high output powers of 23.5 dBm with 7.9% peak PAE and 10.5dB gain at 136 GHz [3]. In comparison, InP PAs have shown the highest PAE numbers for frequencies above 100 GHz. An InP class-B PA using sub-quarter-wavelength balun power combining achieved a power-added efficiency (PAE) of 32% for a single stage PA with a saturated output power (P_{sat}) of 15.3 dBm at 130 GHz [3]. Another InP PA achieved 20.5% PAE with 20.5 dBm Psat at 140 GHz[4]. The prior high PAE work in InP was limited to single stages and lower output power.

In this paper, we present the design of a multi-stage InP power amplifier with a PAE of 30.4% and output power of 19.2 dBm at 135GHz. In section II, we shown the design and stability of a common base degenerated power cell. The design of the coupled-line balun and interstage matching network is shown in section III. Measurement results are shown in section IV.

II. Device Cell Design

The 250-nm InP HBT technology from Teledyne Scientific offers f_{max}/f_T of 600/350 GHz at a bias current of 2 mA/um. The typical breakdown voltage is about 4.5-5V with typical Vce of 2.5V. The maximum current is about 3mA/um of emitter length such that a 4-finger 6-um HBT has an Imax of 72 mA. Passives in this technology are designed using 4 gold metal layers with a top metal layer thickness of 3um.

As in earlier work, a common base (CB) device is used over a common emitter (CE) device due to higher maximum available gain (MAG) at 140 GHz. CB has a MAG of 11.9 dB compared to the CE with a MAG of 5.7 dB at 140 GHz [5].

The MAG for a CB cell with finite base capacitance is also shown on the plot with about 10 dB Gmax. The finite base capacitance provides tradeoff between linearity and gain, with lower base capacitances providing higher OP1dB, but lower gain. This relationship is shown on Fig.2 for different values of base capacitances. If the base capacitance is lossless, the PAE should be invariant assuming harmonic tuning is not significant. For improved OP1dB, the output stage uses a 240fF on each side for a total of 480fF on the base.

Prior work was limited to high PAE results in single stage designs. One issue with multistage designs is the well-known thermal runaway in InP HBT devices. As the device heats up, the Vbe decreases thereby increasing collector current and potentially leading to thermal instability. To prevent thermal runaway issues, a base ballast resistor of 50 Ohms is added, which also acts as a broadband choke for bias stabilization and low-frequency RF stability. In the previous plot, the base connection to the supply was an ideal choke, but by adding a series resistance, the impedance presented to the base has a finite real component for small base capacitance. Consequently, the base network is lossy which reduces the overall gain and PAE. One solution introduces a series quarterwave line with bypass caps so that the quarterwave line

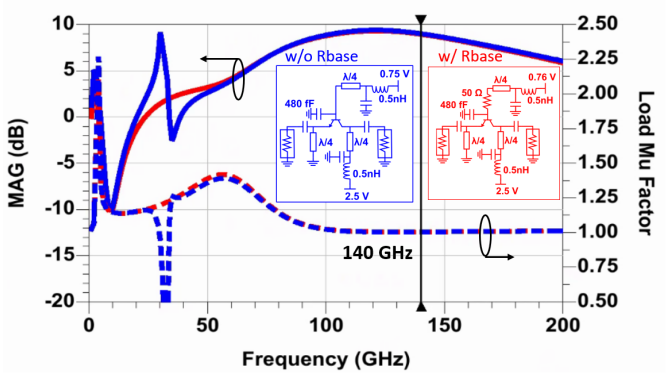

Fig. 1. Comparison of MAG and stability for base network with (red) and without (blue) 50 Ohm series base resistance for a single 4x6um device.

in series with the base resistance presents an open circuit. A comparison of the load μ-factor and Gmax with and without the base resistance for a single 4x6um device is shown on Fig. 1 for the quarterwave line at the base. An equivalent 0.5 nH inductance is added to simulate the equivalent inductance of DC probes. In this case, the base resistance does not impact the Gmax at 140GHz, but eliminates potential stability issues at 32 GHz. Although we estimate the probe inductance to be 0.5 nH, the actual impedance could vary widely and so the base resistance helps isolate DC probe impedance variations.

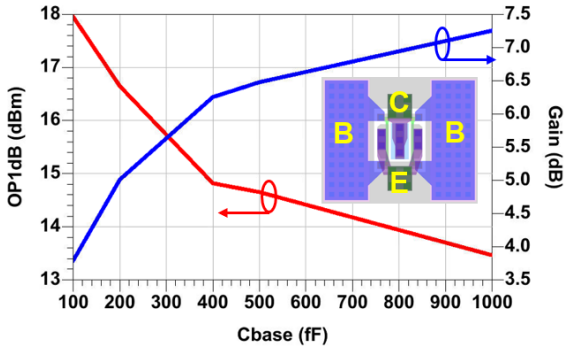

Fig. 2. Tradeoff between OP1dB and Gain for different values of total base capacitance for 4x6um device biased at 0.2 mA/um.

III. Circuit Design

The full circuit schematic for the 2-stage design is shown on Fig. 4 and for the 3-stage design on Fig. 5. This design uses identical sized CB cells for both the first and second stage. The first stage uses a smaller value of 600fF base capacitance to get higher gain. A short section (80x100um^2) coupled line balun is used for output and input matching. The DC collector supply is fed through the center of the coupled line. An open stub is added to one side to tune the amplitude and phase balance with less than 2° phase imbalance and 1-dB amplitude imbalance. The input balun includes about 600fF shunt capacitance for input matching. The output balun presents 0.75 dB of insertion loss while the input balun presents about 1.1 dB of insertion. The output balun is designed to match to 8+j22.8 Ω according to the loadpull simulation on Fig. 3. Since the collector current is a function of input drive due to class-AB biasing, the base voltage drops for higher power. The base is biased at 0.83V and compresses to 0.75 V at higher power. An interstage matching network consisting of a series 240-fF capacitor for matching and DC decoupling and shunt quarterwave lines to present open circuits at the design frequency. The insertion loss of the interstage matching network is about 1.2 dB.

Since the interstage matching and devices are identical, a 3-stage design is simply just cascading another 4x6 um device with an interstage network. To improve the PAE, the voltages for each stage are slightly lowered for each driver stage.

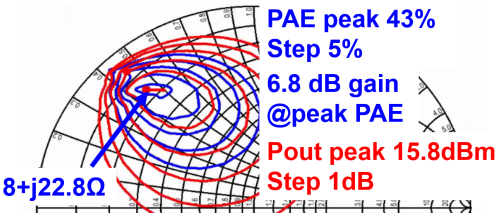

Fig. 3. Loadpull of 4x6um device with 50 Ohm base resistance at 140 GHz. The base is biased at 0.83V and compresses to 0.75V.

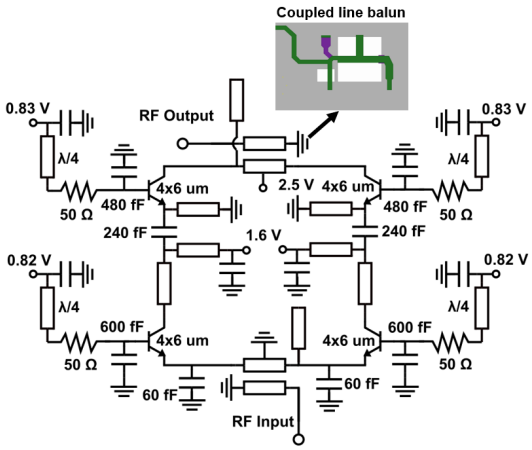

Fig. 4. Circuit schematic for 2-stage PA.

IV. Measurements

S-parameter and power measurements were collected using the PNAX (N5247A) driving VDI 110-170GHz frequency extenders and probed with 100um pitch D-band waveguide probes with about 2dB loss each. VNA calibration was done using CS-15 calibration substrate from GGB. A driver WR6.5 amplifier from VDI was also used to drive the PA. Both the 2-stage and 3-stage chip photographs are shown on Fig. 6.

S-parameter results for the 2-stage and 3-stage are shown on Fig. 7. The S21 peak is 18.5 dB at 141 GHz for the 3-stage and 14.7 dB at 142 GHz for the 2-stage. Overall, there is good agreement with simulations although the S21 for the three stage is slightly lower than simulations.

Large signal measurements for both 2 and 3-stage PA designs are shown on figures 8 and 9. A comparison between simulations (solid) at 140 GHz and measurements (dotted) at

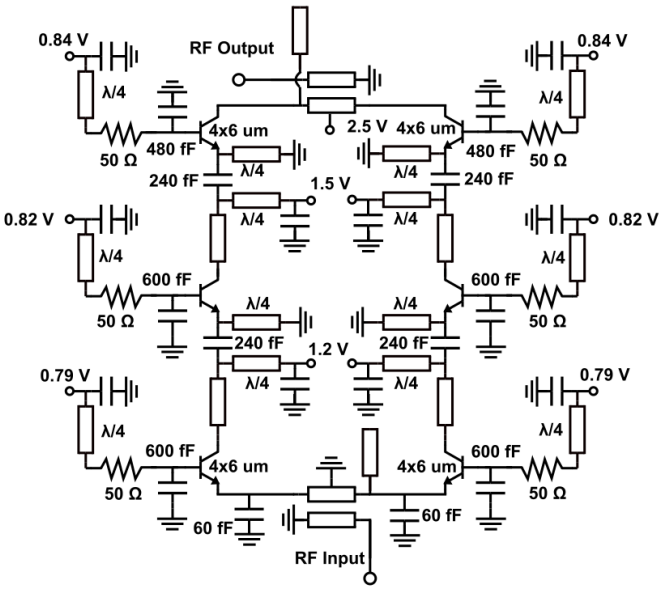

Fig. 5. Circuit schematic for 3-stage PA.

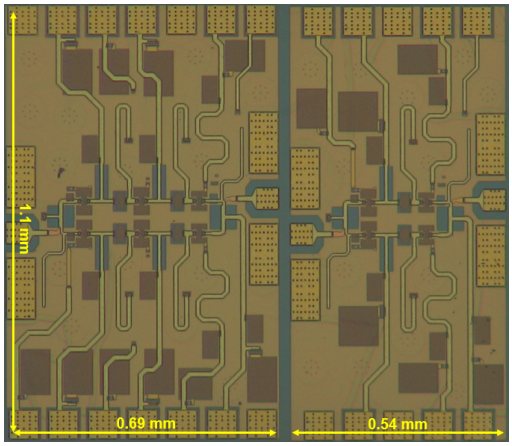

Fig. 6. Chip photo of 3-stage (left) and 2-stage (right) power amplifiers with 1.1x0.69mm^2 and 1.1x0.54mm^2 total chip area respectively.

135 GHz for the 2-stage PA on Fig. 8 shows good agreement. The driver collector voltage was optimized for best PAE in both simulation and measurement and was set at 1.6 V in measurements compared to 2.2 V in simulations. The output stage collector voltages for both measurement and simulations were 2.5 V. The peak PAE achieved was 30.4% at 17.8 dBm output power and Psat of 19.2 dBm at 135 GHz. Two other chips were also measured and are also shown on the same figure. The large signal measurements for the 3-stage on Fig. 9 show some discrepancy between gain and PAE in simulation and measurement. This is explained by large gain variations shown in the 2-stage in Fig. 8 which is compounded in the 3-stage design. Increased thermal coupling between devices with the added stage further reduces the gain for each stage. Measured peak PAE at 135 GHz was 23.8% at 16 dBm with a Psat of 17.1 dBm. Simulations indicate closer to 29% PAE and 19.5 dBm Psat. Multiple measurements from the 2-stage design indicates variability between the chips which could impact the PAE and Psat compared to simulations. The collector voltage for the 1st and 2nd stages were set to 1.2 V and 1.5 V, respectively, in measurement for maximum PAE compared to 1.6 V and 2.2 V in simulation.

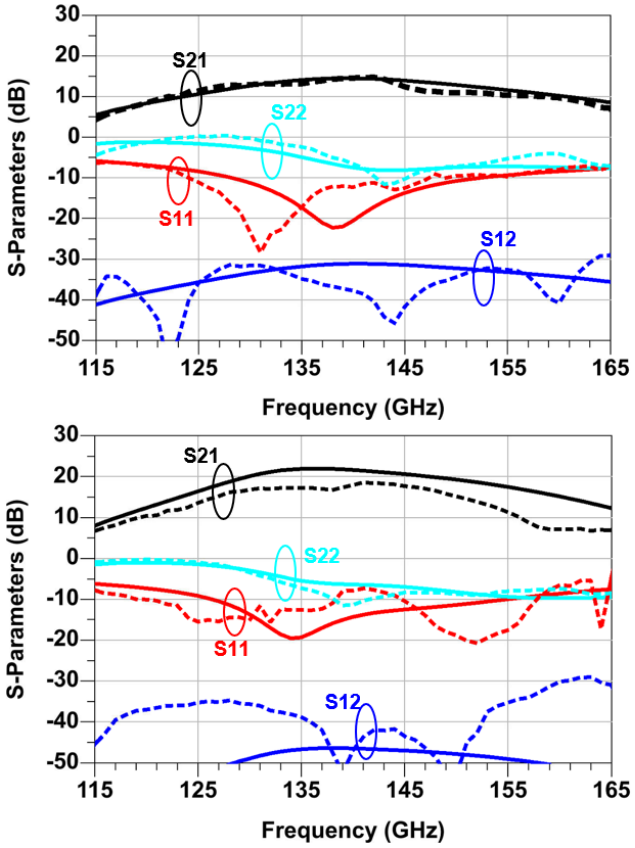

Fig. 7. S-parameter measurement (dotted) and simulation (solid) of 2-stage (top) and 3-stage (bottom) PAs. Measurements were biased according to the circuit diagrams. Simulations were biased similarly but with Vc1 = 2.2V for the 2-stage and Vc1=1.5V, Vc2 = 2.2V for the 3-stage.

V. Conclusion

We present a 2 and 3-stage InP power amplifier design at 135 GHz, making use of compact and low loss coupled line baluns. The 2-stage PA achieves up to 30.4% peak PAE and 19.2 dBm saturated output power. The 3-stage PA achieves up to 23.8% peak PAE and 17.1 dBm saturated output power.

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References

[1] J. F. Buckwalter, M. J. W. Rodwell, K. Ning, A. Ahmed, A. Arias-Purdue, J. Chien, E. O'Malley, and E. Lam, "Prospects for high-efficiency silicon and lll-v power amplifiers and transmitters in 100-300 ghz bands," in *2021 IEEE Custom Integrated Circuits Conference (CICC)*, 2021, pp. 1–7.

Table 1. Comparison between State-of-the-Art D-band PAs

Reference	Technology	Frequency (GHz)	Gain (dB)	Psat (dBm)	PAE (%)	Chip Area (mm^2)
This Work	250nm InP HBT	135	14	19.2	30.4	0.59
			17.3	17.1	23.8	0.76
[6]	250nm InP HBT	118-148	7	15.3	32	0.2
[7]	250nm InP HBT	150-175	31.7	23.1-24	13.1-15.7	1.26
[4]	250nm InP HBT	125-150	12.3-15.9	18.9-20.5	14.3-20.8	0.69
[5]	250nm InP HBT	140	8.4	17.3	22.5	0.44 / 0.1*
[8]	250nm InP HBT	110-128	8.5	17.6	32.7	0.024
[9]	45nm CMOS SOI	140	24	17.5	13.4	0.43*
[10]	55nm SiGe	135	24	17.6	17.5	0.18
			22.4	19.3	13	0.76
[2]	130nm SiGe	161	30.7	18.1	12.4	0.42

*core area

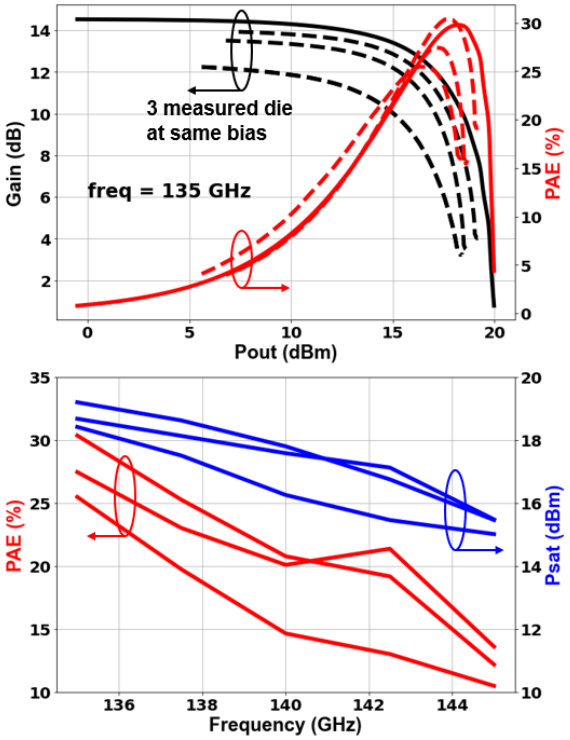

Fig. 8. Large signal measurements (dotted) and simulation (solid) of 2-stage PA from 135 to 145 GHz. Each dotted line is for 3 different die.

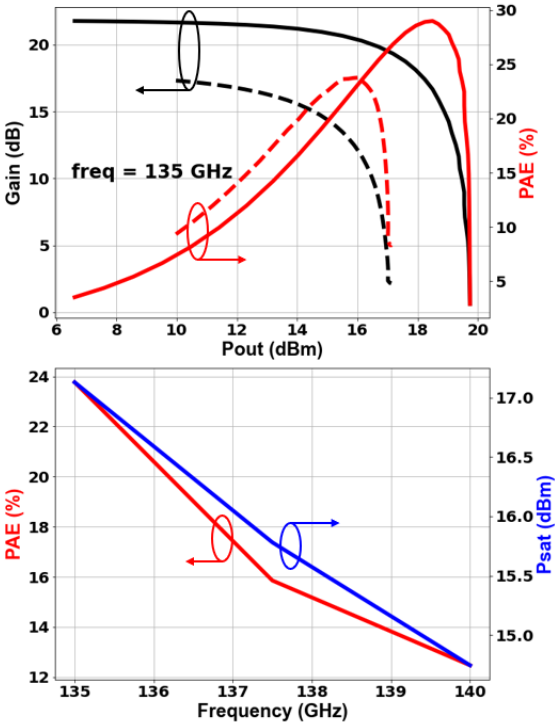

Fig. 9. Large signal measurements (dotted) and simulation (solid) of 3-stage PA from 135 to 140 GHz

[2] X. Li, W. Chen, S. Li, Y. Wang, F. Huang, X. Yi, R. Han, and Z. Feng, "A High-Efficiency 142–182-GHz SiGe BiCMOS Power Amplifier With Broadband Slotline-Based Power Combining Technique," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 2, pp. 371–384, 2022.

[3] E. Lam, A. Arias-Purdue, E. O'Malley, and J. F. Buckwalter, "A 23.5-dBm, 7.9%-PAE Pseudo-differential Power Amplifier at 136 GHz in 40-nm GaN," in *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*, 2022, pp. 119–122.

[4] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter, and M. J. W. Rodwell, "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 492–495.

[5] E. Lam, K. Ning, A. Ahmed, M. Rodwell, and J. Buckwalter, "A 2-stage, 140-GHz Class-B Power Amplifier Achieving 22.5% PAE at 17.3 dBm in a 250-nm InP HBT Technology," in *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, 2022, pp. 448–451.

[6] K. Ning, Y. Fang, M. Rodwell, and J. Buckwalter, "A 130-GHz Power Amplifier in a 250-nm InP Process with 32% PAE," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2020, pp. 1–4.

[7] Z. Griffith, M. Urteaga, P. Rowell, and L. Tran, "A 150–175 GHz 30-dB S21 G-band Power Amplifier with 0.25-W Pout and 15.7% PAE in a 250-nm InP HBT Technology," in *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, 2022, pp. 444–447.

[8] J. S.-C. Chien and J. F. Buckwalter, "A Compact, 114-GHz, High-efficiency Power Amplifier in a 250-nm InP HBT Process," in *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, 2022, pp. 452–455.

[9] S. Li and G. M. Rebeiz, "A 130-151 GHz 8-Way Power Amplifier with 16.8-17.5 dBm Psat and 11.7-13.4% PAE Using CMOS 45nm RFSOI," in *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2021, pp. 115–118.

[10] I. Petricli, D. Riccardi, and A. Mazzanti, "D-Band SiGe BiCMOS Power Amplifier With 16.8dBm PdB and 17.1% PAE Enhanced by Current-Clamping in Multiple Common-Base Stages," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 3, pp. 288–291, 2021.