A High Efficiency Q-band MMIC GaN Power Amplifier for Space Applications

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***Abstract*—This paper describes the design methodology and the On-Wafer (OW) measurement results of three Q-band four-stage MMIC High Power Amplifiers (HPA-LB, HPA-MB & HPA-HB) operating respectively in the 35-41GHz, 37-42GHz and 38-43GHz bandwidths. A Single-Ended HPA topology is considered (SE-HPA). These demonstrators are fabricated in 150-nm HEMT Gallium Nitride on Silicon Carbide technology (AlGaN/GaN on 70µm SiC substrate) for space applications, and thus considering space de-ratings. The main aim of this realization was the achievement of high output power associated with a high Power Added Efficiency. To obtain a good compromise between output power and PAE, a multi harmonic tuning approach of load and source impedances has been applied.**

The On-Wafer measured power results under pulsed wave signal of all SE-HPAs demonstrate a maximum output power (P_{OUT}) higher than 8W (39dBm) with 25% Power Added Efficiency (PAE) and more than 28dB of insertion gain (G_I) in the overall frequency band of the interest.

***Keywords*—Q-band, HPA, Harmonics tuning, MMIC, GaN, High PAE, space applications.**

I. INTRODUCTION

The next generation of satellite communication systems at Q and V bands increases the need for highly performing and increasingly miniaturized MMIC technology. Active antenna systems, especially for air and space borne applications, which consider the integrated microwave power amplifier as one of the most critical RF component. These systems require both, in transmission mode, a high level of output power associated with a high level of PAE and a low dissipated power with a high integration. In fact, these requirements considerably reduce the size, mass, and cost of several modules, in particular the cooling systems necessary for operation, which are very heavy and high-energy-consuming.

The AlGaN/GaN on SiC technology is one of the best candidates addressing both sufficient output power thanks to its high power density and high power added efficiency at high frequencies due to its intrinsic performances. Moreover, it enables high temperature operation due to its high maximum junction temperature capability and ensures good heat dissipation due to its substrate proprieties resulting in the right reliability level.

In this context the main aim of this study was the demonstration of the performances of GaN HPAs in terms of PAE and P_{OUT} across the entire 35 – 43 GHz frequency band and to validate the ability to fulfill the environmental requirements in terms of reducing power consumption and heat dissipation considering the space de-ratings.

II. 0.15-µM GAN TECHNOLOGY

MMICs were designed an fabricated in a 0.15-µm GaN AlGaN/GaN HEMT technology qualified on a 4-inch-diameter 70-µm SiC substrate for drain-source bias up to 25 V. The 0.15-µm technology targets the development of multistage high power high efficiency high gain amplifiers, high power switches, limiters, high power detectors, and robust low noise amplifiers up to 43 GHz.

A comprehensive design kit including electro-thermal hot and cold transistor models, passive devices models, auto layout capabilities and all elements concerning reliability is available.

Recommended Operating Ratings (ROR) and Absolute Maximum Ratings (AMR) have been defined from the resulted qualification tests data.

Table 1 summarizes the main features of the used 0.15-µm GaN technology:

Table 1. Main characteristics of the used 0.15-µm GaN technology.

Parameter	Typical value
Cut-off frequency (f_t)	> 35 GHz
RF power density	3.5 W/mm
I_{DS++}@V_D=7 V, V_G=2 V	1.4 A/mm
G_{mMax}@ V_D=7 V, V_G=Vgmmax	390 mS/mm
$V_{pinch-off}$ # Vg100@ V_D=7 V, Ids=Idss/100	-3.2 V
Drain-source voltage bias	10 to 25 V

III. CIRCUIT DESIGN

The design goals for this amplifier cover 8 W saturated output power at ambient temperature associated with PAE better than 25% and 25-dB linear insertion gain. All these requirements must be achieved in the instantaneous frequency bandwidths from 35-41 GHz, 37-42 GHz and 38-43 GHz.

For optimal amplifier sizing, the first step is to undertake multi-harmonic load-pull and source-pull simulations using the electro-thermal large signal transistor model at both 25-°C and 85-°C backside temperatures. These simulations allow selecting the optimal transistor periphery, unit transistor topology, and appropriate biasing point. Thereby the number of necessary power stages to ensure a requested power gain is defined and the maximum theoretical achievable PAE level in the overall frequency band is calculated as defined by the Bode

and Fano theorems [1-2]. The application methodology of these theorems is given in [3].

A class AB Single-Ended HPA architecture has been selected. The main advantages of the SE-HPA are the lower losses of the output and input matching networks, which allow improve the insertion gain, the output power, and the PAE levels.

All HPAs are based on four stages. The first stage consists in 2 unit FET cells, the second stage is based on 4 unit FET cells. The third one is composed from 8 unit FET cells and finally the power stage includes 16 unit FET cells which are twofold combined. An equivalent electrical model of the bond-wire connection at input and output pads is included in the design.

Table 2 shows for all HPAs the selected transistor topologies and the gate-width periphery for each stage.

Table 2. Transistor topologies and the gate-width periphery for each stage.

		LB-HPA	MB-HPA	HB-HPA
Stg. 1	Unit cell [µm]	4x60	4x60	4x50
	Number of devices	2	2	2
Stg. 2	Unit cell [µm]	4x60	4x60	4x50
	Number of devices	4	4	4
Stg. 3	Unit cell [µm]	4x55	4x55	4x50
	Number of devices	8	8	8
Stg. 4	Unit cell [µm]	4x75	4x75	4x60
	Number of devices	16	16	16

The biasing point (V_D=19 V, I_D=~30 mA/mm) have been identified as interesting, it allows to reach a better trade-offs between PAE, linear gain and power consumption for the considered transistors.

Table 3 summarizes the simulated values of the input impedances (Z_{IN}) at the gate-port and the load admittances (Y_L) at the drain-port for 4x60 µm, at highest the interest fundamental frequency (f_0 =43 GHz).

Table 3. Simulated optimal input impedances, optimal load admittances & associated main performances of one 4x60µm transistor unit at f_0=43GHz

Parameter	Unit	Value
Z_{IN}	$R_{IN} + jX_{IN}$ [Ω]	3.3 – j 2.5
Y_L	$G_L + jB_L$ [S]	0.0091 – j 0.0317
PAE	[%]	34
P_{OUT}	[dBm]	27.20
Small G_I	[dB]	10.20

The source and load terminations at second harmonic are chosen with respect of the criterion defined in [4]. This criterion accurately defines the 2nd harmonic termination to avoid the critical zone of loads in terms of PAE performances.

Fig. 1 illustrates the simulated optimum PAE performances of the 4x60µm transistor versus the phase variation of the 2nd harmonic reflection coefficients and of the source (Γ_S) and load (Γ_L) terminations, for a fundamental frequency of 43GHz.

The critical source termination area extends from 150° to 220°. The optimum of PAE is located at 230°. This phase location is very risky because it is very close to the critical load termination area. The safe load termination area is considered between -120° and 150° on the smith chart.

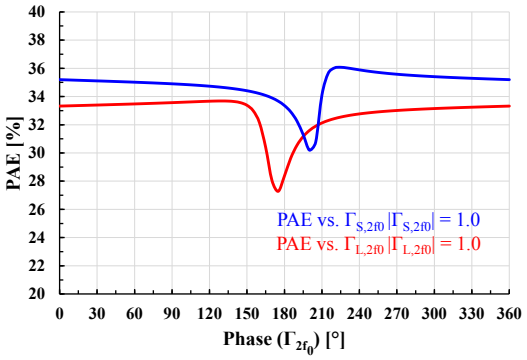

Fig. 1. Influence of the source and load impedances at 2nd harmonic (Γ_S & Γ_L), on simulated PAE at f_0=43GHz of one 4x60µm transistor unit.

The critical load termination area extends from 150° to 230°. The optimum of PAE is located at 140°. This phase location is very close to the critical source termination area. The safe load termination area is considered between -120° and 130° on the smith chart.

All matching networks have been optimized in order to present respectively the optimal load impedances at both fundamental and 2nd harmonic frequencies at the drain-ports of all transistors and the optimal source impedances at fundamental and 2nd harmonic frequencies at the gate-ports of all transistors. In addition, the matching network circuits have low losses and adequate phase variation profiles allow achieving a good AM/AM and AM/PM flattens.

The used 0.15-µm GaN transistors typically have a very high gain at low frequencies which can potentially lead to stability issue. Furthermore, operating the transistors near their maximum potential can also generate in-band and extra-band stability issue. Odd mode cancellation resistors have been inserted at gate ports of transistors.

Stability criterion has been meticulously analysed. Multi-biasing, multi-mode linear and non-linear simulations at different temperatures were done using K-factor and 2-tone probe techniques (odd and even modes).

To ensure the RF specifications, a linear Monte-Carlo analysis and a nonlinear corner analysis including all process and environment variations have been simulated.

IV. Experimental Results

All small and large signal on-wafer characterizations were performed using pulse wave mode (25 µs/10%) at ambient room temperature. The measurements of the HPA-LB, HPA-MB and HPA-HB are done at V_{DS0}=19 V and I_{DS0}=240 mA (~30 mA/mm).

The calibration de-embeds the measurements to the input/ output MMIC RF pads reference plan. The MMIC backside temperature was not controlled by any form of thermal management. All circuits seem to be stable at small and large signal. A particular attention has been paid to the DC-probes decoupling circuit to avoid BF oscillations.

Fig. 2 shows a photograph of the fabricated MMIC LB-HPA, the other amplifiers have identical architecture.

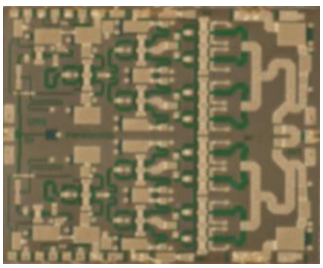

Fig. 2. Fabricated 3.6x2.9mm^2 Q-band LB-HPA MMIC cell unit

A. *Small signal on -wafer measurements*

The On-Wafer measured S-parameters of HPA-LB, HPA-MB and HPA-HB circuits were performed using a standard VNA.

1) *HPA-LB*

Fig. 3 illustrates the measured on-wafer S-parameters of the HPA-LB. The small signal gain (S21) is higher than 28 dB, the input return loss (S11) is better than -8 dB and the output return loss (S22) is better than -8 dB in the overall frequency bandwidth 35-41 GHz.

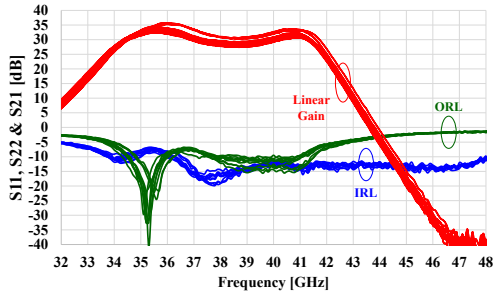

Fig. 3. On-wafer measured HPA-LB S-parameters.

2) *HPA-MB*

The measured S-parameters of HPA-MB is shown in Fig. 4. The S21 is higher than 28 dB, the S11 is better than -7 dB and the S22 is better than -8 dB in the overall bandwidth 37-42 GHz.

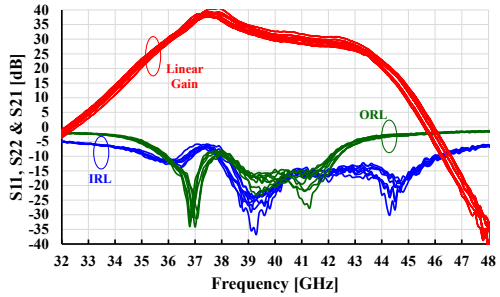

Fig. 4. On-wafer measured HPA-MB S-parameters.

3) *HPA-HB*

Fig. 5 shows the measured on-wafer S-parameters of the HPA-HB. The small signal gain (S21) is more than 28 dB, the input return loss (S11) is better than -9 dB and the output return loss (S22) is better than -12 dB in the overall frequency bandwidth 38-43 GHz.

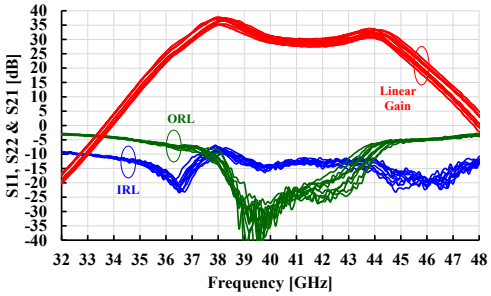

Fig. 5. On-wafer measured HPA-HB S-parameters.

B. *Large signal on-wafer measurements*

The MMIC HPAs were also characterized using pulsed large-signal at ambient room temperature. All measurements have been performed at V_{DS0}=19 V &I_{DS0}=240 mA (~30 mA/mm).

1) *HPA-LB*

The main measured power parameters results of 10 HPA-LB MMIC samples between 35 and 41 GHz are given in Fig. 6.

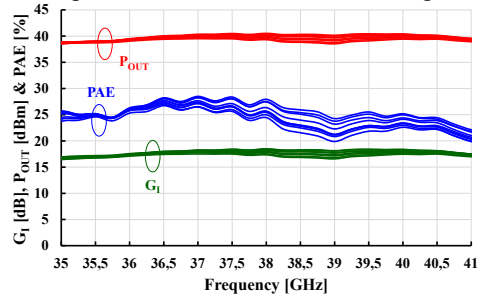

Fig. 6. Measured HPA-LB PAE, P_{OUT} and corresponding G_I over frequency band for V_{DS0}=19 V and I_{DS0}=240 mA at 22 dBm input power.

It can be seen that the HPA-LB shows 21-28% PAE in the entire 6 GHz bandwidth with a P_{OUT} above 8 W and an associated G_I better than 17.5 dB. The PAE peak is measured at 37 GHz with 28 %.

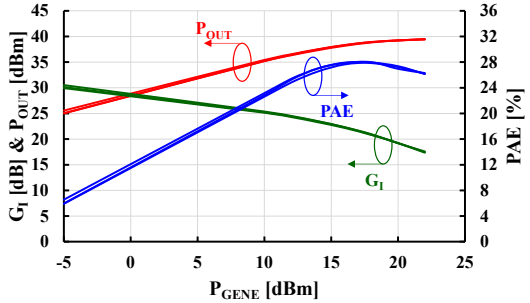

Fig. 7. Measured HPA-LB PAE, output power and insertion gain versus input power for V_{DS0}=19 V and I_{DS0}=240 mA at f_0= 36 GHz.

Very good reproducibility is achieved over 5 MMIC samples randomly selected as shown on Fig. 7 with power measurements at 36 GHz versus P_{IN}.

2) *HPA-MB*

The main measured power parameters results of 10 HPA-MB MMIC samples between 37 and 42 GHz are given in Fig. 8.

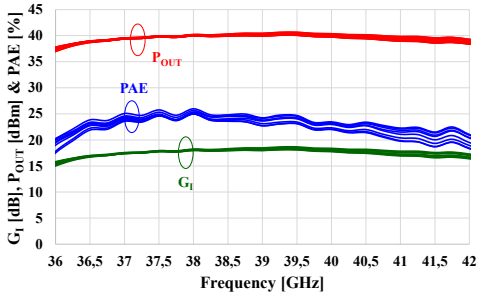

Fig. 8. Measured HPA-MB PAE, P_{OUT} and corresponding G_I over frequency band for V_{DS0}=19 V and I_{DS0}=240 mA at 22 dBm input power.

The HPA-MB shows also 20-26% PAE in the entire 5 GHz bandwidth with a P_{OUT} above 8 W and an associated G_I better than 18 dB. The PAE peak is measured at 38 GHz with 26% and a P_{OUT} of 10 W.

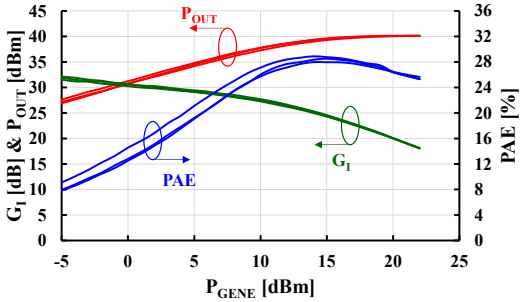

Fig. 9. Measured HPA-MB PAE, output power and insertion gain versus input power for V_{DS0}=19 V and I_{DS0}=240 mA at f_0= 38 GHz.

The main power results (5 MMIC samples) at 38GHz are given in Fig. 9.

3) HPA-HB

The main measured power parameters results of 10 HPA-HB MMIC samples between 38 and 43 GHz are given in Fig.10.

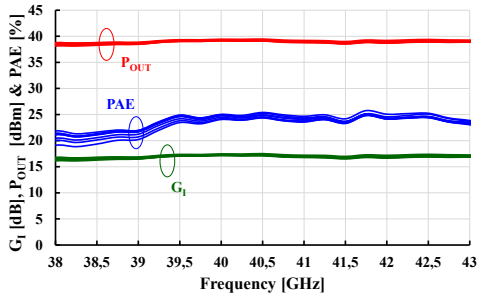

Fig. 10. Measured HPA-HB PAE, P_{OUT} and corresponding G_I over frequency band for V_{DS0}=19 V and I_{DS0}=240 mA at 22 dBm input power.

The HPA-HB provides more than 20% PAE in the entire 5 GHz bandwidth with a P_{OUT} above 8 W and an associated G_I better than 16.5 dB. The PAE peak is measured at 40.5 GHz with 26% and a P_{OUT} of 9 W.

Fig. 11 shows the main measured power curves of 5 MMIC samples at 41GHz versus P_{IN}.

In Table 4 the performances of the presented amplifiers (HPA-LB, HPA-MB and HPA-HB) are compared with the previous published GaN HEMT Q-band HPAs.

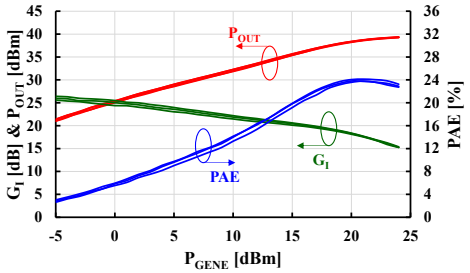

Fig. 11. Measured HPA-HB PAE, output power and insertion gain versus input power for V_{DS0}=19 V and I_{DS0}=240 mA at f_0= 41 GHz.

Table 4. Comparison with other Q-band HPA using GaN HEMT technology.

Ref.	Process Techno.	Test Signal	Freq. [GHz]	VD [V]	P_{OUT} [W]	G_I [dB]	PAE [%]	Area [mm²]
[5]	0.10µm GaN/Si	CW	37.5-42.5	8	2	25	30	11
[6]	0.10µm GaN/SiC	CW	35-40	15	0.25	9	18	2.3
[7]	0.15µm GaN/Si	/	37.5-42.5	24	10	16	17	21
[8]	0.10µm GaN/Si	/	37-43	12	10	18	30	10.08
HPA-LB	0.15µm GaN/SiC	Pulsed 25 µs/10%	35-41	19	8-10	> 28	25	10.44
HPA-MB	0.15µm GaN/SiC	Pulsed 25 µs/10%	37-42	19	8-10	> 28	25	10.44
HPA-HB	0.15µm GaN/SiC	Pulsed 25 µs/10%	38-43	19	8-10	> 28	25	10.44

V. Conclusion

In this paper, Q-band three single-ended HPAs designed for space applications and covering 35-43GHz frequency band were presented. Thanks to a harmonic tuning on source and load impedances of the transistor, the PAE level has been maximized on a large operating frequency range.

This work highlights and confirms the potential of the used 0.15-µm GaN on SiC technology in terms of integration and RF performances considering the space de-ratings rules.

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