Broadband Hetero-Integration of InP Chiplets on SiGe BiCMOS for mm-Wave MMICs up to 325 GHz

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***Abstract* — We present a broadband flip-chip approach for the hetero-integration of indium phosphide based chiplets on a BiCMOS carrier. To accommodate for a limited temperature budget, the process temperatures are kept below 200°C in order to not degrade device performance. Using indium soldering together with a pillar-based approach instead of the common bump array technique ensures good scalability, repeatability and flexibility in terms of complex broadband transitions. The RF performance of this transitions was evaluated using standard 50 Ω microstrip line test chips and carriers without any special interconnect optimization. The results show excellent broadband characteristics from DC up to 325 GHz.**

***Keywords* — Flip-chip interconnects, hetero-bipolar transistor, indium phosphide (InP), millimeter-wave (mm-wave) integrated circuits, semiconductor device packaging**

I. Introduction

Nowadays, high-speed wireless and optical communications such as 6G as well as THz sensing and imaging applications drive the advancement of mm-wave Monolithic Microwave Integrated Circuits (MMICs) [1], [2]. In many cases, these technologies demand relatively high output powers and energy efficiencies at frequencies well above 100 GHz. With the standard CMOS technologies reaching their physical limits, other technologies like indium phosphide (InP) hetero-bipolar (HBT) and high-electron-mobility (HEMT) transistors, silicon-germanium (SiGe) and even gallium-nitride (GaN) HEMTs come into play. Since all these technologies have different strengths and weaknesses, hetero-integration techniques with low-loss RF interconnects have become the corner stone for seamless hetero-integration of different III-V-based technologies with CMOS and BiCMOS technologies. This would allow harvesting their advantages without compromising in system complexity. With 6G extending into the sub-THz frequency range, such commercially viable solutions for frequencies above 100 GHz become a necessity.

This is the motivation behind the work presented here. The target is to combine bipolar InP chips with BiCMOS to form a single InP-on-BiCMOS chip. As a first step, an interconnect technology has to be developed that satisfies the boundary conditions in terms of RF performance, process compatibility and volume scalability, which is the purpose of this paper.

Conventional wire bonding has been successfully demonstrated for frequencies below 100 GHz. However, with increasing frequency and bandwidth, wire-bond inductance severely limit its electrical characteristics. The flip-chip approach, on the other hand, allows for minimal physical separation between the chip and carrier, thus minimizing the transitions losses between the circuits. It yields an arrangement where the InP chip(let) is stacked upon the BiCMOS chip or wafer. With the current placement accuracy of fine-placers, chip alignment errors of less than 1 µm can be routinely achieved. Such an approach is believed to have significant advantages in hetero-integration when compared to other scenarios, due to its ease of accommodating different technologies processed even in different fabrication facilities.

Details of this process are described in the following section. The difference between our new process and the standard ball-bump based flip-chip process is the extreme scaling of the bump height and area which makes it feasible to cover frequencies well above 200 GHz.

II. Process

The most critical parameter in the flip-chip process is the choice of the solder material. Due to the limited thermal budget of the InP MMIC process (temperatures above 200 °C should be avoided), indium (In) was chosen because of its low melting point of around 156 °C and the low surface tension [3]. To be able to accurately control the separation between the chip and the carrier, a gold pillar structure was incorporated on top of which the indium layer for soldering is placed. A cross section of the process flow is depicted in Fig. 1.

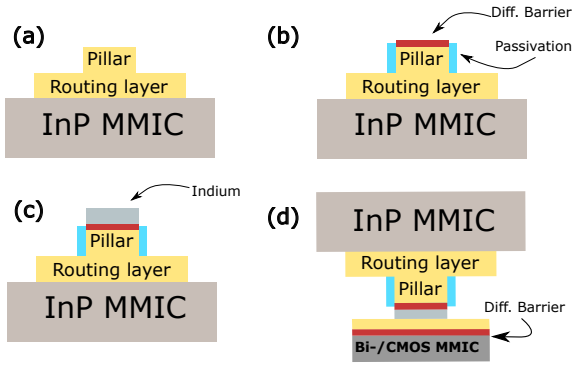


Fig. 1. A simplified process flow diagram of the flip-chip process developed. Starting with the pillar galvanic (a), the diffusion barrier and the passivation (b) are deposited. This is followed by the indium evaporation (c), and finally flip-chip bonding on the BiCMOS carrier (d).

The pillars are grown using a gold-galvanic process with a final thickness of $4\,\mu\mathrm{m}$. Subsequently, a platinum-based diffusion barrier is evaporated on top of the pillar serving as an under bump metallization (UBM). The sidewalls of the pillars are encapsulated with silicon nitride, in order to limit the indium diffusion. Indium with a thickness of $2\,\mu\mathrm{m}$ is finally deposited using e-beam evaporation and lifted off to realize the entire pillar structures. The final pillar structure can be seen in Fig. 2. The process utilizes i-line stepper lithography and is compatible to the InP DHBT MMIC process. The InP chiplet with the bumps is then flipped and mounted onto the BiCMOS wafer or substrate using soldering. Thermal stress was taken into consideration such that the process maintains strictly a thermal budget below $200\,^{\circ}\mathrm{C}$. This temperature was chosen as even with cyclic annealing to $200\,^{\circ}\mathrm{C}$ little-to-no changes were observed in the active circuit components

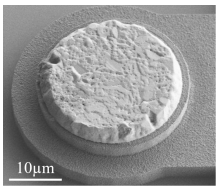
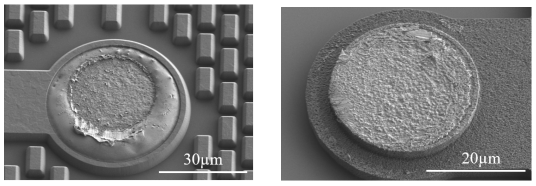


Fig. 2. SEM image of a fully processed pillar

The process was electrically and mechanically qualified. First, 4-terminal DC measurements were performed on 30 pillar daisy-chain structures which were flipped onto a test carrier. Electrical measurements show a connection resistance of about $10\,\mathrm{m}\Omega$ per bump. Mechanical shear tests were performed on the same daisy chains and a shear force of about $1\,\mathrm{N}$ was achieved. In Fig. 3a and 3b the SEM pictures of a released connection are presented. Fig. 3a, the pad on the BiCMOS carrier, shows that most of the indium is pressed out of the bond interface, leaving only a very thin layer between the pillar and the pad. The excess indium is kept in place by the passivation on the BiCMOS side, yielding a very controlled interface. The very thin indium adhesion layer provides good mechanical stability with low electrical resistance at the same time.



(a) (b)

Fig. 3. Flip-chip interconnect post shear test: (a) landing pad on the BiCMOS carrier ; (b) pillar on the InP MMIC chiplet.

III. Characterization

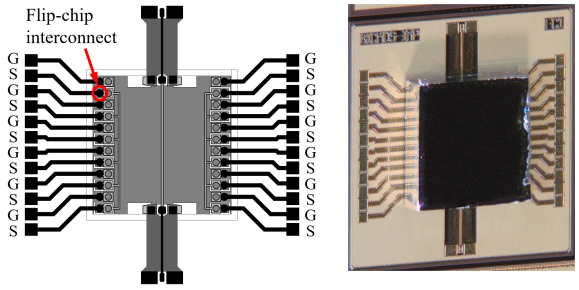
We evaluated the DC and RF interconnect characteristics of the proposed InP-BiCMOS hetero-integration technology using a passive structure. InP chiplets with a $50\,\Omega$ thru-line were bonded to a BiCMOS carrier with the appropriate feeding lines so that it can be probed with on-wafer measurement tips. On each carrier, two InP chiplets were bonded successively. The carrier was fabricated using IHPs backend technology with a 7-layer aluminum metallization stack. $10\,\mu\mathrm{m}$ wide lines in TopMet2 layer were used for the DC routing. The pads on the BiCMOS wafer were equipped with an electroless deposited nickel diffusion barrier covered by a thin gold bonding layer. For the chiplets we used the InP MMIC-stack with BCB as a dielectric and $4\,\mu\mathrm{m}$ electroplated gold for the pillars, as described in the previous section. The chiplets had a size of $900 \times 900\,\mu\mathrm{m}^2$ and incorporated a symmetrical pad layout with a total of 30 pillars, 6 for the two RF interconnects and 24 for DC and thermal connection.

A. DC Measurements

In order to verify the electrical interconnect quality, we first measured the electrical resistance using a four-port configuration. Force and sense were placed on the same pad of the carrier, respectively. On each side of the chiplet, all DC pads (S) were connected on the chiplet to one another to allow a daisy chain measurement of two consecutive flip-chip interconnects at a time. Hence any measured value includes:

- carrier line ($385\mu m \leq l_1 \leq 435\mu m$)
- flip-chip transition 1
- chiplet line ($l = 230\mu m$)
- flip-chip transition 2
- carrier line ($385\mu m \leq l_2 \leq 435\mu m$),

were $l_1 \neq l_2$ is. The setup for the DC characterization is shown in Fig. 4a. Black and dark gray denote the two metallization layers TopMet2 and Met3 on the BiCMOS carrier, while semi-light gray and light gray correspond to GND and G2 on the InP MMIC chip.



(a) (b)

Fig. 4. RF submounts: (a) Mounted test structure: electrical lines on the BiCMOS carrier are displayed in black and dark gray while for the chiplet lines the lighter gray tones are used. (b) Microscope picture of a DUT.

The calculated DC line resistance for the 5 adjacent transition pairs falls in the range of $560\,\mathrm{m}\Omega$ to $600\,\mathrm{m}\Omega$. Due to the chip symmetry, 10 measurements per chip are possible, yielding 12 measured transitions. We used two identical BiCMOS test carriers equipped with two DC-wise equal landing spots, respectively. All chiplets were bonded one after the other using the same bond parameters. The measurement results are shown in Fig. 5. All measured transitions show good electrical connectivity and their DC

resistance shows comparable average values and distributions. The offset of about 20 mΩ to 30 mΩ can be attributed to the contribution of the two transitions. This is in reasonably good agreement with the value of about 10 mΩ per bump mentioned above. Furthermore, the results showed almost no systematic difference between the first and second bonded chiplet on each carrier. This indicates good wafer-level scalability and is in good agreement with the results presented in [4].

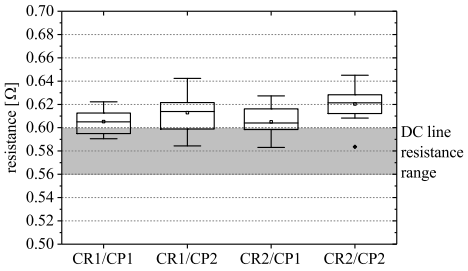


Fig. 5. DC characterization of 4 chiplets (CP) on two different carriers (CR). Ten measurements per chip each consisting of two consecutive flip-chip transitions including connecting lines

B. RF Measurements

We used two setups to characterize the submounts, which consist of 6 chiplets mounted onto the 3 carriers as described earlier. A single-sweep 220 GHz Vector Network Analyzer (VNA) and a VNA with waveguide modules in the frequency range from 220 GHz to 325 GHz utilizing 50 µm pitch ground-signal-ground (GSG) on-wafer probes. The calibration and line characterization was carried out using multiline Thru-Reflect-Line (mTRL) [5] with both on-carrier and on-chiplet calibration standards. The reference planes shown in Fig. 6a were set in the microstrip line environment 160 µm in front of the transition.

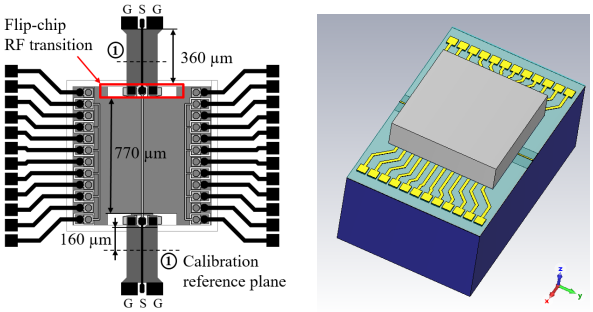


Fig. 6. RF submounts: (a) Sketch of the RF submount position including calibration reference plane and microstrip line lengths; (b) 3D-Model of the test structure within the calibration reference planes.

The test sub mount used for the evaluation had standard 50 Ω microstrip lines on the BiCMOS carrier and on the InP chiplet, respectively. Optimized launchpads for 50 µm pitch GSG probes were used for the carrier probing, were as for the flip-chip interface non-optimized 45 µm diameter pads with a pitch of 75 µm were incorporated. On the chiplet side, a 770 µm long microstrip line connects the two GSG interconnect launchpads equipped with the pillars that form the flip-chip interconnect. The use of mTRL enabled us to extract the line characteristics, which is important to later extract the performance of the transition itself. The results are shown in Fig. 7.

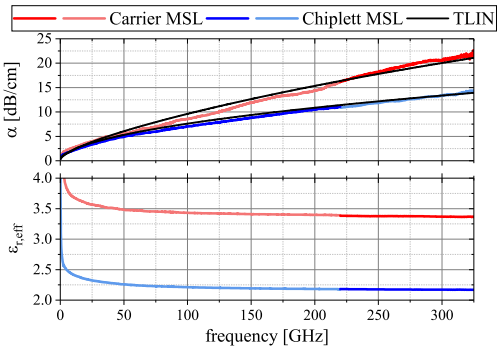


Fig. 7. Characteristics for the 50 Ω microstrip lines on the carrier and the chiplet, the two frequency bands are distinguished by color since each measurement had to be performed separately.

The upper graph shows the frequency dependent attenuation of both microstrip lines, whereas in the lower graph the effective relative permittivity is plotted. The transition between the two measurement bands below and above 220 GHz exhibit a very smooth transition for both lines, which indicates a reliable calibration and good measurement accuracy.

In order to analyze the various loss contributions the results were compared to the lossy transmission line model (TLIN) in Agilent ADS. The model takes conductor and dielectric losses into consideration. Conductor losses are treated as a square root frequency dependence of the attenuation constant ($\alpha(f) = \alpha(F) \cdot \sqrt{\frac{f}{F}}$), whereas dielectric losses are included in the shunt admittance G of the R-L-C-G transmission line equivalent circuit in the model. The frequency dependency is modeled using the linear relation ($\omega \cdot \tan\delta$). Radiation losses are not taken into account. Comparing the results to the reasonably well fitted model proves the expectation, that conductor losses are dominant for the microstrip line on the chiplet. They constitute a major part for the line losses on the carrier as well, while there appears to be an additional contribution the root cause of which has yet to be determined.

As already mentioned, each BiCMOS carrier offered landing spots for two InP chiplets. Accordingly, the 6 measured chiplet DUTs were distributed among 3 individual carriers. DUT1 and DUT4, DUT2 and DUT5, and DUT3 and DUT6 shared the same carrier, respectively. RF-wise, both landing spots on the carrier were slightly different. One had the area below the chiplet conductor-free (w/o shield), and one had a closed metal shield below (w/ shield), i.e., at the same metallization level used for the microstrip ground of the carrier. Thus, DUT1, DUT2, and DUT3 are w/o shield and DUT4, DUT5 and DUT6 are w/ shield. Each back-to-back measurement includes the performance of the 160 µm long access line parts on the carrier, two flip-chip interconnects

and the 770 µm long microstrip line on the chiplet. The flip-chip interface is composed of 75 µm pitch GSG pads, optimized for wafer probing up to 350 GHz. Each pad was equipped with 30 µm diameter, 4 µm high pillars for the vertically self aligned bonding. This leads to a transition with a geometrical length of about 100 µm. To evaluate the broadband characteristics of the interconnect we used the extracted propagation constants to estimate the losses of the pure microstrip line on the DUT back-to-back measurements. This is a fairly good approximation since reflections are low. Although a slight detuning of the chiplet characteristic impedance is induced, due to the small chiplet-to-carrier spacing, the effect on the losses is expected to be low. The results are plotted in Fig. 8, together with the frequency response of the 6 measured DUTs.

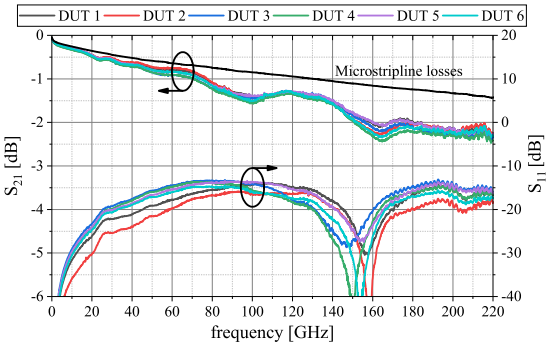


Fig. 8. Back-to-back small signal characteristics of flip-chip bonded InP chiplets DUT1…DUT6 on 3 BiCMOS carriers, DUT1, DUT2 and DUT3 w/o shield and DUT4, DUT5 and DUT6 w/ shield below the chiplet.

Overall, excellent broadband characteristics are obtained. The low variation in the frequency response of all 6 measurements indicates the good repeatability of the bond process and documents the low influence of the shielding below the chiplet. The reflections remain lower than −13 dB for the two-interconnect structure over the entire frequency band from DC to 220 GHz Comparing the insertion loss with the pure line losses derived from the propagation constants in Fig. 7, we calculate a per-transition loss well below 0.5 dB for almost the entire bandwidth.

We used DUT1 and DUT6 to further characterize the interconnects up to 325 GHz. The results are shown in Fig. 9. Both devices show very similar responses. The return loss for both devices up to 300 GHz remains below −13 dB. The insertion loss follows the pure line losses, yielding loss per transition close to 0.5 dB. Over 300 GHz the characteristics get slightly deteriorated to −10 dB for the return loss and 0.75 dB per transition insertion loss. Regarding the interconnect itself, one concludes that the approximately 5 µm high flip-chip bump structures induce very low parasitics, so the major parasitic effect originates from the pad design on the carrier and on the chiplet. These pads were chosen to be compatible to wafer probing and thus future designs with RF-optimized pads can even improve the interconnect performance.

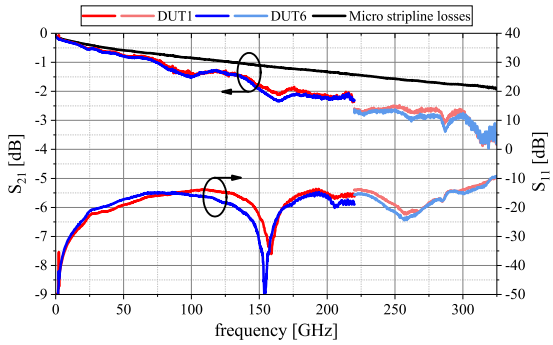


Fig. 9. Back-to-back characteristics up to 325 GHz of flip-chip bonded InP test chiplets on 2 different BiCMOS carriers, DUT1 w/o and DUT6 w/ shield

IV. Conclusion

A flip-chip-based approach is presented for the broadband hetero-integration of InP MMIC chiplets on BiCMOS carrier. Indium is used to enable soldering with less than 200 °C process temperature to maintain the full performance of the InP chips. High yield and reasonably mechanical stability are achieved. RF characterization up to 220 GHz of several samples showed excellent broadband RF performance together with good repeatability. Reflections are below −13 dB for the back-to-back structure and a very low insertion loss below 0.5 dB per transition is extracted. Further measurements extending the frequency range up to 325 GHz revealed very good performance for the entire investigated frequency range. These results document that the proposed hetero-integration process for InP chiplets on BiCMOS carrier chips is very promising for a variety of applications in the frequency range beyond 100 GHz.

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