A Q-band SiGe-HBT Cryogenic Colpitts VCO for Frequency-Division Multiplexed Quantum Computing

Eren Vardarli[#1], Xiaodi Jin[#], Austin Ying-Kuang Chen[$], Klaus Aufinger[*], Michael Schröter[#]
[#]Chair for Electron Devices and Integrated Circuits, TU Dresden, 01062 Dresden, Germany
[$]Department of Electrical and Computer Engineering, University of California, Santa Cruz, USA
[*]Infineon Technologies AG, 85579 Neubiberg, Germany
[1]eren.vardarli@tu-dresden.de

***Abstract*— A Q-band (33-50 GHz) Colpitts voltage-controlled oscillator (VCO) operating from 300 K to 4 K is presented. To validate model-to-hardware correlation, the compact model HICUM/L2 has been extended, and the corresponding model parameters were extracted at cryogenic temperatures (CTs). At 1 MHz/10 MHz offset, the VCO achieves a phase noise of -94/-120 dBc/Hz at 46 GHz (CT) and -92.6/-115 dBc/Hz at 43.5 GHz (room temperature (RT)) while consuming a P_{DC} of 45 mW from a 2.5-V supply voltage. The measured tuning range is 39.5 to 45 GHz (13%) at 300 K and 43.9 to 46.5 GHz (5.8%) at 4 K. With the cascode buffer in the Colpitts topology, the measured single-ended output power at CT and RT is 5.8 dBm and 4.5 dBm, respectively. To the best of the authors' knowledge, this is the highest reported oscillation frequency and output power for a VCO that can operate under cryogenic conditions for quantum computing.**

***Keywords*— Colpitts, cryogenic operation, hetero-junction bipolar transistor, mm-wave, phase noise, quantum computing, silicon-germanium, Q-band, voltage-controlled oscillator.**

I. Introduction

Quantum computing has generated great interest in the area of integrated microwave control/read-out electronics [1], [2] due to the introduction of scalable, high-fidelity solid-state qubit technologies such as single-electron spin-qubits confined in gate-addressable silicon quantum dots [3], [4]. These structures have longer coherence times than competing technologies and have the potential to be integrated in high density with reliable commercial silicon-based fabrication processes [5], [6].

Due to the need for fault-tolerant quantum computers that call for thousands of qubits to be integrated within the same quantum processor, highly energy-efficient control/read-out schemes have to be implemented to keep the power consumption at ~1 mW/qubit, limited by the cooling power of existing refrigerators (~1.5 W at 4 K). To reach this goal, simultaneous control/read-out of spin-qubits using frequency division multiplexing (FDM) has been proposed [1], [2], [7], [8]. This approach has the added benefit of reducing the number of LO generators and RF cables-per-qubit needed to interface the quantum processor (20-100 mK) with the control/read-out electronics (1-4 K). However, FDM requires multi-carrier generation (i.e. an on-chip cryo-PLL [2], [9]), an increase in the receiver bandwidth and pulse shaping of the microwave control signals to minimize spectral leakage to other qubits. The increase in bandwidth can be achieved by moving to millimeter-wave (mm-wave) frequency bands (>30 GHz) where an intermediate frequency (IF) bandwidth of tens of gigahertz is possible [10]. In addition, digitally-intensive power-hungry polar modulators used for complex pulse shaping [8] can be avoided by choosing higher channel spacing between qubits, making use of the abundantly available bandwidth. Moreover, the surface mounted (at <1 GHz) LC matching networks used for dispersive gate-based read-out of quantum dots can be replaced by on-chip inductors (<1 nH) and capacitors, reducing the area and mitigating routing/interconnect issues while improving the read-out bandwidth.

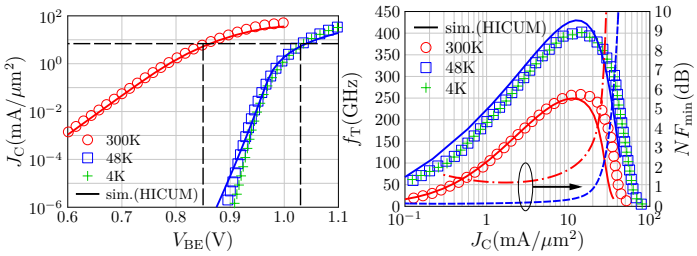


Fig. 1. Measured and simulated (a) transfer characteristics and (b) transit frequency (f_T) versus collector current density (J_C) of a single HBT at 4 K, 48 K and 300 K for $V_{BC} = 0\,V$. Minimum noise figure (NF_{min}) is simulated at CT (dashed line) and RT (dash-dotted line) with $V_{BC} = 0\,V$ at 45 GHz.

The cryogenic VCO presented in this work can be integrated as part of a mm-wave frequency synthesizer to generate multi-carrier control signals and/or to down-convert the qubit-modulated carriers to IF-band in an FDM-based mm-wave receiver. The circuit was fabricated in B11HFC, a 250/370-GHz f_T/f_{max} 0.13-µm silicon-germanium (SiGe) HBT BiCMOS process of Infineon AG with 6 copper metal layers, in order to benefit from the lower (an order of magnitude) $1/f^3$ (flicker) phase noise corner of HBT-based VCOs at CTs compared to CMOS-based VCOs [11].

II. Design Considerations and Circuit Description

A. Cryogenic modeling and device measurements

Due to the increase in the turn-on voltage of the HBT with cooling, higher voltage headroom is required at CTs to operate the VCO. As indicated by the horizontal lines in Fig.1a, the base-emitter (BE) voltage of the HBT must be

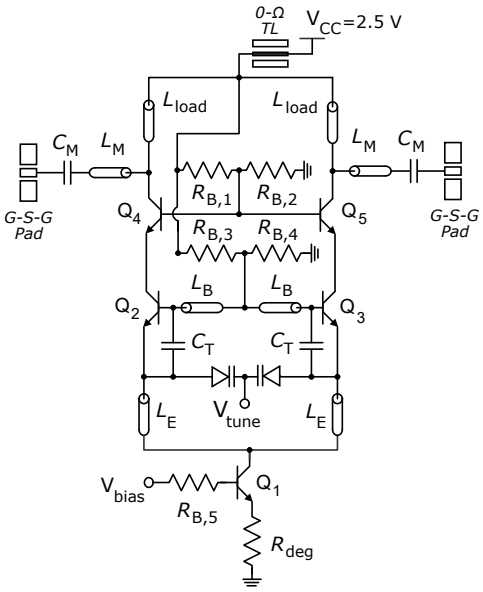


Fig. 2. The schematic of the Q-band cryogenic VCO.

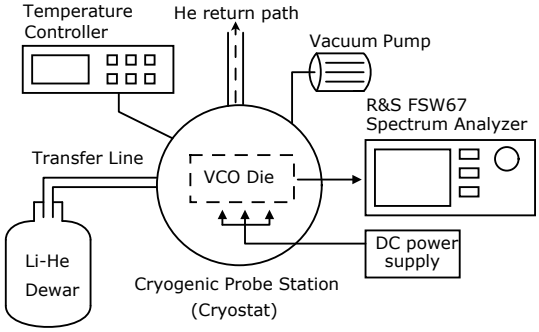


Fig. 3. The Q-band cryogenic VCO measurement setup.

increased by ∼160 mV at 4 K in order to achieve the same J_C as 300 K. This adjustment is required to have an accurate comparison of performance parameters between CT and RT. The increase in the slope of the transfer characteristics at 4 K and 48 K indicates the increase in the transconductance (g_m) of the device. This, together with the decrease of the transistor's series resistances (i.e. $R_{Bx}, R_{Cx},$ and R_E), is reflected in Fig.1b where the measured peak f_T is improved by a factor of 1.6 at CTs. The HICUM/L2 has been extended [12], [13] and its model parameters were extracted for various scalable device geometries and configurations by performing dc and s-parameter measurements at CTs. These parameters are optimized at 48 K and facilitate the convergence of transient simulation. From Fig.1a and Fig.1b, it is seen that the measured dc and rf characteristics of the device do not change below 48 K and that the optimized model parameters at 48 K can be used to represent simulation results at 4 K.

B. Circuit design at RT and CT

The schematic of the Q-band VCO is presented in Fig. 2. The VCO is based on the differential common-collector Colpitts topology (Q_{1-3}) with a cascode buffer (Q_{4-5}) which enables current re-use at the cost of a slightly higher supply voltage. Oscillation frequency is determined by L_B and the capacitance seen from the base of Q_{2-3} which is mainly composed of the varactor capacitance. An additional MIM capacitor (C_T) is added between the base and emitter terminals of Q_{2-3} to increase the varactor capacitance seen by L_B, thereby increasing the tuning range. A collector current of 9 mA is targeted for the devices in order to obtain high output power and low phase noise by improving the voltage swing across the tank. All transistors are biased with $J_C \sim 7\,\mathrm{mA/\mu m^2}$ to operate in the low noise region of the HBT (Fig. 1b). The current source is composed of two parallel $10\,\mu\mathrm{m} \times 0.13\,\mu\mathrm{m}$ transistors and is degenerated with a small resistance (10 Ω). Resistive dividers ($R_{B,1-4}$) are utilized for biasing the negative-g_m and buffer transistors to suppress common-mode oscillations and cancel the temperature dependence of the polysilicon-type resistors, thereby achieving constant bias across a wide range of temperatures. Since the temperature coefficient of polysilicon resistors change with geometry (i.e. the width and length), a unit cell of fixed geometry is used in series to achieve the needed resistance values. The choice of unsalicided p+ doped polysilicon resistors was justified and their usage was successfully demonstrated in previous cryogenic designs [14]. The inductor located at the emitters of Q_{2-3} (L_E) is used to isolate the parasitic capacitance of the current source from the tank and to filter the associated high-frequency noise [15].

The circuit operation is verified in simulation for both RT and CT by modifying V_{bias} to achieve identical supply currents at 4 K and at 300 K (i.e. 18 mA). The values of passive elements such as MIM caps and transmission lines are expected to change slightly (∼5%) at CTs [16].

III. Measurement Setup and Experimental Results

As illustrated in Fig. 3, the cryogenic measurement setup uses the LakeShore Cryotronics table-top probe station (TTPX) as the cryostat (chamber), which has six probe arms. In the setup, four arms are used for the DC needles (i.e. V_{CC}, V_{tune}, V_{bias}, and ground) and the remaining two arms for the cryogenic GSG RF probes. Single-ended phase noise and spectral power measurements are performed using the FSW67 spectrum analyzer from Rohde&Schwarz. The second RF probe is landed as well and is terminated with a 50 Ω off-chip load. The 1.85 mm (up to 67 GHz) coaxial cable outside the cryostat along with the cryogenic cable and the probe located inside the cryostat are calibrated using the N5247A PNA-X from Keysight. The tuning voltage is applied with a high-precision SMU (B2912A) while the supply and the bias voltages/currents are provided/measured by another SMU (N6705B). The liquid helium in a Cryotherm STRATOS dewar is fed through the transfer line to the cryostat in order to perform the cooling operation down to 4 K. Prior to cooling, a vacuum pump system HiCube 80 from Pfeiffer is used to

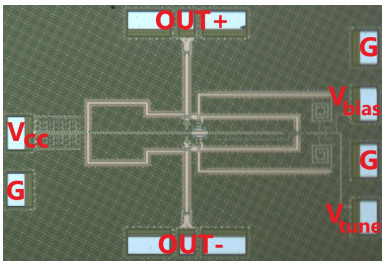
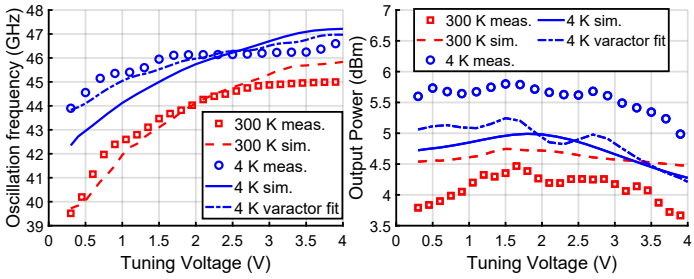


Fig. 4. Chip micro-photograph of the Q-band cryogenic VCO.



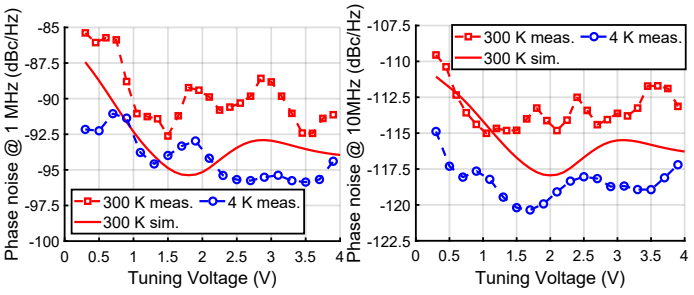
(a) (b)

Fig. 5. Measured and simulated (a) oscillation frequency and (b) single-ended output power at 4 K and at 300 K. Measurements are performed at the same supply current for RT and CT.

establish the required vacuum level of 10^{-6} bar inside the chamber.

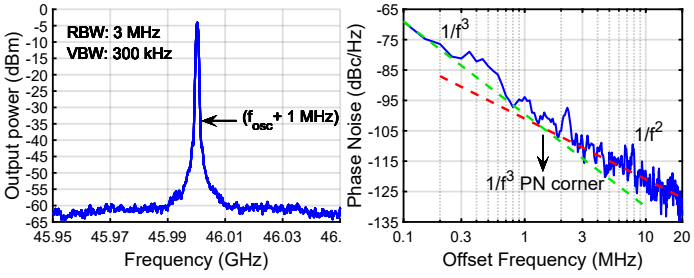
The chip micro-photograph is shown in Fig. 4. The overall chip area including the pads is $820\,\mu\text{m} \times 540\,\mu\text{m}$. All components including the metal stacks, MIM capacitors, microstrip transmission lines, pads, and the 0-Ω transmission line were EM-simulated using the 2.5D ADS Momentum.

As shown in Fig. 5a, the oscillation frequency ranges from 39.5 to 45 GHz at RT which is equivalent to 13% fractional bandwidth. The oscillation frequency increases at CT due to the decrease in the value of charge-based (i.e. depletion and diffusion) BE and base-collector (BC) capacitance of Q_{2-3} (∼24% decrease obtained from simulation at 4 K). The depletion capacitance of the junction-based diode varactor is also expected to decrease. The tuning range at CT decrease to 5.8%, presumably because of the earlier saturation of the diode varactor at CT (∼1.7 V) than at RT (∼3 V), leading to the degradation of C_{max}/C_{min} ratio. Since a cryogenic model of the diode varactor has not been available, the simulation result at CT cannot capture these effects. Therefore, the depletion capacitance of the varactor, modeled by the SPICE diode equation $C_j = C_{j0}/(1 - V_{pn}/V_{bi})^m$, is modified to achieve a better fit across the tuning range. The zero-bias p-n junction capacitance (C_{j0}) is reduced by 15%, the built-in junction voltage (V_{bi}) is increased by 200 mV as suggested in Fig.1a, and the junction grading coefficient (m) is reduced to account for the degradation of the C_{max}/C_{min} ratio. The tuning range can be improved by employing switched-capacitor banks for coarse tuning, composed of weakly temperature-dependent MOM capacitors.



(a) (b)

Fig. 6. Measured (4 K/300 K) and simulated (300 K) phase noise at (a) 1 MHz and (b) 10 MHz offset.



(a) (b)

Fig. 7. Measured (a) output spectrum within a span of 100 MHz and (b) phase noise up to 20 MHz of offset with a center frequency of 46 GHz at 4 K. Output power is not calibrated for the probe and cable losses.

Fig. 5b shows an increase at CT in the output power across the tuning range which can be attributed to the increase in g_m and the higher quality factor of the passive elements due to higher metal conductivity and the lower substrate loss [16]. The measured output power at CT is relatively constant across the tuning range with only 1.8 dB variation. The characteristic of the output power across the tuning range is better captured by using the same modified varactor model parameters and values. The two separate single-ended outputs can drive a divider chain and a quadrature mixer simultaneously with high isolation when the VCO is employed as part of a cryogenic PLL.

The measured phase noise at CT is improved by ∼5 dB at 10 MHz offset (Fig. 6b) because of the decrease in temperature and the improvement in the quality factor of the tank. The quality factor of the varactor is expected to improve caused by the freeze-out of the substrate, causing it to present higher resistivity. The phase noise improvement at 1 MHz offset is less prominent due to the increased $1/f^3$ phase noise corner at CTs [11]. The best case phase noise values across the tuning range at CT are -95.8/-120.3 dBc/Hz at 1 MHz/10 MHz offset. Phase noise simulation results at CT are not available due to a convergence issue during the harmonic balance simulation. Fig. 7b shows a measured flicker noise corner of 1.3 MHz which explains the drop in improvement at 1 MHz offset.

Table 1 outlines the performance of this work and other prior published state-of-the-art cryogenic VCOs. The VCO has the highest oscillation frequency and the output power among

Table 1. Comparison of state-of-the-art cryogenic VCOs with highest reported operating frequencies

	ISSCC 2022 [11]	ISSCC 2021 [7]	CICC 2021 [9]	RSI 2018 [17]	**This work**
Technology	130 nm SiGe	40 nm CMOS	40 nm CMOS	130 nm SiGe	**130 nm SiGe**
Temperature (K)	3.5	4.2	4.2	4	**4**
Frequency (GHz)	15.9	12.7	10.8	33.7	**45.2**
Tuning range	13.9-18.1	N/A	9.4-11.6	30.7-36.7	**43.9-46.5**
P_{DC} (mW)	3.1	4.4	1.7	112[a]	**45**
P_{out} (dBm)	N/A	N/A	N/A	-21.5	**5.8**
PN[b] @1 MHz / 10 MHz (dBc/Hz)	-119.9 / -141.7	-114.5 / -136.2	-113 / -138	-110 / NA	**-95.8 / -120.3**
Flicker PN corner (kHz)	165-497	800	4000	N/A	**1300**
FoM[c] @1 MHz / 10 MHz (dB)	199[d] / 200.8[d]	190.1[d] / 191.8[d]	191.4[d] / 196.4[d]	159.1 / NA	**178.2 / 182.7**

[a]estimated from plot, [b]best-case values across the tuning range
[c]$\mathrm{FoM} = |\mathrm{PN}(\Delta\mathrm{f})| + 20\log\left(\frac{\mathrm{Freq.}}{\Delta\mathrm{f}}\right) - 10\log\left(\frac{\mathrm{P_{DC}\,(mW)}}{\mathrm{P_{out}\,(mW)}}\right)$
[d]normalized to 1 mW output power

the reported works. Good model-to-hardware correlation is achieved at CT for the HBTs only. Modeling of passive elements, especially the diode varactor, and the substrate for cryogenic conditions can further improve the correlation.

IV. Conclusion

Design and characterization of a mm-wave differential cryogenic VCO is presented. The VCO was designed using HICUM/L2 with model parameters extracted at CTs to ensure first-pass success. Reasonable agreement between circuit measurement and simulation has been achieved. Observed deviations are attributed to the lack of a cryogenic model for the varactor and substrate related elements.

At 46 GHz (CT), the phase noise is -94/-120 dBc/Hz at 1 MHz/10 MHz offset with an improvement of ∼5 dB compared to RT at 10 MHz offset. A single-ended output power of 5.8 dBm is achieved at CT, which relaxes the LO buffer requirements needed to drive the I/Q mixer of a mm-wave read-out receiver. The mm-wave operation allows for a high degree of frequency multiplexing of qubits to reduce power consumption and interconnect complexity of control/read-out electronics of a quantum computing system operating at 4 K. To the best of the authors' knowledge, this is the first successful demonstration of a Q-band cryogenic VCO with the highest reported oscillation frequency and output power.

Acknowledgment

The authors would like to thank Infineon Technologies AG for chip fabrication.

References

[1] J. P. G. V. Dijk *et al.*, "A scalable cryo-CMOS controller for the wideband frequency-multiplexed control of spin qubits and transmons," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2930–2946, Nov. 2020.

[2] Y. Peng, A. Ruffino, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba, and E. Charbon, "A cryo-CMOS wideband quadrature receiver with frequency synthesizer for scalable multiplexed readout of silicon spin qubits," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2374–2389, Aug. 2022.

[3] M. Veldhorst *et al.*, "An addressable quantum dot qubit with fault-tolerant control-fidelity," *Nat. Nanotechnol.*, vol. 9, no. 12, pp. 981–985, Oct. 2014.

[4] M. Veldhorst, H. G. J. Eenink, C. H. Yang, and A. S. Dzurak, "Silicon CMOS architecture for a spin-based quantum computer," *Nat. Commun.*, vol. 8, no. 1, pp. 1–8, Dec. 2017.

[5] T.-Y. Yang, A. Ruffino, J. Michniewicz, Y. Peng, E. Charbon, and M. F. Gonzalez-Zalba, "Quantum transport in 40-nm MOSFETs at deep cryogenic temperatures," *IEEE Electron Device Lett.*, vol. 41, no. 7, p. 981–984, Jul. 2020.

[6] S. G. J. Philips *et al.*, "Universal control of a six-qubit quantum processor in silicon," *Nature*, vol. 609, no. 7929, pp. 919–924, Sep. 2022.

[7] A. Ruffino, Y. Peng, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba, and E. Charbon, "A fully-integrated 40-nm 5-6.5 GHz cryo-CMOS system-on-chip with I/Q receiver and frequency synthesizer for scalable multiplexed readout of quantum dots," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 2021, pp. 210–212.

[8] B. Patra *et al.*, "A scalable cryo-CMOS 2-to-20GHz digitally intensive controller for 4 × 32 frequency multiplexed spin qubits/transmons in 22nm FinFET technology for quantum computers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 2020, pp. 304–305.

[9] J. Gong, E. Charbon, F. Sebastiano, and M. Babaie, "A 2.7mW 45fsrms-jitter cryogenic dynamic-amplifier-based PLL for quantum computing applications," in *IEEE Custom Integr. Circuits Conf. (CICC)*, Austin, TX, USA, Apr. 2021, pp. 1–2.

[10] U. Alakusu, M. S. Dadash, S. Shopov, P. Chevalier, A. Cathelin, and S. P. Voinigescu, "A 210-284-GHz I-Q receiver with on-chip VCO and divider chain," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 1, pp. 50–53, Jan. 2020.

[11] Y. Peng, A. Ruffino, J. Benserhir, and E. Charbon, "A cryogenic SiGe BiCMOS hybrid class B/C mode-switching VCO achieving 201dBc/Hz figure-of-merit and 4.2GHz frequency tuning range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 2022, pp. 364–366.

[12] M. Schröter and X. Jin, "A physics-based analytical formulation for the tunneling current through the base of bipolar transistors operating at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. 70, no. 1, pp. 247–253, Jan. 2023.

[13] X. Jin, M. Müller, P. Sakalas, A. Mukherjee, Y. Zhang, and M. Schröter, "Advanced SiGe:C HBTs at cryogenic temperatures and their compact modeling with temperature scaling," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 7, no. 2, pp. 175–183, Dec. 2021.

[14] E. Vardarli, A. Mukherjee, X. Jin, P. Sakalas, and M. Schröter, "X- and Ku-band SiGe-HBT voltage-controlled ring oscillators for cryogenic applications," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 7, no. 2, pp. 209–217, Dec. 2021.

[15] E. Vardarli, M. Müller, and M. Schröter, "A W-band SiGe-HBT Colpitts VCO for millimeter-wave applications with an analog tuning range of 12%," in *IEEE 22nd Top. Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Las Vegas, NV, USA, Jan. 2022, pp. 81–84.

[16] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, p. 448–456, Apr. 2020.

[17] A. Hollmann, D. Jirovec, M. Kucharski, D. Kissinger, G. Fischer, and L. R. Schreiber, "30 GHz-voltage controlled oscillator operating at 4 K," *Rev. Sci. Instrum.*, vol. 89, no. 11, pp. 1–5, Nov. 2018.