A 1024-channel Wideband Digital Subsystem Prototype for Large Aperture Array Radio Telescope

Rui Cao[#1], Manqing Wu[#], Xiaohui Tao[#], Guoliang Peng[#], Lihui Jiang[#], Kun Li[$], Jinzhong Zhang[#], Hongqi Zhang[#], Xiaorong Xu[#], Dawei Rong[#], Huiyue Yang[#], Ming-ao Ye[#], Chao Wang[#], Yan Zhang[#], Yulong Xu[#], Xiaolong Yu[#], Dehui Lu[#], Dezhi Zhu[#]

[#]Key Lab of Aperture Array and Space Application, Hefei, China

[$]School of Electronic Information Engineering, Anhui University, Hefei, China

[1]wxtcao@outlook.com

***Abstract*—The new generation of aperture array radio telescopes need to process analogue signals from thousands of antennas, including channelization, correlation, and digital beamforming. The huge amount of raw data poses a great challenge to the processing capability of digital processing system. For 400 MHz bandwidth observation signal fed by 1024 antennas, the digital system should be able to process and exchange a real-time data stream of 3.88 Tbps. A 1024-channel digital subsystem prototype developed, which uses Field Programmable Gate Array (FPGA) transceivers to implement direct, passive, high-speed serial connections between 16 Chinese Tile Processing Modules (CTPM) in one sub-rack and between different sub-racks, standard 10 Gbit/s Ethernet links are used to transfer data to Graphics Processing Unit (GPU) nodes. The digital sub-system can be flexibly customized and expanded to enable different configurations for 16~1024 and 1024*N analogue inputs. Preliminary experimental results such as channel response and channel correction showed that the prototype system has good channel-to-channel consistency and stability, which is suitable for large-scale aperture array applications.**

***Keywords*— Radio telescope, aperture array, digital processing, correlator, digital beamforming, CTPM, FPGA.**

I. INTRODUCTION

Conventional radio telescope array consists of a small number of large reflectors with single or array feed, which has a small number (e.g., dozens to hundreds) of analogue channels . The new generation of aperture array telescope employs large-scale antenna array, with the number of antennas ranging from hundreds to thousands, such as LOFAR[1], MWA[2], LWA[3], CHIME[4], etc., while SKA-LOW even has more than one million antennas[5]. Along with the rapid increase in analogue channels, the observing bandwidth of radio telescopes is also extended. The huge amount of raw data greatly challenges the processing capacity of existing system architectures.

Unlike conventional radio telescopes, which mainly face cost and technical challenges from mechanical structures and cryogenic receivers, the design and implementation of digital processing systems comes to the biggest challenge for aperture array radio telescope. The real-time digital processing to be carried out in aperture array radio telescope usually includes [6]:

- Digitization of analogue signals, which may be carried out hierarchically in multi-receiver systems after down-conversion process.
- Frequency channelization of digital signals, which is done by FFT-based filter banks. Signals from different antennas can be processed in parallel.
- Signals from multiple antennas are combined by weighted summation (i.e., beamforming) or multiplication (i.e., correlation), which can be carried out in parallel on multiple frequency bins.

Each analog input channel contains a signal from one antenna over the entire frequency bandwidth, while data from all antennas on a specific frequency bin is required for beamformer and correlator, which requires a data exchange operation like matrix transpose (Corner-turn). However, when only a small number of beams need to be formed, a hierarchical beamforming can be an alternative, where corner-turn is not required.

Different radio astronomy instruments generally choose the same hardware to achieve the individual functions, such as ADC for analog signal digitization, FPGA for frequency channelization, and FPGA/GPU for beamforming or correlation. However, in terms of the overall system architecture, different radio astronomy instruments have different ways to realize data corner-turn. LOFAR adopts an all GPU solution[7], MeerKAT adopts a solution with FPGA and optical switch[6], while CHIME uses both FPGA and GPU in its digital processing system[8].

Chinese Tile Processing Module (CTPM) for digital processing of radio array telescopes is developed[9][10]. Based on CTPM modules and combining with a 4-stage corner-turn network, a 1024-channel digital subsystem suitable for large-scale aperture array radio telescopes is built. The digital subsystem uses FPGA and GPU as the core of F-engine and X-engine respectively, cooperating with a passive high-speed data exchange network and optical switching network, it can realize the digitization, beamforming, and correlating process of 1024-channel analog inputs and 1024 frequency bins.

The digital subsystem can serve as an independent signal processor for 16~1024 analogue channels, but also can be extended by combining multiple such subsystems, which is well suited for large scale aperture array radio telescopes.

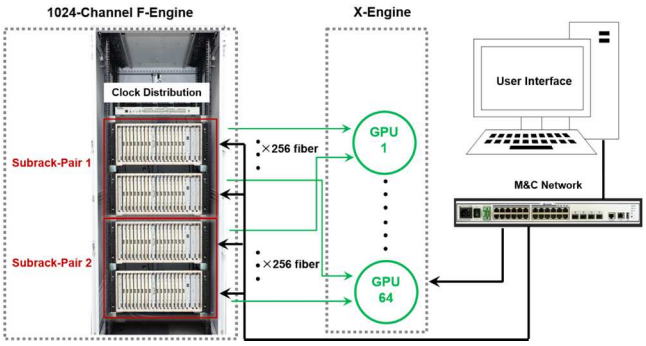

Fig.1. Block diagram of the 1024-channel digital subsystem

II. System Design and Implementation

The F-engine of the 1024-channel digital subsystem adopts FPGA processing module and high-speed backplane, consisting a scalable real-time digital processing system with low cost and low technical risk. Combined with the X-engine processing nodes composed of GPUs, the digital subsystem is capable of handling all the processing tasks from the front-end input to the back-end data pipeline in aperture array radio telescope.

The 1024-channel digital subsystem consists of four 256-channel digital processing sub-racks. Based on the 16-channel CTPM, digital processing sub-rack with different analog inputs can be customized, for example, 16, 32, 64, 128 and 256 channels. The system block diagram is shown in Fig.1 and the main technical specifications are shown in Table 1.

A. F-Engine

The F-engine of 1024-channel digital subsystem contains a total of 64 CTPMs distributed in 4 sub-racks. CTPM is the key module of the digital beamforming system, as shown in Figure 2. One FPGA and four dual channels ADCs are used in the module, which can meet the requirements of most low frequency aperture array, by reasonably selecting data accuracy and number of simultaneous multiple beams.

CTPM digitizes 16 channel signals in 14 bits resolution and 800 MSPS sampling rate, which results in 11.5 Tbps of raw data. The instantaneous bandwidth 400 MHz signal is then divided into 1024 frequency bins, which are then transmitted to the X-engine after 4 stages of corner-turn. Fig. 3 shows the data flow through the F-engine and corner-turn network.

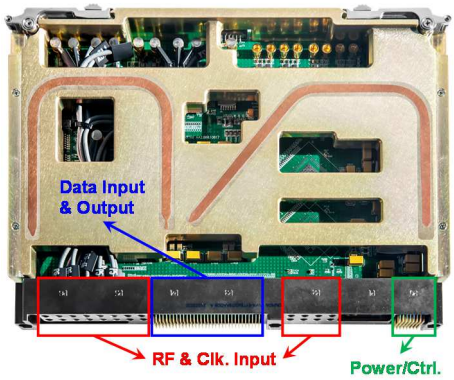

Fig. 2. CTPM with VPX connector and conductive cooling enclosure

Table 1. Technical specifications

Items	Specification
Max Radio Frequency Input	1024
Max Data Flow (Typically)	3.88 Tbps
Max Instantaneous Bandwidth	500 MHz
X-Engine Computation	3.36 PFLOPs/s
ADC Sample rate | Resolution | Noise Spectral Density	1,000 Msamp/s | 14 bits (10 ENOB) | -154 dBFS/Hz
Coarse Channel | Oversample Rate | BW per Channel	1024 | 32/27 | 390.625 kHz
Filter Length	30
Out-of-band suppression | Adjacent Channel Overlap | Ripple	$>$ 60 dB | $<$ 1.8 dB | $<$ $\pm$ 0.07 dB
Channelization Output Bits	4 bit I + 4 bit Q
F-Engine Input Raw Data | bits	11.5 Tbps | 14 bit
Input Data of Third Corner-turn | Output Data | Output Interface	4 Tbps | 3.88 Tbps |32 QSFP+ cable (10 Gbps)
Input Data of Fourth Stage Corner-turn | Output Interface	3.88 Tbps | 512 digital fiber or 128 QSFP+

B. Corner-turn Network

The first stage corner-turn is at CTPM-level. The channelized signals from 16 channels of analogue inputs are divided into 16 subsets in CTPM, and then reorder by frequency bins. After on board exchanges, each subset includes 64 frequency bins of all 16 channels. One of those 16 subsets is kept from data exchange while other 15 subsets are sent to other CTPMs via backplane of sub-rack.

The second stage corner-turn is carried out via the 10Gbps backplane of sub-rack. All 1024 frequency bins from 256-channels inputs are reordered into 32 subsets, each subset includes 32 bins from all 256 inputs. Data exchange between adjacent sub-racks is achieved via QSFP+ 4×10 Gbps cables. Each cable transmits 7.8 Gbps data. Total 256 cables are required for the output data from the second stage corner-turn, which form the third stage corner-turn network.

The third stage corner-turn network is achieved between sub-racks. Digital signal is exchanged between sub-racks and 512 frequency bins from all 512 inputs are gathered in each sub-rack, which are divided into 256 subsets. Data of 8 subsets in one CTPM are sent to one GPU node through eight 10 Gbps optical fibres, the data rate on each fibre is up to 7.6 Gbps.

The fourth corner-turn network is implemented with GPU. 8 subsets of data from one CTPM is fed into the network adapter via 8 optical fibres, which is transferred to two GPUs

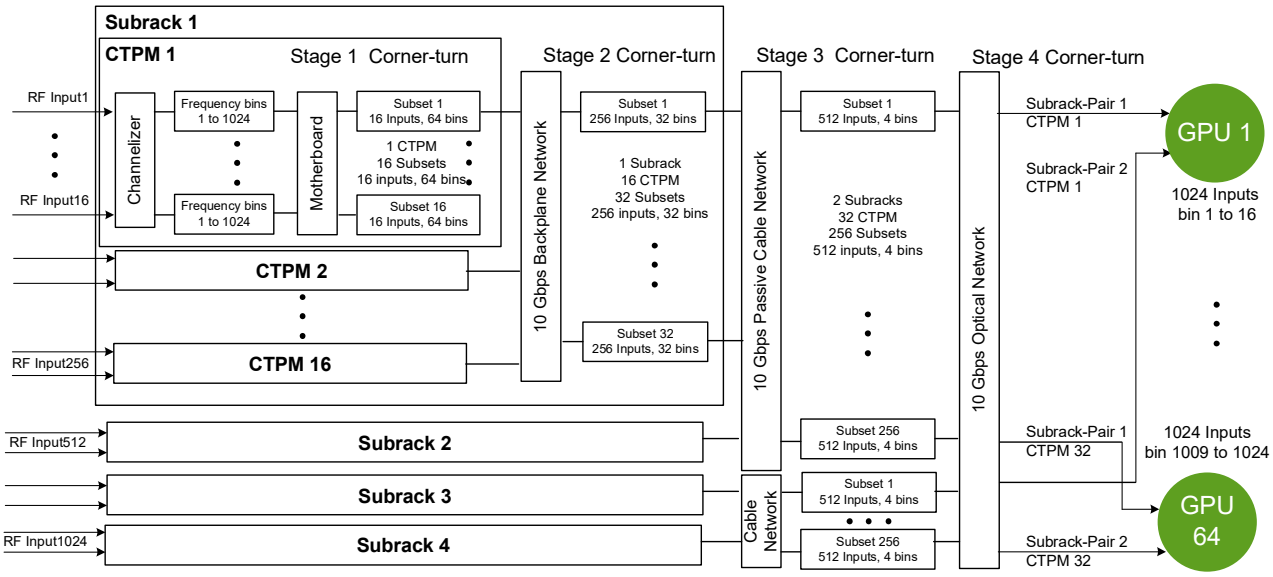

Fig. 3. Data flow through the F-engine and corner-turn network

through PCI-E. Each GPU receives 4 subsets of data from two CTPMs in different sub-rack pairs, to carry out correlating operation of 16 frequency bins from all 1024 inputs.

C. X-Engine

The X-Engine performs beamforming, spatial correlations, and other real-time signal processing operations. Data payload is transferred between FPGA and GPU on 10 Gbps fibre SFP+ links, which is packaged into UDP packets. For a system with N receiving channels and a instantaneous bandwidth of B, the total computation required for correlation operation (including autocorrelation) is:

$$\text{FLOPS} = 8 \bullet 2B \bullet N(N+1)/2 \quad (1)$$

So, the total computation for 1024-channel inputs with 400 MHz instantaneous bandwidth is about 3.36 PFLOPs/s.

A. Monitor and Control

The host computer sends control instructions to four sub-racks and receives BITE information and data samples from sub-racks. The M&C software provides rich control functions includes status information query, system self-test, sample collection, and output channel selection. In addition, the system is equipped with safety and health monitoring such as over-temperature protection and health status management.

B. Liquid Cooling System

Sub-rack adopts a liquid-cooled temperature control system. The coolant that meets the requirements of pressure, flow rate, temperature and water quality is supplied to each sub-rack through circulation pipes. After absorbing heat from functional modules, the coolant returns to the cooled water tank. The circulating system can effectively take away the heat in sub-racks to ensure that the internal electronic devices work properly. The heat consumption of a single sub-rack is no more than 1.5 kW, and the junction temperature of FPGA in CTPM can be guaranteed to not exceed 90°C.

III. Test and Verification

To facilitate the functional verification of system and modules, a 16-channel full-function test and verification system is built, including all the functional modules, such as CTPM module, M&C module, clock distribution module, power module, high-speed backplane, and the host computer. The test and verification system uses air-cooled structure, which has SMA interfaces for RF inputs and external clock input, JTAG interface, serial port, gigabit network port, 10-gigabit optical port, power supply and ground interface, etc.

On this test and verification system, channel response consistency calibration, frequency bin response test, digital beamforming, control function test and data payload transmission function test are carried out.

Sine wave signal from 99MHz to 100MHz in steps of 10 MHz is fed into the test system, output signal is recorded to analyse the response of different frequency bins. The test results are shown in Fig. 4. The out-of-band suppression for frequency bin is better than 65 dB.

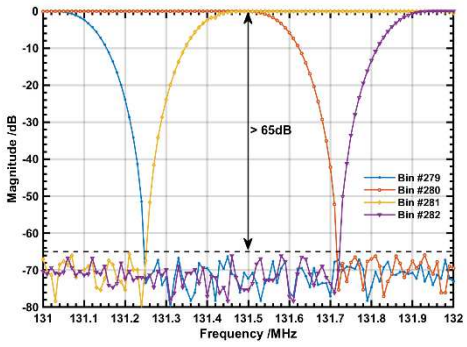

Fig. 4. Frequency bin response test result

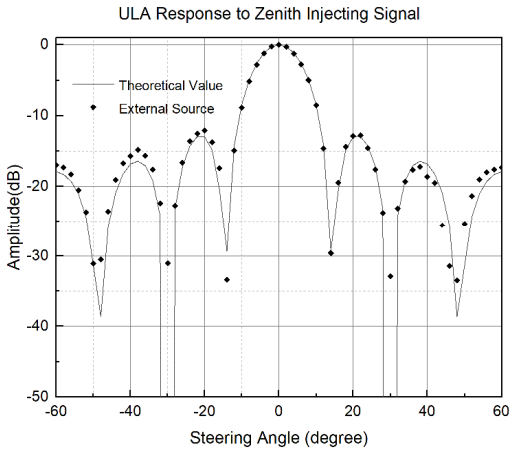

Fig. 5. DBF test result

Sine wave signal is fed into the RF inputs by power divider to simulate a far-field signal normally injected to an 8-antenna uniform line array with an antenna spacing of half a wavelength. Different sets of beam coefficients for scanning angles from -60 degrees to 60 degrees (relative to the normal direction) are configured to the FPGAs and the corresponding output beam data is recorded. Plotting all the amplitude of output data in one figure to get the array response of ULA, as shown in Fig. 5.

After all the independent functions are vitrificated, the inter-channel synchronization of 128-channel digital subsystem is tested. An external signal source was used to generate sweep signals ranging from 49MHz to 201MHz. Samples before and after calibration are collected in each frequency bin. The amplitude and phase of samples from all frequency bins and analogue inputs are shown in Fig. 6. All channels have good amplitude and phase consistency, which can fulfill the requirements of digital beamforming and related processing.

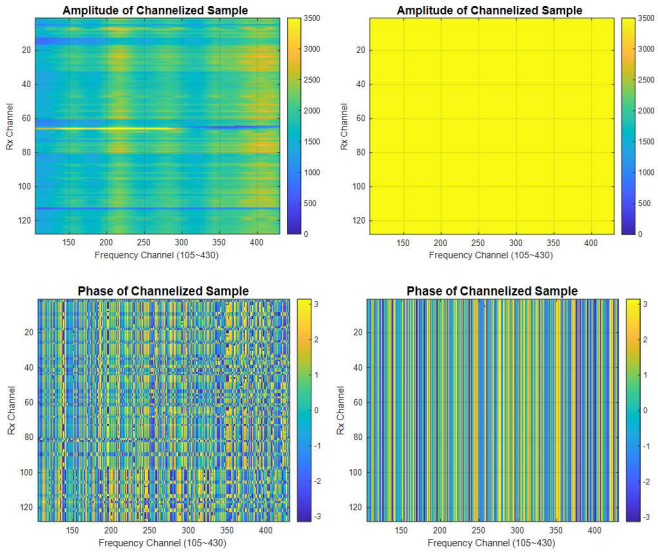

Fig. 6. The amplitude and phase of collected samples from all 128 channels analogue inputs before and after calibration (Top left: quantitative amplitude of 128 channels before calibration; Top right: quantitative amplitude of 128 channels after calibration; Bottom left: phase of 128 channels before calibration; Bottom right: 128 channels after calibration)

IV. CONCLUSION

The 1024-channel wideband digital subsystem adopts FPGA and GPU as core components of F-engine and X-engine respectively. Combined with passive high-speed data exchange network, the implementation is suitable for digital processing of large aperture array radio telescope with its advantages both in cost and technique. A fully functional digital subsystem based on CTPM is built and it includes clock distribution network, M&C system, high-speed passive data exchange network, power distribution system, environmental control system, as well as verified firmware and software. The system demonstrates good stability and reliability, which is especially suitable for the engineering realization of large aperture array telescope instruments.

The system can realize flexible configure expansion of 16- to 1024-channel inputs. Furthermore, it can be used for 1024*N large scale array by combining multiple systems, which is suitable for aperture array telescopes of different size, such as low frequency aperture array, mid-frequency aperture array, PAF, etc.

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