A Monolithic 0.8-to-18 GHz Ultra-Wideband Reconfigurable Dual-Mode Transceiver Front-End in 0.15 μm GaAs Technology

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***Abstract*—This paper presents a monolithic 0.8-to-18GHz reconfigurable transceiver with dual-mode of direction and conversion functions. In the direction mode, the transceiver processes the signals from 0.8 to 5GHz. While in the conversion mode, it up-converts or down-converts the signals in a frequency from 4.5 to 18GHz. An overlap of 0.5GHz exists in the two modes, so that the transceiver will be flexible in frequencies from 4.5 to 5GHz. In the RX, the two modes share the LNA, tunable LPF, and VGA. Similarly, the two modes of TX share the VGA and reconfigurable PA. The proposed transceiver was prototyped using a 0.15-μm E-mode GaAs pHEMT process. The RX exhibits gain range of 7.3 to 41.9dB, gain step of 1dB, tunable instantaneous bandwidth from 1 to 4.2GHz. The TX demonstrates gain ranging from -2.1 to 30.4dB and output 1dB compression point of 18.8dBm. The chip occupies 79.8-mm^2 area including padframe.**

***Keywords*—wideband transceiver, dual-mode, tunable bandwidth, reconfigurable power amplifiers.**

I. Introduction

Multi-octave band transceivers (TRXs) are essential for software defined radios, instrumentations, spectrum sensing, wideband imaging systems, multi-standard communications, etc. Conventional measures to realize RF front-ends for the above systems are taking use of discrete circuit modules with integrations on board levels. Due to its process stability, performance features and environmental tolerance, III-V process is greatly proper for such discrete MMICs. However, it encounters great difficulties in realizing higher circuit integration level when using III-V technologies (e.g., GaAs), especially for the monolithic multi-octave band transceivers. Different from silicon technologies, highly integrated transceivers in III-V technologies were rarely reported.

To date, some of remarkable literatures focus on ultra-wideband receiver (RX) or transceiver (TX). A RX with bandwidth for 0.1 to 40 GHz is reported in [2], in which a peak staggering LNA and a symmetric distributed drain mixer are deployed. The work achieves an impressive bandwidth, and it can be used in zero-IF receiving systems. But it contains merely a LNA and a mixer, which means its integration levels and functions will be limited. Another monolithic integrated RF front-end is presented in [5], using 0.5 μm InGaAs E/D-mode p-HEMT process. It realizes dual-frequency mode functions, i.e., 2.4-to-2.5GHz and 3.4-to-3.6GHz. However, it only supports direction-mode transmitting and receiving, which means it contains LNAs and PAs but with no mixer.

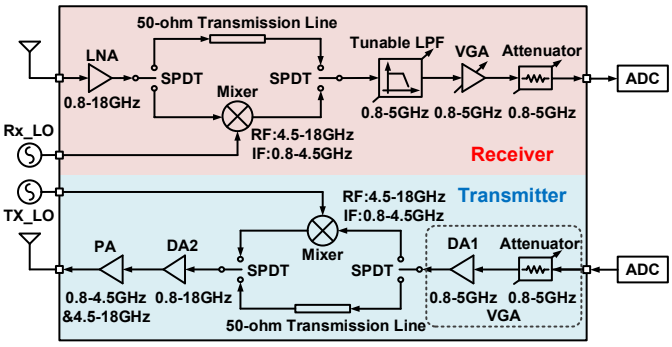

Fig. 1. The simplified structure block diagram of the proposed transceiver.

Classical works on silicon technologies can be found in [3, 4]. A 0.7-to-5.7 GHz reconfigurable direct-conversion RX is proposed in [3]. [4] describes a 0.1-to-5 GHz reconfigurable TX. Both works realize double operation mode at different frequency bands. However, for silicon circuits, the bandwidth and key performance are limited by the processes, thus impede their applications on multi-octave band systems.

In this paper, a monolithic 0.8-to-18GHz reconfigurable dual-mode TRX front end is proposed, covering applications from L to Ku bands. The proposed TRX can be configured into either direction mode or conversion mode. It can support direct transmitting and receiving, single heterodyne architecture, superheterodyne architecture, (i.e., cascading one more up-and-down conversion modules), etc. In the direction mode, the transceiver handles the signals from 0.8 to 5 GHz. In the conversion mode, it converts the signals up or down in a frequency range from 4.5 to 18 GHz. There is an overlap of 0.5 GHz existing in the two modes of this work, enabling the chip functional at the vicinity of the two modes. Architecture of the proposed TRX front end is illustrated in Fig. 1. In the RX, a 0.8-to-18 GHz distributed LNA is utilized as the first stage to achieve low noise performance, ultra-wideband SPDTs are used to switching signal following paths. In the RX, the two operation modes share the usage of the LNA, LPF and VGA. Here, the LPF is designed to be tunable which is used to alter instantaneous bandwidths, while the VGA performs gain adjustment to cater for different power levels. In the conversion mode, the down converter is realized by a double-balanced mixer, which benefits on even harmonic rejections. In the TX, a 0.8-to-18GHz PA is proposed using reconfigurable bias inductors topologies, which can enhance power efficiencies for broadband operations; followed by a DA and a VGA to handle

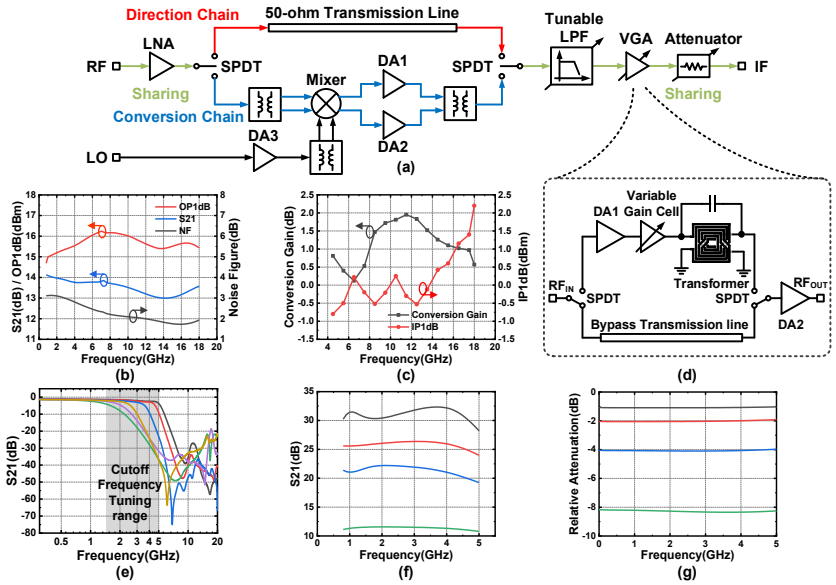

Fig. 2. (a) Receiver structure; (b) S21, OP1dB and NF of LNA; (c) conversion gain and IP1dB of down-conversion mixer; (d) VGA structure; (e) S21 of tunable LPF; (f) main gain levels of VGA; (g) attenuator control.

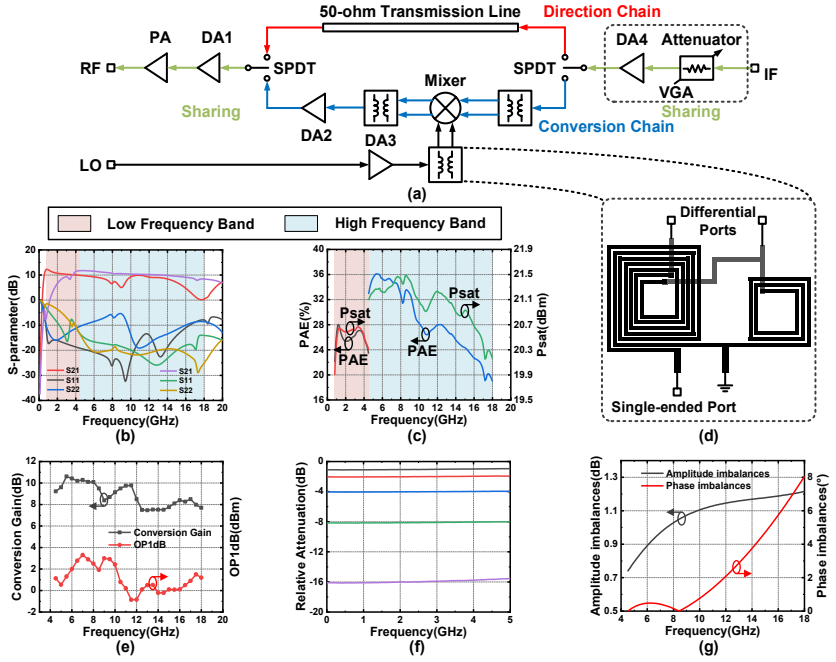

Fig. 3. (a) transmitter structure; (b) S-parameter of PA; (c) large-signal simulation of PA; (d) Balun structure; (e) conversion gain and OP1dB of up-conversion mixer; (f) attenuator control; (g) simulation of balun.

signal amplitudes. Similarly with the RX, a double-balanced mixer is used for up-conversion. The TRX was prototyped using 0.15 μm E-mode GaAs pHEMT technology, and it occupies 79.8-mm^2 area including padframe.

II. Receiver Design

Fig. 2 shows the design architecture of RX as well as detailed simulation results. The LNA locates at the first stage instead of RF switches, so that the noise figure of RX can be optimized. It adopts distributed structure to realize broadband low-noise performance. SPDTs are used to realize path alternations for direction mode and conversion mode. Two modes share the usage of the distributed LNA, the tunable LPF and the VGA.

In the direction mode, the signal enters a tunable passive LPF direct through a 50-ohm transmission line. The LPF utilizes switched capacitor arrays and parasitic capacitance of transistors to achieve coarse and fine bandwidth adjustments. Fig. 2d shows the architecture of VGA, it is proposed with heterogeneous chains. The VGA consists of two distributed amplifiers, a variable gain cell, a transformer, and an attenuator. The proposed heterogeneous chain topology leads to fine

linearity overall all different gain steps, whereby the attenuator is responsible for 1-dB step resolution.

In the conversion mode, the RF signal is converted into intermediate frequency (IF) signal by the down-conversion mixer, and then entered into the tunable LPF. The mixer core adopts a double-balanced topology in order to suppress the even harmonics. Here, to realize single-to-differential transformations of LO, RF, and IF signals, Ruthroff baluns are used, which is also suitable for on-chip integration. Driven amplifiers (DAs) are designed using distributed topology to extend bandwidths, which are used to maintain a proper LO and IF signal levels. Thanks to the DAs, requirements of outside LO power level can be relaxed, and the conversion gain can be increased.

The simulation results of the distributed LNA are shown in Fig. 2b. From 0.8 to 20 GHz, the gain is larger than 13 dB, where the fluctuation is less than 1.2 dB. The simulated noise figure (NF) is less than 3.2 dB and the output 1-dB compression point (OP1dB) ranges from 14.6 to 16.3 dBm. As depicted in Fig. 2e, the cut-off frequency of the tunable LPF varies from 1.8 to 5 GHz and the insertion loss is less than 1.3 dB. Fig. 2c presents conversion gain and input 1-dB compression point (IP1dB) of the down-conversion mixer. The conversion gain ranges from 0.12 to 1.95 dB, and the IP1dB varies from -0.5 to 2.2 dBm. Fig. 2f demonstrates the coarse gain steps from 11.6 dB to 32.3 dB. The attenuator in the RX is 4-bit digitally controlled, where the cells is of 1-dB, 2-dB, 4-dB and 8-dB resolutions. The Fig.2g shows the results of fine gain steps.

III. Transmitter Design

Fig. 3a shows the structure of TX. In the TX, the VGA consists of a fixed gain distributed amplifier and a 5-bit attenuator. Similarly, SPDTs are used to enable switching between direction and conversion modes, while the attenuator attains 1-dB step resolution. The two modes share the usage of the VGA and the PA.

In direction mode, the signal flows through a 50-ohm transmission line, and then enters the DA and the PA. The PA is designed to be frequency reconfigurable using switched bias inductors, hereby the broadband matching and power efficiency can be improved.

In conversion mode, the IF signal is converted into RF signal via the up-conversion mixer, and enters the DA and the PA. The structure of the up-conversion mixer is similar to that of the down-conversion mixer. The DA with distributed topology is used to drive the LO signal and amplify the RF signal.

Simulated S-parameters of the reconfigurable PA are displayed in Fig. 3b. In the low frequency band from 0.8 to 4.5 GHz, its gain is larger than 9.8dB; in the high frequency band from 4.5 to 18 GHz, the gain is better than 7.8dB. Fig. 3c illustrates the large-signal simulations of the broadband reconfigurable PA. In the low frequency band, power added efficiency (PAE) ranges from 22.0% to 28.0% and saturated output power (Psat) ranges from 19.9 dBm to 20.7 dBm. In the high frequency band, PAE ranges from 18.9% to36.1% and Psat ranges from 20.1 dBm to 21.5 dBm. Fig. 3e shows the conversion and OP1dB of the up-conversion mixer. The conversion gain ranges from 0.12 to 1.95 dB, and the IP1dB varies from -0.5 to 2.2 dBm. The suggest wideband balun is demonstrated in Fig. 3d. As revealed by the Fig. 3g, the balun keeps phase and amplitude imbalances under control well. Compared with the attenuator in the RX, a 16dB attenuation cell is added in the transmitter. Fig. 3f shows the effect of each attenuator cell with 1-dB, 2-dB, 4-dB, 8-dB and 16-dB steps.

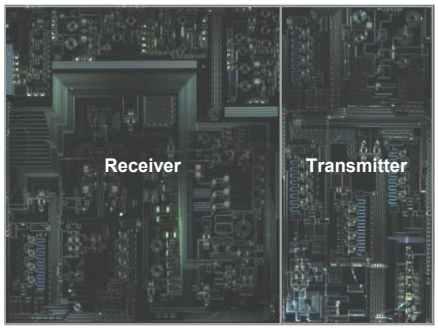

Fig. 4. Die micrograph of the proposed transceiver.

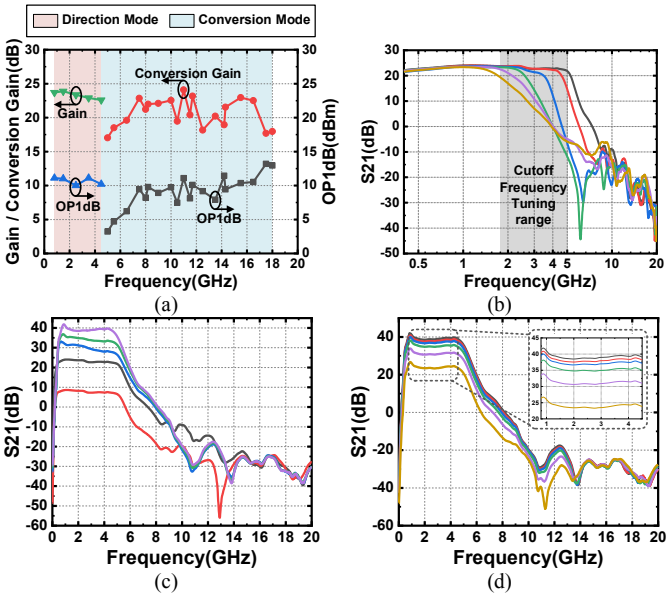

Fig. 5. Measured data of the receiver: (a) Gain, Conversion Gain and OP1dB; (b) Cutoff frequency variation range; (c)Gain variation range; (d) attenuator gain control steps.

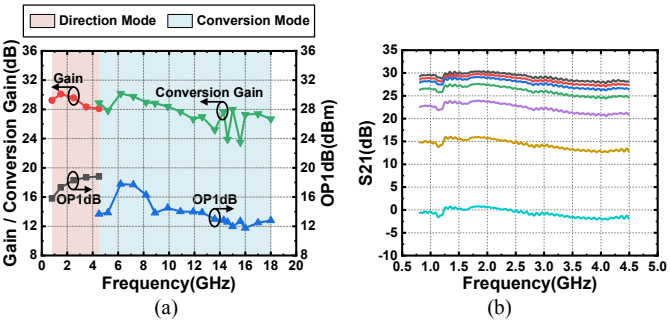

Fig. 6. Measured data of the transmitter: (a) Gain, Conversion Gain and OP1dB; (b) Gain variation range.

Table 1. Performance summary and Comparison with previously published receiver/transmitter

	This work	[1]	[2]	[3]	[4]	[5]
Architecture	Transceiver	Transceiver	Receiver	Receiver	Transmitter	Transceiver
Function	Direction & Conversion	Direction	Conversion	Conversion	Conversion	Direction
RX Freq./GHz	0.8-18	3.4-5.4	0.1-40	0.7-5.7	-	2.4-2.5/3.4-3.6
RX BW/%	183	45	199	156	-	4/6
RX Gain/dB	41.9	26.8[1]	16	41	-	11.2
RX Gain dynamic range/dB	34.6	-	-	-	-	-
RX NF/dB	4-4.4	5.1-6.1	3.4-4.2[1]	5.5-11.1	-	2.5
RX Pdc/mW	716	13.5	415	77-139	-	15
RX instantaneous BW /GHz	1-4.2	-	-	-	-	-
TX Freq./GHz	0.8-18	3.4-5.4	-	-	0.1-5	2.4-2.5/3.4-3.6
TX BW/%	183	45	-	-	192	4/6
TX Gain/dB	30.4	N.A.	-	-	-	25
TX Gain dynamic range/dB	32.5	-	-	-	-	-
TX OP1dB/dBm	11.75-18.8	20[2]	-	-	19	25.5/32.9
TX Pdc/mW	996	306	-	-	161.4-391.1	3720/547.8
Area/mm^2	79.8	6.03	1.89	0.53	6.6	70
Technology	0.15um GaAs	65nm CMOS	0.15um GaAs	22nm FD-SOI CMOS	65nm CMOS	0.5um InGaAs

[1]LNA test result. [2] PA Psat.

IV. Measurement Results

The proposed transceiver is implemented in a 0.15-μm GaAs pHEMT technology and occupies an area of 7.6×10.5 mm^2. The die micrograph is shown in Fig. 4.

Measurement results of the RX are shown in Fig. 5. In the direction mode (see Fig. 5a), the OP1dB ranges from 10 dBm to 11.1 dBm, the gain fluctuates within the range of 22.6 dB to 23.7 dB. In the conversion mode, the OP1dB ranges from 3.2 dBm to 13.2 dBm, and correspondingly the conversion gain is from 17.0 dB to 24.0 dB. Fig. 5b shows the cutoff frequency varies from 1.8 to 5 GHz, which is controlled by the tunable LPF. The gain of the RX can be varying from 7.3 dB to 41.9 dB, see Fig. 5c. Attenuator with different gain steps are measured in Fig. 5d, where the minimum step is 1 dB. The measured NF is from 4 to 4.4 dB within the whole bandwidth.

The measured results of TX gain, conversion gain and OP1dB are shown in Fig. 6a. In direction mode, the OP1dB ranges from 15.8 dBm to 18.8 dBm, the maximum gain is 30.4 dB with fluctuation of 2.3 dB. In conversion mode, the OP1dB ranges from 11.75 dBm to 17.78 dBm, the gain is from 23.5 dB to 30.2 dB. Fig. 6b shows the gain tuning range. The maximum gain is 30.4 dB and the minimum gain is -2.1 dB. The gain tuning range is 32.5 dB and the gain fluctuation in all gain states is less than 3 dB.

Table 1 summarizes the work and compares it with the state-of-the-arts.

V. Conclusion

This paper presents a highly integrated dual-mode monolithic reconfigurable transceiver with of direction and conversion functions. It can support direct transmitting and receiving, single heterodyne architecture, superheterodyne architecture, (i.e., cascading one more up-and-down conversion modules), etc. The design architecture, detailed topologies, simulations, and measurements are discussed. The works is prototype using a GaAs process. It works in frequencies from 0.8 to 18 GHz with 4.5 octave bandwidth. To the best of the authors' knowledge, the work is with the highest integration level in GaAs technology, and will greatly meaningful for instrumentations, spectrum sensing, wideband imaging systems, multi-standard communications, etc.

References

[1] X. Xiao et al., "A 65-nm CMOS Wideband TDD Front-End With Integrated T/R Switching via PA Re-Use," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, pp. 1768-1782, July 2017.

[2] J. Hu and K. Ma, "Analysis and Design of a Broadband Receiver Front End for 0.1-to-40-GHz Application," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2393-2403, June 2021.

[3] S. Golabighezelahmad, E. A. M. Klumperink and B. Nauta, "A 0.7–5.7 GHz Reconfigurable MIMO Receiver Architecture for Analog Spatial Notch Filtering Using Orthogonal Beamforming," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 5, pp. 1527-1540, May 2021.

[4] Y. Yin, B. Chi, Y. Gao, X. Liu and Z. Wang, "A 0.1–5.0 GHz Reconfigurable Transmitter With Dual-Mode Power Amplifier and Digitally-Assisted Self-Calibration for Private Network Communications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 11, pp. 3266-3277, Nov. 2014.

[5] P. -H. Wu, S. -M. Wang and M. -W. Lee, "Wi-Fi/WiMAX dual mode RF MMIC front-end module," *2009 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2009, pp. 289-292.