High Sensitivity RF Energy Harvesting System with Self-calibrate Network

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***Abstract*—An effective codesign methodology of high sensitivity RF energy harvesting (RFEH) system for passive IoT applications is proposed, and chip implementation based on this solution was fabricated in standard TSMC 180 nm CMOS technology. By this systematic approach, a RFEH system including antenna, rectifier, power management unit (PMU) and impedance self-calibrate network were adopted to achieve an excellent sensitivity performance, which is characterized not only by high-Q factor but also large bandwidth. This work achieved high sensitivity performance of -32 dBm in 920~925 MHz for 0.7 V output voltage in anechoic chamber environment. Moreover, it can be powered by 36 dBm effective-isotropic radiated power source at a distance of 68 m outdoors.**

***Keywords*—RFEH, high sensitivity, Automatic calibration, low power, passive Internet of Thing (IoT).**

I. INTRODUCTION

With the wide coverage range of 5G networks, passive IoT technology has developed rapidly in recent years due to the advantages of low deployment and maintenance costs, flexible application scenarios, and networking with greater range of coverage. Compared with the traditional structure, passive IoT system based on bistatic backscatter communication shown in Figure 1 could greatly expand the uplink distance of the data transmission and the coverage area of a single receiver. In addition, as another key specification of the system, the range of the RF power source to the passive nodes directly determines the cost of system deployment, which is this research working on. The proposed RFEH system aims at maximizing the range of coverage (d1) of a single RF source, that is, optimizing the sensitivity as high as possible. What is noteworthy is that the work adopts RF energy source as the energy source of the IoT terminal chips. As widely used passive IoT nodes power source, RF energy source not only meets the demand of low cost, but also could realize data transmission of network system.

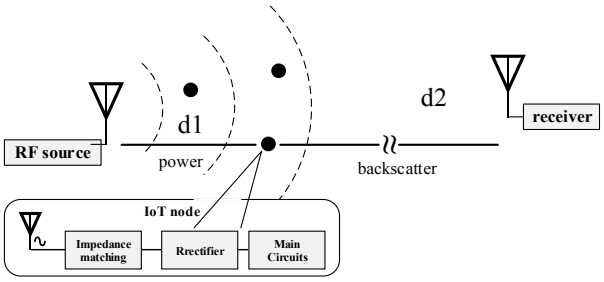


Fig. 1. The structure of the passive IoT.

High sensitivity means that the incident power received by the chip is very small. In order to overcome the imbalance between the high sensitivity requirements and relatively high power consumption of the sensing chips (around 10 to 100 uW) [1]. A duty cycle working mode at IoT nodes was adopted by introducing off-chip energy storage capacitor and PMU, which achieves the separation of energy harvesting and power consumption of main circuits in time. To some extent, this solution trades charging time for sensitivity, which is applicable to passive environment IoT scenarios with low time-efficiency requirements.

Over the years, there are various rectifier structures and design method have been reported to improve the energy conversion efficiency and sensitivity [2]-[7], such as the energy harvesting circuits based on rectifier and antenna co-design method, which can achieve adaptive impedance matching in a certain range, and so on. Different from these reports, the design approach of RF energy harvesting system proposed in this work elevates the design of the antenna, rectifier circuit, PMU and automatic impedance regulating unit to a joint analysis at the system level. Although High-Q design can achieve higher sensitivity, which are susceptible to impedance mismatch due to process, power variations and so on. In this work, a fully integrated self-tuning network is presented, which automatically calibrate the impedance deviation between the rectifier and the antenna. Therefore, the proposed RFEH in this paper has both high sensitivity and large bandwidth. The measurement results illustrate that the RFEH system based on this solution not only achieves ultra-high sensitivity, but also ensures the simple structure, low cost and high robustness.

II. DESIGN STRATEGY AND CIRCUIT IMPLEMENTATION

A. Sensitivity analysis

Figure 2 shows the system block diagram of the RFEH, which is composed of antenna, rectifier, energy storage capacitor, impedance self-tuning network and PMU. As we all know, high sensitivity performance means the available power output of the antenna must be minimized while the rectifier antenna port voltage Vant reaches the rectifier power-up threshold voltage. Therefore, the linear model of the antenna rectifier interface will first be studied in this work. The linear model of ant-chip interface intuitively equates the antenna as a series of AC voltage source, radiation resistance and inductor, and the chip as a parallel connection of resistance and capacitance. Taking into account a conjugate matching between the antenna and the chip, the output power of the

antenna under the model is given by the following analytical expression:

$$\boldsymbol{P_{av}} = \frac{\left(\frac{V_{ANT}}{\sqrt{2}}\right)^2}{R_P} = \frac{\left(\frac{V_{ANT}}{\sqrt{2}}\right)^2}{R_S + \frac{X_S^2}{R_S}} \approx \frac{R_S\left(\frac{V_{ANT}}{\sqrt{2}}\right)^2}{X_S^2} \quad (1)$$

where R_S and X_S are the real part and imaginary part of the chip impedance respectively. The Q factor of rectifier and the resonator composed of antenna and rectifier is defined by the following formula

$$\boldsymbol{Q_{rec}} = \frac{X_S}{R_S} \quad (2)$$

$$\boldsymbol{Q_{sys}} = \frac{1}{Q_{rec}} + \frac{1}{Q_{ant}} \quad (3)$$

From the above formulas, it can be concluded that the key point to achieving high sensitivity is to increase the Q factor of chip input impedance while maintaining low R_S.

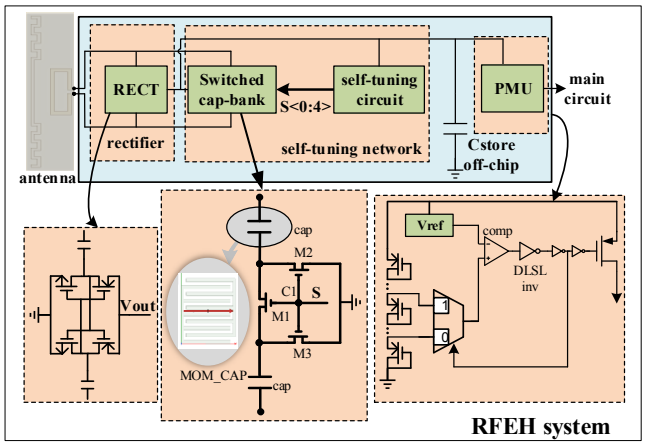


Fig. 2. The structure of the RFEH system in this work.

For the design of the RFEH system, there are several parameters that need to be compromised at the system level. First, considering the conjugate matching between the antenna and rectifier with high-Q factor discussed in previous section, the antenna also needs to be high-Q characterized. Inductively coupled loop (ICL) dipole antenna, this structure can realize higher inductance under lower radiation resistance, has been widely used in UHF EH. For this reason, the ICL antenna structure was chosen in the work. Additionally, FR4 substrate material was adopted to satisfy the requirement of cost control in commercial applications. However, FR4 substrate limits the Q factor of antenna (generally below 40), which means that it is hard to reduce the radiation resistance to very small, otherwise the gain and efficiency of the antenna will deteriorate rapidly. That is to say, the smaller Q value of antenna cannot fully match the optimized larger value of chip (around 100), which requires a compromise design between the system Q factor and antenna characteristics such as gain and efficiency.

B. Rectifier and implementation

A fully differential driven cross-coupled rectifier is adopted as shown in Fig 2. The electrical characteristics of the rectifier include input impedance, boost coefficient (which is defined as the ratio of rectifier output voltage V_{RECT} to input voltage Vant), charging time and power conversion efficiency (PCE). Among these parameters, the optimization of input impedance is particularly critical, which determines the optimal sensitivity that can be attached when the antenna resonates with the rectifier. Similarly, this value also needs co-designing with the antenna. Besides, it is worth putting out, PCE is not considered as the most important specification in this design, because the load current of rectifier is very small when charging in duty cycle mode. The rectifier circuit design aims at reaching the output voltage requirements at low power, by optimizing the transistor size W, L, and series stage N. The minimum transistor length was selected to reduce parasitic capacitance and on-resistance. Moreover, the transistor width W is closely related to the impedance due to its contribution to capacitance, boost coefficient and charging time. Therefore, W also needs to be carefully designed. If the W value is too small, the impedance imaginary part will be too large and the antenna cannot match it. Meanwhile, boost coefficient of the rectifier will be descend and charging time will be increase significantly because on-resistance of the transistor is too large. Therefore, the value of W combined with other parameters of the system was iteratively optimized for several times to achieve optimal performance. The series stage N also has an impact on the impedance and charging time, but more consideration is to reach the target output voltage through cascades. The N value should not be too large in the single well process, generally 4 or 5 stages, which is due to the low boost coefficient caused by the body effect of the rear stage rectifier.

C. Self-calibrate network implementation

From the previous analysis, the antenna and rectifier must form a high-Q resonator to obtain high sensitivity performance, which will result in a very small bandwidth. It means that resonant frequency is susceptible to impedance mismatch due to process, manufacturing and packaging dispersions, which will lead to deterioration of system robustness. The previous work has verified the feasibility of capacitor bank adjustment, but its adjustment module was either operated off-chip or powered by external power supply, and the start-up voltage and power consumption are large, which cannot be started with impedance mismatch [1] [9].

To improve the tolerance of the resonator for impedance mismatch, a fully integrated impedance self-tuning network is presented, which automatically calibrate the impedance deviation between the rectifier and the antenna by adjusting the 5-bit binary-weighted switched capacitor bank parallel to the rectifier through a feedback control loop. The feedback control loop selectively joins the capacitor bank by detecting the change of V_{RECT} to adjust the reactance part until V_{RECT} is detected to reach the maximum value, and the control loop locks the current capacitor bank state to complete the automatic correction of impedance deviation. Its architecture and low-power feedback control algorithm flow are shown in Figure 3. When the RFEH starts to work, first, once the output

voltage V_{RECT} is detected to be stable and reaches the start-up voltage of the circuits, the feedback control loop under the clock driving will be enabled by V_{EN1}. The timing adjustment circuit starts working when the rising edge of V_{EN1} arrives and is used to generate a pair of non-crossover clocks, namely the sample hold clock CLK_{SH} and the comparison clock CLK_{CO}, where the comparison clock is one clock cycle ahead of the sample clock. When the count enable signal V_{EN2} arrives and starts to change, the count signal V_{COUNT} adds one for the first time, the sampling comparison circuit compares the V_{RECT} twice, and so on until the V_{RECT} is detected to decrease, generating the adjustment end enable signal V_{EN3} that closes the impedance adaptive adjustment module, and latching the data to end the self-tuning process. When the adjustment is finished, the counter output vector is locked and the clock block is cut off to save power. At this time, the antenna and rectifier reach the best impedance matching state at the operating frequency. The capacitance array is consist of MOM capacitor with the same layer metal insert finger structure, and the minimum capacitance value is 5 fF. The frequency of the clock is 1 KHz in this work, which is depends on the stabilization time of the output voltage at the lowest input power. Power consumption of the whole network is less than 10 nW.

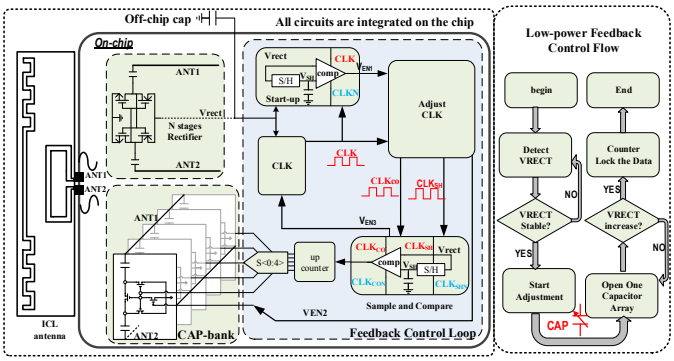


Fig. 3. The structure of the RFEH system in this work.

III. Measurement Results

Fig.4. is micrograph of the chip. The chip implementation was fabricated in the TSMC 180 nm CMOS technology，connected via bonding to the test board without package assembly. The antenna was also integrated on the FR4 board. First of all, the sensitivity specification was measured in the anechoic chamber environment, as shown in Figure 5(a). The RF source was connected to the linearly polarized TR antenna and the RFEH was measured at a distance 2m from the TR antenna. The Figure 5(b) illustrates test output voltage and PCE in 922.5 MHz, with load resistances 10 MΩ and 100 MΩ respectively. According to the measurement results, the sensitivity of the EH system is -32dBm for 0.7V output with PMU load only, where there is a deviation of 1~1.5dBm from the simulation result due to various non-ideal parasitic effects. In addition, the PCE is relatively small because the load current of the rectifier is as small as tens of nanoamperes under steady-state conditions. Then, the work measured the farthest distance of the RF source to power up the chip outdoors to simulate the actual application environment of the passive IoT nodes, as shown in Figure 6. The experimental results indicates that the 36 dBm power source could power up the chip beyond 68m, which means that the coverage area of a single RF source could be as large as 14500 m ².

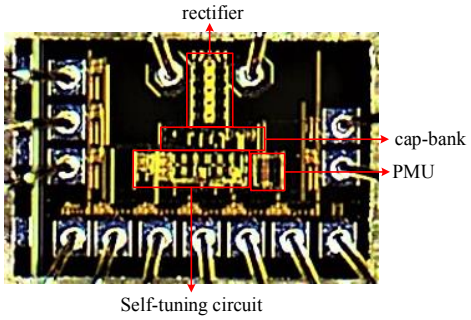


Fig. 4. Micrograph of the chip

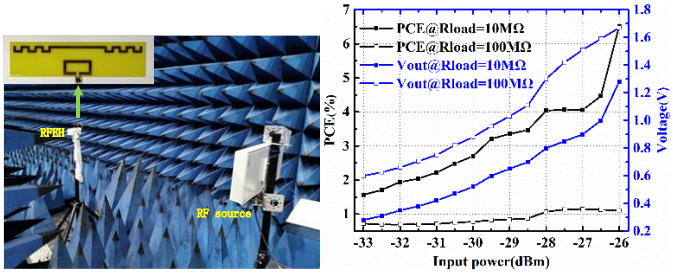


Fig. 5. (a)Test environment in anechoic chamber. (b)Measured sensitivity and power conversion efficiency of the RFEH system.

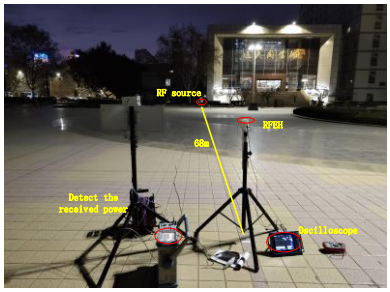
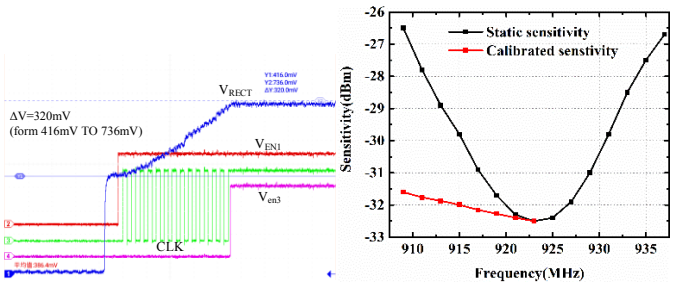


Fig. 6. Test environment outdoors with 36dBm RF power source.

In the end, a slight mismatch is introduced into the antenna to measure the impedance self-tuning network in the system with high-Q factor. The key signals and expansion of bandwidth are shown in Figure 7, and the average power consumption is 8 nW. From the results, the self-tuning network starts when the V_{RECT} is 433 mV, then the control loop starts to work and drives the switch to connect the capacitor to the modulating impedance after the voltage is stabilized. The antenna and chip matched well after 28 adjustment cycles, at which time the output voltage is 732 mV. What's more, multiple tests were carried out with slightly mismatched antennas with different degrees, and the results are shown in Figure 7(b), which demonstrates that network

can greatly expand system bandwidth. Consistent with our design, when the system starts to work, the capacitance continues to increase, so it is only effective on one side. The slight decrease in sensitivity is caused by the insertion loss of the switched capacitance. Table 1 is comparison between this work to already proposed RFEH.



(a) (b)

Fig. 7. (a)The key signals of self-calibrate network. (b) Expansion of bandwidth due to impedance self-calibrate well.

Table 1. Comparison between the proposed RFEHS.

Reference	this work	[4]	[8]
process	180 nm	90 nm	180 nm
frequency	904.5 M	915 M	915 M
sensitivity	-32 dBm	-27 dBm	-14.8 dBm
tunable	co-design & tunable	co-design & tunable	co-design
condition	0.7 V@10 nA	1V@n/a	2.4 V@1 uA

IV. Conclusion

An effective design approach of high sensitivity RFEH system with impedance self-tuning network for passive IoT nodes has been presented, which is based on CMOS differential-drive rectifiers and ICL antennas implemented on FR4 printed board. The approach focuses on the design of both antenna and rectifier, and jointly optimizes them as a whole system to improve the RFEH sensitivity as high as possible. This approach is implemented in standard TSMC 180 nm process, and the experimental results demonstrated that state-of-the-art sensitivity is achieved at 922.5 MHz. Measurements in an anechoic chamber show the sensitivity is -32dBm at the target voltage of 0.7 V. Outdoors, the same voltage could be generated from a 4 W RF source at more than 60 m distance. In addition, the system has a high tolerance for impedance mismatch. This work makes the passive IoT system with large coverage becoming a reality.

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