A 26-32GHz Differential Attenuator with 0.23dB RMS Attenuation Error and 11.2dBm IP1dB in 40nm CMOS Process

An Sun[#], Junjie Gu[#], Hao Xu[#1], Weitian Liu[#], Kefeng Han[$], Rui Yin[#], Zongming Duan[*], Hao Gao[^], Na Yan[#2]

[#]Fudan University, China
[$]Jiashan-Fudan Joint Research Institute, China
[*]East China Research Institute of Electronic Engineering, Anhui, China
[^]Eindhoven University of Technology, the Netherlands
[1]haoxu@fudan.edu.cn, [2]yanna@fudan.edu.cn

***Abstract* — This paper presents a 26-32GHz 6-bit differential attenuator in 40nm CMOS process. This attenuator adopts an optimized cascade scheme that incorporates simplified T-type (ST-type), T-type and Π-type attenuator units. Driven by a complete analysis of the pole-zero pattern introduced by the compensation capacitor, the design achieves a state-of-art uncalibrated RMS attenuation and phase error. The design methodology of shunt branches for constant phase and cascade linearity enhancement achieves a high linearity while minimizing the phase variation across the whole frequency band. The attenuator achieves a 31.5dB attenuation range with 0.5dB step and -8.5 to -9.5dB insertion loss in a compact area of 0.54mm×0.23mm. The measured RMS attenuation error remains below 0.23dB without calibration and phase error is less than 5.58°. IP1dB in the reference state is better than 11.2dBm across 26–32GHz.**

***Keywords* — mm-wave, CMOS, differential attenuator, phase compensation, attenuation/phase error, linearity.**

I. Introduction

Phased array transmitters have been widely employed in satellite communication systems that often occupy Ka/K bands. Accurate gain control and phase synchronization are among the key requirements in phased array applications. Whereas the variable gain amplifier provides accurate gain control, its tuning range and bandwidth are usually limited. Excessive gain tuning in active amplifiers may lead to large phase variations. This calls for the need of attenuators, which along with the variable gain amplifier, achieve the necessary gain tuning.

While the switching path attenuator exhibits low phase error, its loss grows with the number of attenuators, which limits its use in high dynamic range applications [1]. The distributed attenuator has lower loss, but is only suitable for small attenuation bits [2]. At the cost of area, the switch-T or Π-type attenuator simultaneously achieves low phase error and low insertion loss by utilizing inductive compensation [3]. Compared to inductive compensation, capacitive compensation exceeds in area without sacrificing key performances [4]. Specifically, tail-capacitor compensation further expands the operation range to higher frequencies, yet it is mostly used in narrowband applications so far [5].

This paper presents a 6-bit differential attenuator with capacitive compensation in 40nm CMOS process. Differential

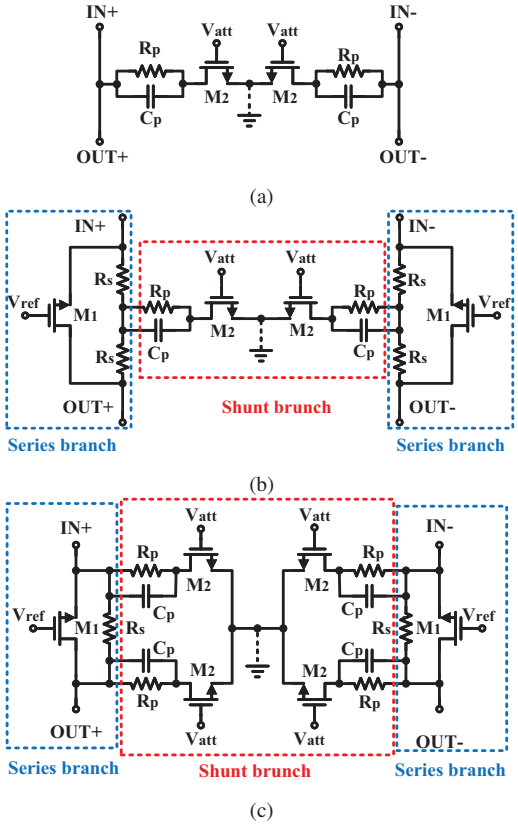


Fig. 1. Differential (a) simpified T-type; (b) T-type; (c) Π-type attenuator unit with capacitive compensation.

configuration is adopted to minimize the performance degradation caused by bond wires. Driven by the analysis of pole-zero patterns, the capacitive compensation scheme is optimized to achieve a low attenuation/phase error without calibration. Its high linearity is ensured by the optimum cascading order of the attenuation units.

II. Circuit Optimization and Implementation

A. Attenuator Units with Capacitive Compensation

Three different types of attenuator units are utilized in this work for different purposes. The simplified T-type attenuator,

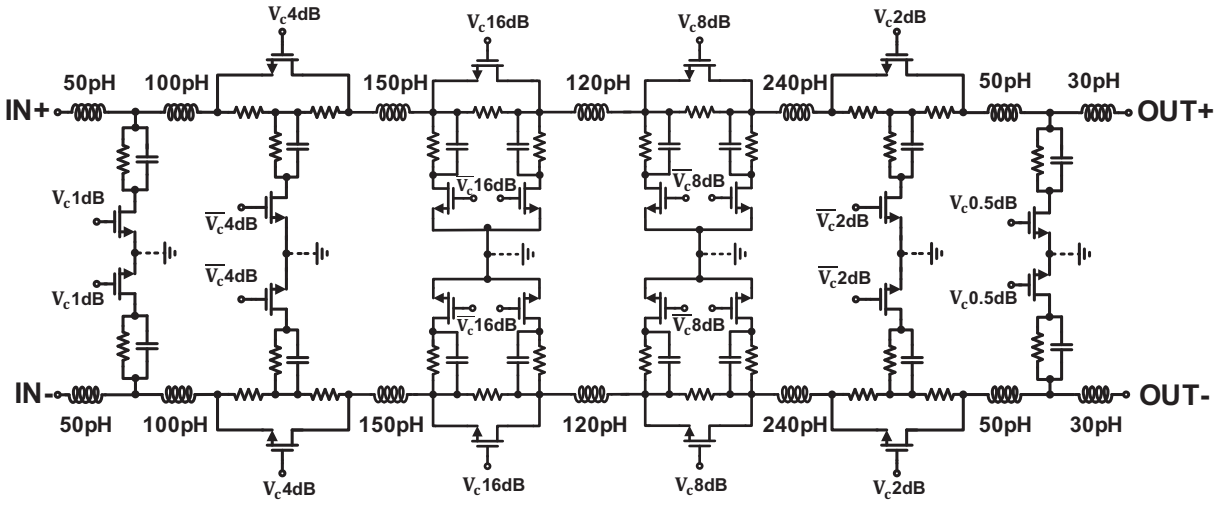
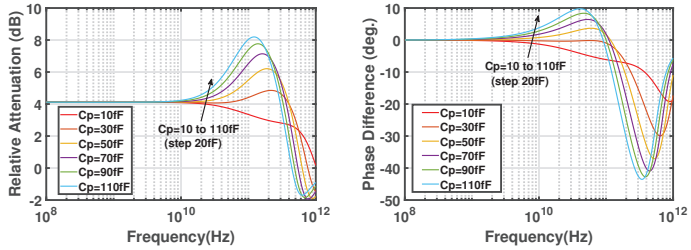


Fig. 2. Schematic of the proposed differential 6-bit attenuator.



(a) (b)

Fig. 3. (a) Simulated relative attenuation and (b) simulated phase difference of the 4dB T-type attenuator unit.

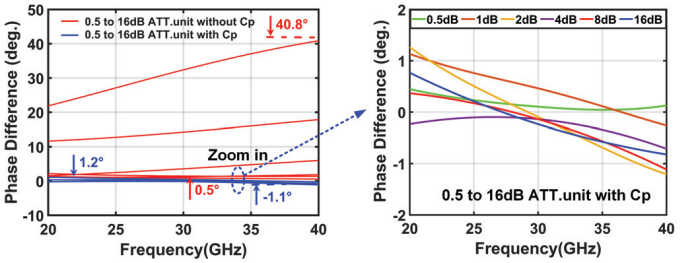
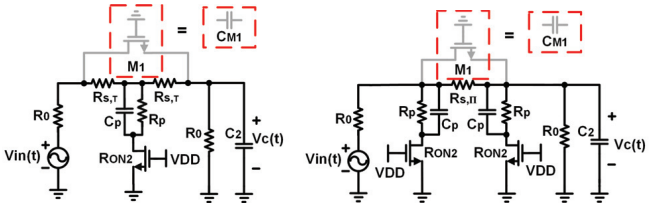


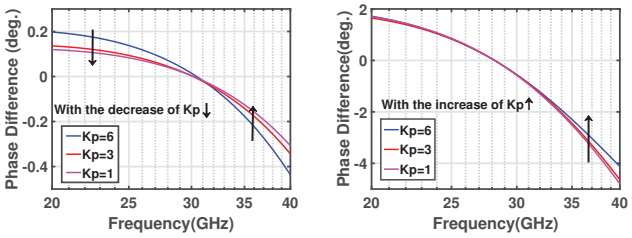
Fig. 4. Simulated phase difference of attenuator units with/without C_p.

essentially a one-port impedance that minimizes the insertion loss as shown in Fig.1(a), provides fine attenuation control with 0.5/1dB step. The T-type attenuator as shown in Fig.1(b) offering good matching is used in 2/4dB attenuator units. Units of larger attenuation weights utilize the Π-type attenuator as shown in Fig.1(c) for accurate attenuation control. Shown in Fig.2 is the overall attenuator that adopts a fully differential configuration with common-mode ground termination in each attnuator unit to suppress potential common-mode excursions. In order to obtain low amplitude and phase variation between the reference state and other attenuation states, compensation capacitor [4] that creates pole-zero cancellation is inserted in each unit. The impact of the compensation capacitor is visualized in Fig.3, which compares the amplitude and phase response of the 4dB attenuator with C_p being increased from



(a) (b)

Fig. 5. (a) Equivalent circuits of the T-type attenuator in attenuation state; (b) Equivalent circuits of the Π-type attenuator in attenuation state.



(a) (b)

Fig. 6. Phase difference with different values of K_p for (a) the 4dB T-type attenuator unit and (b) the 16dB Π-type attenuator unit.

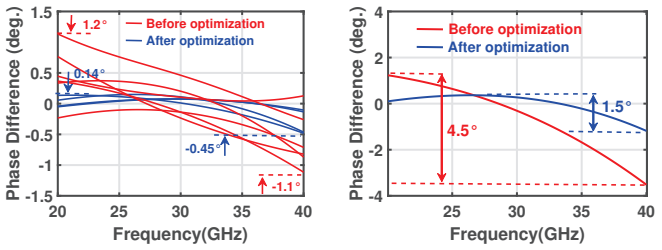
10fF to 110fF. The proper C_p leads to a flat in-band amplitude response with minimal phase variation, which is a direct outcome of pole-zero cancellation as shown in Fig.4.

B. Phase Stable Design Methodology in Shunt Branches

Instead of purely relying on C_p to control the frequency response, this work further expands the design space by adjusting the ratio of R_p/R_{ON2}, where R_p represents the linear resistor and R_{ON2} represents the on-resistance of the transistor in the shunt attenuation branch respectively, as shown in Fig. 5. Without loss of generality, we choose T-type attenuator unit to analyse the impact of K_p. The dominant pole and zero in in the T-type attenuator are defined as,

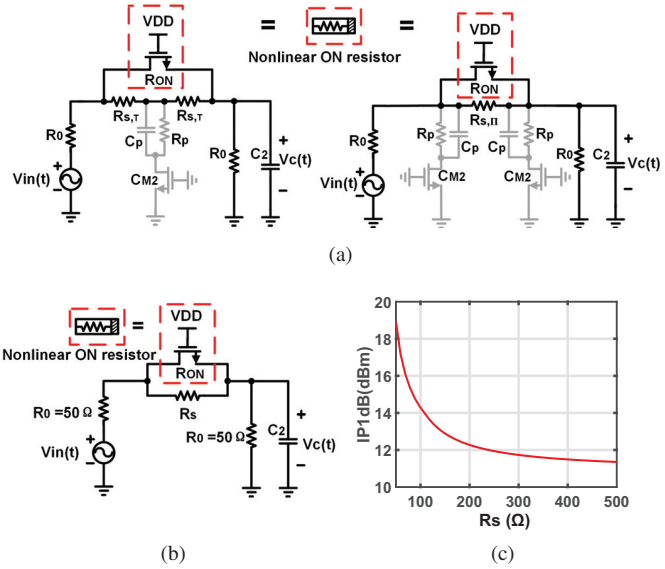
$$\omega_{z,T,Att} = \frac{K_p+1}{C_pR_p + C_{M1}(R_s^2/R_{ON2} + 2R_sK_p + 2R_s)} \quad (1a)$$

$$\omega_{p,T,Att} = \frac{R_s + R_0 + 2R_{ON2}(K_p+1)}{C_pR_{ON2}(R_sK_p + R_0K_p + 2R_p)} \quad (1b)$$



(a) (b)

Fig. 7. (a) The phase difference of each attenuator units before and after the optimization of K_p; (b) The maximum phase difference of the overall attenuator before and after the optimization of K_p.



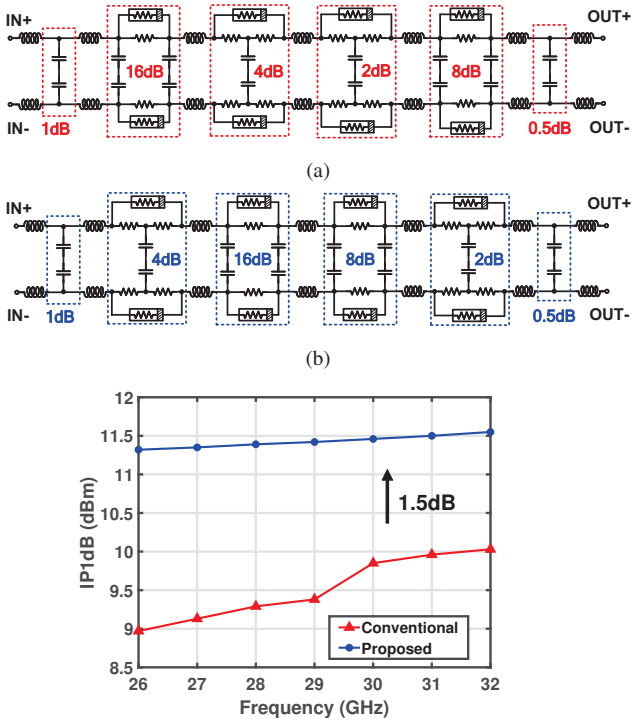
(a) (b) (c)

Fig. 8. (a) Equivalent circuits of the T/Π-type attenuator in the reference state; (b) Simplified equivalent circuits of attenuator units in the reference state; (c) Simulated IP1dB versus R_s.

where $K_p = R_p/R_{ON2}$ represents the resistance ratio controlled by design, and $R_0 = 50\Omega$ represents the source resistor and output termination resistor. The positions of the poles and zeros depend on both K_p and C_p. Compared with the conventional method of only adjusting the compensation capacitor C_p, K_p adds another degree of design freedom. While reducing K_p in the Π-type attenuator suppresses the phase variation, the T-type attenuator prefers a larger K_p for the same purpose as shown in Fig.6. This is a direct outcome of the duality between T-network and Π-network. $K_{p,i}$ in each stage is thus adjusted accordingly to achieve an overall flat frequency response as shown in Fig.7.

C. Cascading Order for Linearity Improvement

Based on the analysis of distortion in a passive FET-switch-based sampling circuit in [6], this paper follows the same approach to understand the linearity limit. Both T-type and Π-type attenuators have the same equivalent circuits in the attenuation state as shown in Fig.8. The nonlinear ON resistance of the series bypass transistor dominates the linearity



(a) (b) (c)

Fig. 9. (a) Conventional cascading order of the attenuation units; (b) Proposed cascading order of the attenuation units; (c) Simulated linearity comparison.

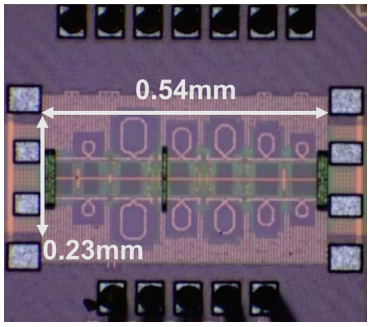


Fig. 10. Chip micrograph of the proposed 6-bit attenuator.

with its impact on compression point approximated as below,

$$A_{in,1dB} \approx \sqrt{0.145\frac{4(1+\beta V_{ov}R_s)^3}{\omega_0 n^2\beta^2 R_s^3 C_2}} \quad (2)$$

where $\beta = \mu C_{ox}W/L$, $V_{ov} = V_{DD} - V_{th} - nV_{DC}$, $n \approx 1.2$ represents the body effect and ω_0 is the input frequency. (2) reveals that the linear resistor R_s mitigates the impact from R_{ON} and linearity degrades with higher R_s. As the unit of higher attenuaton needs greater R_s, its linearity is always worse than the attenuator of lower attenuation. As the overall IP1dB of the attenuator is largely determined by the attenuation units closest to the input, we propose a modified cascading order that further improves the linearity compared to a similar previous work [8]. Fig.9 shows the difference in IP1dB between the two cascading orders for the same attenuation range and step. The proposed cascading order improves the linearity by at least 1.5dB across the frequencies of interests.

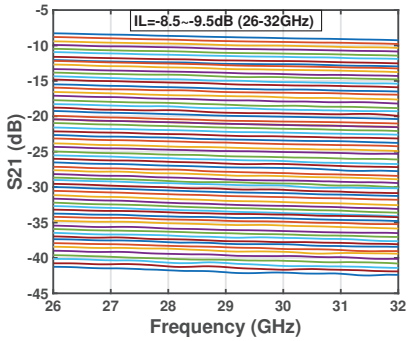
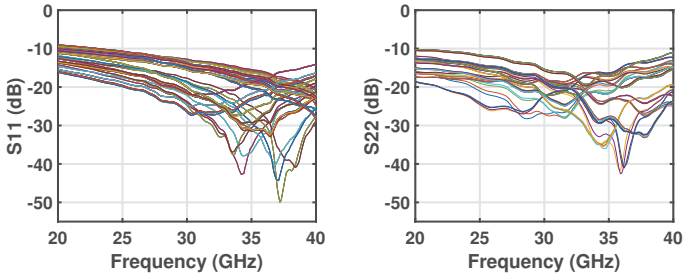


Fig. 11. Measured S21 across all 64 attenuation states.



(a) (b)

Fig. 12. Measured (a) S11 and (b) S22 across all 64 states.

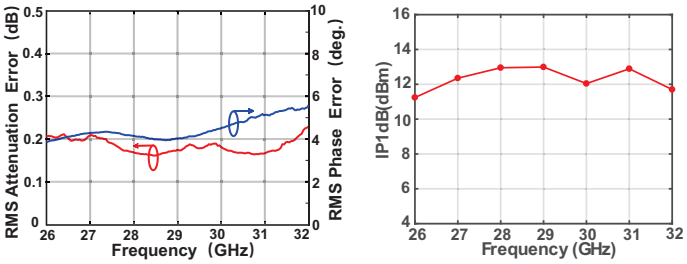
III. Measurement Results

The proposed 6-bit fully differential attenuator is fabricated in a 40nm CMOS process and the chip micrograph is shown in Fig.10. The core chip area is 0.124mm^2(0.54mm×0.23mm). The S-parameters of the attenuator are measured using GSSG probes. Fig.11 plots the measured S21 in all the attenuation states with the reference state insertion loss within -8.5 to -9.5dB across 26-32GHz. The return losses at the input and output port remain below –11.1dB as shown in Fig.12, which indicates good matching of the differential attenuator. Thanks to the applied compensation capacitor and optimization in the shunt branches, the measured RMS attenuation error is less than 0.23dB and the RMS phase error is better than 5.58° as shown in Fig.13(a). The IP1dB of the reference state is better than 11.2dBm across 26-32GHz as shown in Fig.13(b).

Table I compares the key performance metrics with state-of-art designs. The proposed design simultaneously achieves a very low attenuation error and high linearity in CMOS designs.

IV. Conclusion

In this paper, a 6-bit 26-32GHz differential attenuator is proposed. The employment of the capacitive compensation and optimization of the shunt branches lead to low RMS phase errors among different attenuation states. The cascading order of the attenuation units is refined based on the analysis that identifies the dominant source of nonlinearity. The measured results further validate the analysis and effectiveness of the design choices. The attenuator fabricated in a 40nm CMOS process achieves low RMS attenuation/phase error (<0.23dB/<5.58°) and high linearity (IP1dB>11.2dBm) within a compact area (0.124mm^2).



(a) (b)

Fig. 13. (a) Measured RMS attenuation error and phase error; (b) Measured IP1dB in the reference state versus frequency.

Table 1. Table of Comparison

	JSSC'18 [4]	TCAS-I'20 [5]	RFIC'17 [7]	IMS'20 [8]	**This work**
Process	0.13μm SiGe	65nm CMOS	65nm CMOS	55nm CMOS	**40nm CMOS**
Freq./GHz	DC-20	37-40	26-32	DC-32	**26-32**
Att.range/dB	31.5	31	31	32.4	**31.5**
LSB/dB	0.5	1	1	0.255	**0.5**
Insertion Loss/dB	1.7-7.2	7*	N/A	3.5-8.4	**8.5-9.5**
RMS ATT. Error/dB	0.37	0.27	0.5	0.32	**0.23**
RMS Phase. Error/deg.	4	3.7	5	5.33	**5.58**
Return Loss/dB	<-12	<-12	N/A	<-9.6	**<-11.1**
IP1dB/dBm	10	12*	N/A	9.1@30G	**11.2-13**
core area (mm^2)	0.14	0.21	N/A	0.054	**0.124**

*Simulation results

Acknowledgement

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