

A Comparison of 25GHz-LC-VCO Circuit Topologies for SEU Mitigation in 22nm FinFET

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Abstract— Three LC-tank voltage-controlled oscillators (VCOs) are designed in a 22nm FinFET process with varactor and tail filter permutations to compare their sensitivity to single event upsets (SEUs) and understand the overhead these circuit techniques have on electrical performance. Each VCO has a tuning range from 15.8-25.9GHz yielding a tuning aware FOM of 186.12dBc/Hz for the radiation hardened VCO design. Furthermore, these three VCOs were tested at the Texas A&M Cyclotron Institute at linear energy transfer (LET) levels of 10, 35, and 70 MeV.cm²/mg. Testing results showed both a marked decrease in the VCO area sensitive to radiation when using the rad hard varactor tank configuration, and the effectiveness of the LC tail filter for both phase noise and SEU mitigation.

Keywords—CMOS, impulse sensitivity function (ISF), PLL, radiation effects, single-event upset (SEU), VCO.

I. INTRODUCTION

Multi-gigahertz serial link systems for space-based applications are increasingly demanding sub picosecond low jitter phase-locked loop (PLL) clocking solutions. LC-VCOs are a key PLL block in terms of both jitter contribution and sensitivity to SEUs in the space environment [1]. Hence, it is important develop and study LC VCO design techniques that mitigate sensitivity to high energy ions without compromising overall phase noise performance. This paper presents the design, SEU [2] and impulse sensitivity function (ISF) analysis [3], and experimental verification of three 15.8-25.9GHz LC-VCOs with regards to both their electrical performance and SEU sensitivity. In these designs we use FinFET devices which are known to have higher LET thresholds [4] in addition to several other design techniques such as a varactor grounding scheme, LC tail filter [5][6], and RC filtering on the VCO current bias in order to reduce the VCO's sensitivity to SEUs while maintaining competitive phase noise performance when compared to state-of-the-art designs [7][8].

II. CIRCUIT DESIGN

Fig. 1 shows the three LC-VCO schematic permutations, radiation hardened (RH) VCO with tail filter Fig. 1(a), standard (STD) VCO with tail filter Fig. 1(b), and RH VCO without tail filter Fig. 1(c). For the core VCO, the cross coupled pair and tail current source are NMOS due to their lower flicker noise when compared to the same aspect ratio PMOS devices in the 22nm process. For the varactor, in the standard configuration the NWELL of the varactor is connected to the control voltage while the gate of each varactor is connected to the outputs of

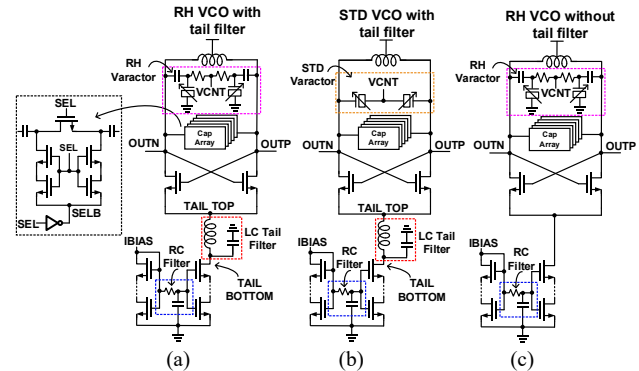


Fig. 1. LC-VCO permutations: (a) RH with tail filter; (b) STD with tail filter; (c) RH without tail filter.

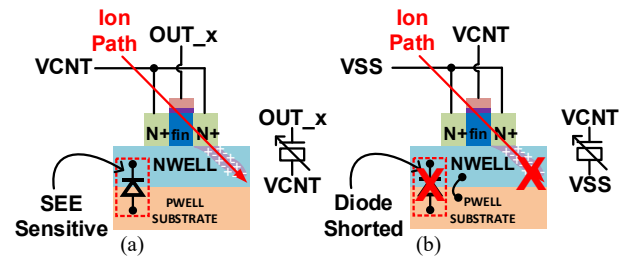


Fig. 2. Varactor configuration: (a) standard; (b) radiation hardened.

the VCO. In the radiation hardened varactor configuration [1], the NWELL of the varactor is grounded reducing the overall area that is sensitive to SEUs since the NWELL becomes grounded. Furthermore, Fig. 2(a) shows the standard varactor configuration and Fig. 2(b) shows the radiation hardened varactor cross sectional connection diagram. The reverse biased junction diode in the standard version is sensitive to SEUs, and upon connecting the NWELL and PWELL substrate to a common VSS any charge collection occurring at this junction is immediately shunted to VSS in the radiation hardened version hence reducing the SEU sensitivity. The varactor is biased through 1kohm resistors the value of which was selected by balancing the thermal noise contribution of the biasing resistors with the need for a high tank Q. Since the biasing resistors are in parallel with the tank, increasing their value leads to less reduction of tank Q but an increase in thermal noise contribution. The ac coupling capacitors are 285fF and couple the varactor to the tank which has a differential capacitance of 20fF to 66fF across the supply (0V to 850mV). Moreover, the

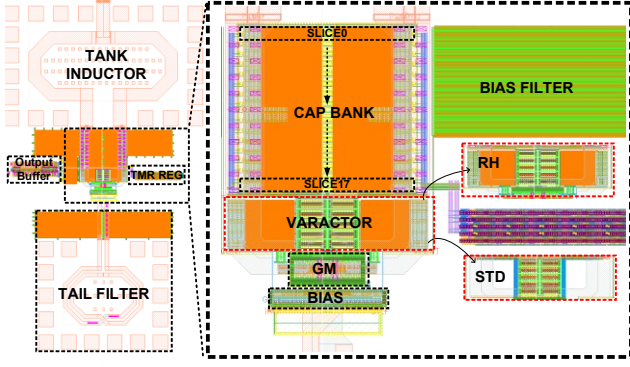


Fig. 3. LC VCO layout.

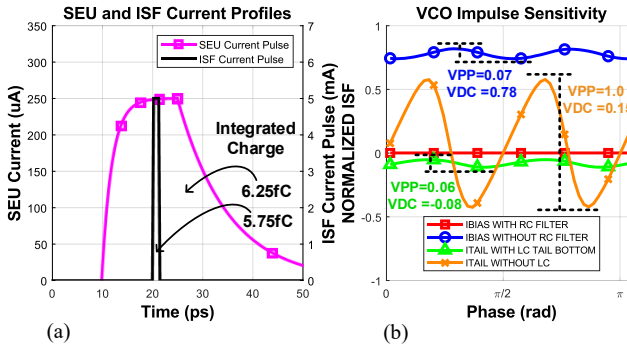


Fig. 4. VCO: (a) SEU and ISF current profiles; (b) impulse sensitivity.

ac coupling introduces bottom plate capacitance and loads the VCO thereby reducing the VCO tuning gain. Overall, the RH varactor configuration provides radiation hardening at the cost of decreased tuning range due to the extra tank capacitance, and reduced phase noise performance due to the introduction of parallel resistance and thermal noise from the varactor biasing resistors. The LC tail filter is comprised of a 340pH two-turn 63umx46um inductor and 9.4pF shunt capacitor which together with the capacitance at the sources of the cross coupled pair provide second harmonic noise filtering [6]. Given its filtering properties, the tail filter also serves to filter transients induced from single event upsets on the tail current path [5]. On the VCO current bias input path, RC filtering is added via a 340kohm resistance and 6.0pF of capacitance to both reduce upconverted flicker noise and filter SEUs. For the current mirror, three devices are cascaded to improve the linearity of the current source and decrease the overall noise contribution of the reference and tail devices. The capacitor bank is 6-bit binary weighted allowing for 64 course tuned states with fine inter-band tuning provided by the varactor. The capacitor bank unit-cell capacitance is 35fF and uses a complementary select cap bank switch to reduce off state leakage induced Q degradation. The tank inductor is a 95pH 55umx118um single turn inductor. In order to enable robust operation of the VCO capacitor bank without SEU induced bit flips, triple modular redundancy (TMR) is used for the serial control interface which controls the capacitor bank of each VCO. The overall differences in layout area between the three VCO variants are

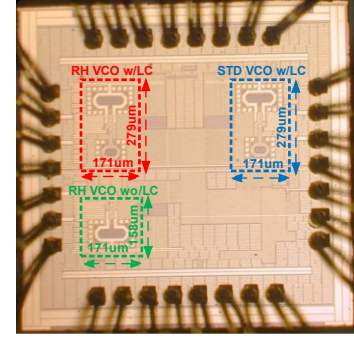


Fig. 5. VCO chip micrograph.

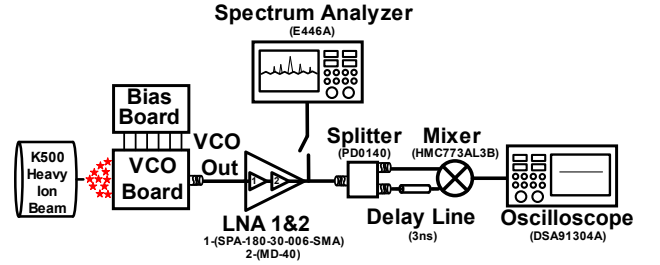


Fig. 6. VCO electrical and SEU test setup.

shown in Fig. 3 with the tail filter and reference bias filter taking up substantial area while comparatively the varactor hardening scheme invokes little area overhead.

III. VCO SEU AND ISF ANALYSIS

Single event upsets in silicon occur when an ion with sufficient energy penetrates into the silicon substrate causing a funnelling of charged particles to occur. These particles can be found in the space environment at varying energy levels depending on the position in orbit as well as the timing of galactic weather phenomena. In the simulation environment, we can model SEUs as a double exponential current source placed in parallel with the drain source regions of a CMOS device. This double exponential current pulse is used to model heavy ion induced charge flow between device diffusions from a particle strike, and the geometry of these SEU current pulses depends on the process technology, penetration depth into silicon, and the LET of the ion [2]. For the VCO in this work, double exponential current pulses were used to model the SEU induced current and verify our hardening techniques in the design stage.

The impulse sensitivity function of a periodic oscillator is found by injecting current pulses over a fixed time interval at different points in an oscillator's period to measure the resulting phase shift [3]. For SEU analysis, we perform the same operation as in the ISF analysis except unit impulse current pulses are replaced with double exponential current pulses. In Fig. 4(a), the geometry of the current profiles used in both ISF and SEU are shown with the integrated ISF current impulse delivering ~5.75fF of charge and the integrated SEU current pulse delivering ~6.25fF of charge. Furthermore, we

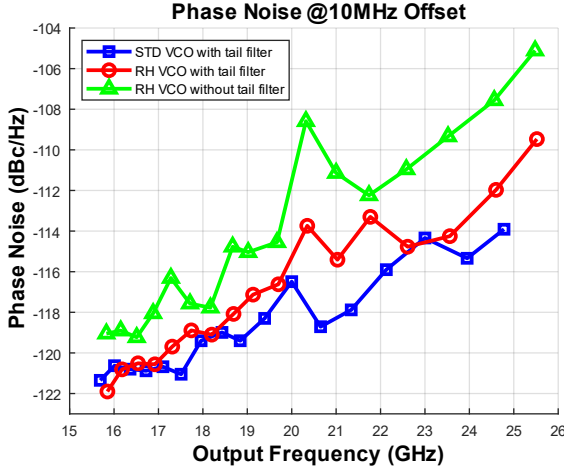


Fig. 7. VCO phase noise @10MHz offset across frequency.

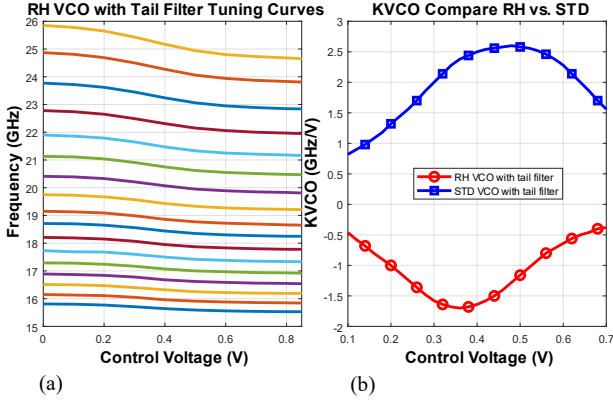


Fig. 8. VCO: (a) frequency tuning bands; (b) RH and STD Kvco.

know that when an oscillator is in the linear range (which it is here since the injected charge is $\ll 10\%$ of the total charge on the node of interest) we can measure the ISF with any arbitrary input current profile as in this region the VCO phase shift is linearly proportional to just total injected charge [3]. Hence, as we look at the ISF in Fig. 4(b), we gain insight into what impact the filtering solutions have on both the phase noise performance as well as their SEU filtering. In Fig. 4(b), the results of the simulated ISF analysis for the VCO @15.8GHz are shown with several circuit permutations. Namely, we can see an almost complete elimination of sensitivity when using an RC filter on the reference bias node which also mapped to improved phase noise performance due to filtering of the reference current input transistors noise. For the LC tail filter, we achieve a $\sim 2\times$ reduction in the sensitivity peak to peak swing when comparing to the LC VCO without a tail filter.

IV. EXPERIMENTAL RESULTS

All three VCOs were fabricated Fig. 5 and tested across their full frequency range with the setup in Fig. 6 to plot the phase noise @10MHz offset as is shown in Fig. 7. For these measurements the bias current to the VCO was kept constant across the entire frequency range. Overall, the RH varactor configuration degrades the phase noise performance due to the

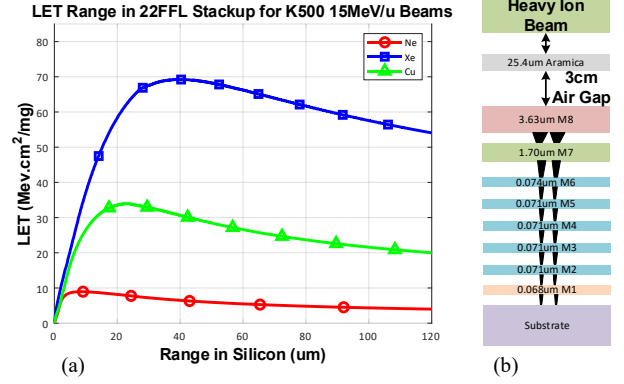


Fig. 9. (a) K500 cyclotron LET range; (b) SEU testing layer-map.

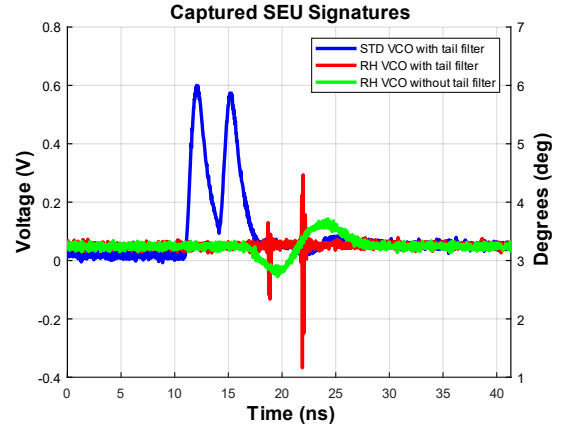


Fig. 10. Captured SEU signatures.

introduction of resistance in the tank for the varactor biasing, however, with the LC tail filter $\sim 4\text{dB}$ of phase noise can be recovered past the designed LC resonance frequency of 21GHz. The tuning band overlap characteristics of the rad-hard VCO for 17 of the 64 capacitor bank states is shown with inter-band varactor tuning yielding a tuning range of 15.8GHz to 25.9GHz as shown in Fig. 8(a). Furthermore, Fig. 8(b) also shows a comparison of the Kvco for the equally sized varactors used in the STD VCO and RH VCO. As was previously mentioned, the tuning polarity for the RH VCO is inverted and the overall Kvco is lower than that of the STD VCO. Due to the large tuning range, low power, and tail filtering, this design has reasonable performance when compared with state-of-the-art designs in [7], and [8] while improving over the rad hard design in [1].

For SEU radiation testing, the delay line discriminator setup in Fig. 6 is used to capture transient phase steps within the VCO chip. The 3ns delay line is used to delay the VCO signal such that there is a phase difference between the carrier and delayed signal should a phase step within the chip occur. Furthermore, this phase difference is converted to a voltage difference with a mixer-based phase detector. The two series LNAs increase the gain of the delay line system thereby increasing the voltage output swing. Fig. 9(a) shows the three ions that were tested at the Texas A&M Cyclotron along with their respective modelled LET versus range in silicon. Furthermore, the LET modelling

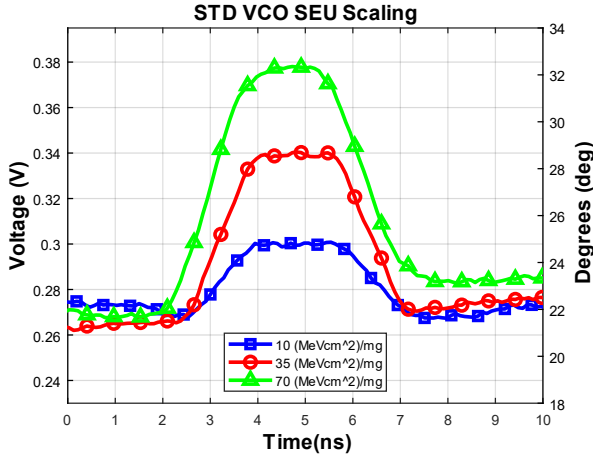


Fig. 11. STD VCO captured SEU induced transients across LET levels.

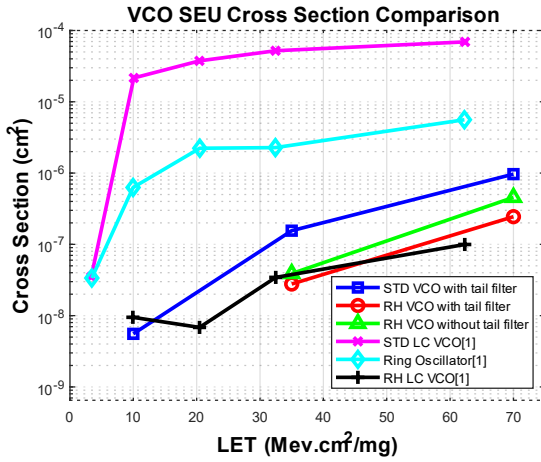


Fig. 12. VCO cross sectional area comparison.

in Fig. 9(a) takes into account the 22FFL layers, beam lens, and air gap to accurately model the test setup Fig. 9(b). Transient waveforms of captured SEU induced phase jumps are shown in Fig. 10 at an LET of 70 MeV.cm²/mg with the phase detector output voltage converted to its equivalent phase step in degrees. In Fig. 11 the output phase step from the STD VCO is shown versus input LET showing the scaling of the induced phase step for an increasing LET. The oscilloscopes 250ps oscilloscope triggering limitation set the minimum SEU event duration that we could capture, and our hysteresis window of +/-35 mV set the minimum amplitude phase jump we could capture. The cross-sectional area of the three VCOs is show in Fig. 12 with total fluences ranging from 9.0e7 to 1.8e8 ions/cm². From these results, the unhardened design had the largest cross section due to the sensitivity of the varactor to SEUs [1] with no events being detected at an LET of 10 MeV.cm²/mg for the radiation hardened VCOs. Additionally, it is shown that the LC tail filter provides 1.5x~2x reduction in cross section across the two LETs where upsets were detected. These SEU results correlate with the sensitivity findings from our ISF modelling with regards to the tail filter. Compared to the radiation hardened VCO in [1], our measured cross sections were at similar orders

Table 1. Performance Summary

Work	J. Prinzie TNS'18 [1]	O. El-Aassar JSSC'21 [7]	Z. Chen TMTT'17 [8]	[This Work] RH LC/STD LC/RH no LC
Implementation	VCO	VCO	VCO	VCO
Technology	65nm	22nm	90nm	22nm
Frequency	2.5-2.65	8-17	19.18-22.49	15.8-25.9
VCO Power Consumption [mW]	1.8	17-33	8.1	6.6
Tuning Range (%)	4	72.0	15.8	48.0
Phase Noise (PN) @10MHz [dBc/Hz]	-139.0	-134.7	-123	-115/-116.5/-112
FoM [dBc/Hz]	179.38	180.65	180.29	173.87/174.68/170.18
FoM _T [dBc/Hz]	168.92	197.8	183.81	186.12/188.31/183.81
Cross Section cm ² @ 50 MeV.cm ² /mg	6.4E-8	N/A	N/A	7.1E-8/3.4E-7/1.1E-7
Radiation Hardening	Yes	No	No	Yes

$$FoM = -PN + 20\log_{10}(f_o/\Delta f) - 10\log_{10}(P_{dc}/1mW)$$

$$FoM_T = FoM + 20\log_{10}(TuningRange/10\%)$$

of magnitudes. Overall, the delta between cross sections for the unhardened and hardened VCOs for the work in [1] was much larger than our results. Moreover, this can be attributed to the relative SEU hardness of FinFET devices [4] compared to the 65nm planar devices and/or the difference in the ratio of the varactor area to the other SEU sensitive devices in the VCO design.

V. CONCLUSION

We have presented three high-performance 15.8-25.9GHz LC-VCOs in a 22nm FinFET process, and verified both the varactor and LC tail filter hardening techniques at the Texas A&M Cyclotron Institute.

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REFERENCES

- [1] J. Prinzie, *et al.*, "A 2.56-GHz SEU Radiation Hard LC -Tank VCO for High-Speed Communication Links in 65-nm CMOS Technology," in *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 407-412, Jan. 2018, doi: 10.1109/TNS.2017.2764501.
- [2] G. C. Messenger, "Collection of Charge on Junction Nodes from Ion Tracks," in *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 2024-2031, Dec. 1982, doi: 10.1109/TNS.1982.4336490.
- [3] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179-194, Feb. 1998, doi: 10.1109/4.658619.
- [4] J. Noh *et al.*, "Study of Neutron Soft Error Rate (SER) Sensitivity: Investigation of Upset Mechanisms by Comparative Simulation of FinFET and Planar MOSFET SRAMs," in *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1642-1649, Aug. 2015, doi: 10.1109/TNS.2015.2450997.
- [5] Z. Zhang, H. Djahanshahi, C. Gu, M. Patel and L. Chen, "Single-Event Effects Characterization of LC-VCO PLLs in a 28-nm CMOS Technology," in *IEEE Transactions on Nuclear Science*, vol. 67, no. 9, pp. 2042-2050, Sept. 2020, doi: 10.1109/TNS.2020.3008142.
- [6] E. Hegazi, *et al.*, "A filtering technique to lower LC oscillator phase noise," in *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1921-1930, Dec. 2001, doi: 10.1109/4.972142.
- [7] O. El-Aassar and G. M. Rebeiz, "Octave-Tuning Dual-Core Folded VCO Leveraging a Triple-Mode Switch-Less Tertiary Magnetic Loop," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 5, pp. 1475-1486, May 2021, doi: 10.1109/JSSC.2021.3059442.
- [8] Z. Chen *et al.*, "Linear CMOS LC-VCO Based on Triple-Coupled Inductors and Its Application to 40-GHz Phase-Locked Loop," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 8, pp. 2977-2989, Aug. 2017, doi: 10.1109/TMTT.2017.2663401.