Implementation of SIW Cavity in Commercial CMOS Technology for Sub-Terahertz Band Applications

Samundra K. Thapa*, Ramesh K. Pokharel*, Adel Barakat*, Ruibing Dong#, Shuhei Amakawa^, Shinsuke Hara#, Issei Watanabe#, Akifumi Kasamatsu#
*Graduate School of Information Science and Electrical Engineering, Kyushu University, Japan
#National Institute of Information and Communication Technology, Japan
^Hiroshima University, Japan
thapa.samundra.391@s.kyushu-u.ac.jp, pokharel@ed.kyushu-u.ac.jp

***Abstract*—For sub-terahertz band applications, two compact and low-loss on-chip substrate integrated waveguide (SIW) cavities are designed in CMOS technology. Compact size cavity is achieved by utilizing the folded ridge structure in the quarter mode SIW (QMSIW) structure which is loaded with complementary split-ring resonators (CSRRs). Two prototypes of the proposed QMSIW cavities with and without CSRR are fabricated in 1P6M CMOS technology. From the measurement, both cavities present return losses higher than 27 dB and external *Q*-factors higher than 140. The proposed work shows that even at such high frequencies, compact and low-loss SIWs can be fabricated in commercial CMOS technology and opens a window to utilizing such cavities for other low-loss components such as oscillators, on-chip bandpass filters and on-chip antennas for sub-terahertz band applications.**

***Keywords*— cavity, CMOS technology, substrate integrated waveguide (SIW), sub-terahertz.**

I. Introduction

5G has successfully launched with sub-6 GHz and quasi-millimeter wave bands. Now, researchers are targeting millimeter and sub-terahertz waves. For such high-frequency applications, one growing demand is to design integrated active-passive systems in the same process to minimize the effect of active-passive interconnection losses [1]–[2]. Due to inherent low attenuation and planar integration capabilities, a low-profile substrate integrated waveguide (SIW) has been an attractive solution for low-loss designs, even at high frequencies. The only demerit of the SIW topology is its broadside width which depends on the cut-off frequency but remains still significantly large even at frequencies in the millimeter and above bands.

Several attractive works on compact-size high-quality (*Q*-) SIW-based RF and microwave components have been reported ranging from filters to active devices and antennas in printed circuit board (PCB) technology [3]–[7]. For *on-chip* SIW designs, the major disadvantages of the SIW-based designs are its wide broadside width and the predetermined constraints, including available via sizes and dielectric thicknesses, and metal density rules. The sub-mode SIW structures significantly reduce the size in both on-chip and off-chip designs, but due to open boundaries, undesired radiation leakage appears, resulting in *Q*-factor degradation [3]–[4], [6]–[10]. Besides, performance can also degrade due to dielectric losses and added dummy metal fills. Therefore, designing on-chip compact low-loss SIW-based components at high frequencies is still challenging.

This work presents on-chip 200 GHz band cavities based on compact quarter-mode SIW (QMSIW) designed using a commercial CMOS technology. The effect of predetermined via size and via spacing in the design is also discussed in this paper. Two prototypes of folded ridge QMSIW cavities with and without complementary split-ring resonators (CSRR) loading are fabricated and verified. Measurements results of both designs are in good agreement with simulation results.

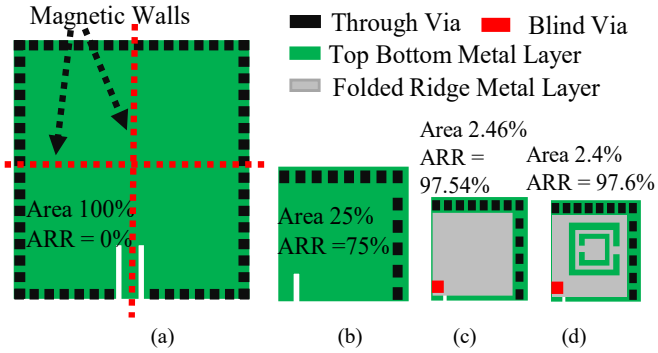


Fig. 1. SIW cavity: (a) standard mode; (b) QMSIW; (c) folded ridge QMSIW; (d) folded ridge QMSIW with CSRR loadings. *ARR = Area Reduction Ratio compared to standard SIW at the same resonance.

II. 200 GHz Folded Ridge QMSIW Cavities

A. Folded Ridge QMSIW Cavity Design

In the fundamental TE_{10} mode, the standard SIW cavity has electric field distribution with several perfect symmetry planes (magnetic walls), and sub-mode cavities can be obtained by making cuts along these symmetry planes, ideally without affecting its resonance. The QMSIW cavity is designed by taking a quarter of the standard SIW cavity design by making two symmetric cuts as shown in Figs. 1(a) and (b). An area reduction of 75% is achieved but due to two sideways openings, different losses start to appear, and it is difficult to prevent resulting return loss and the quality factor degradation.

By introducing a capacitive ridge as folded structure inside the cavity as shown in Fig. 1(c), the performance can be improved due to the stronger electric field inside the cavity [4], [6], [8]–[9]. The resonant frequency becomes lower due to the

added capacitance achieving substantial miniaturization. The variation of the frequency and the reflection coefficient with respect to the ridge width (W_r) is shown in Fig. 2, which shows that wider ridge width will result in lower frequency. This is because additional capacitance appears due to the closeness of the edge of the folded ridge to the sidewall of the main SIW cavity [4], [6]. This added capacitance of the folded ridge depends on ridge width dimensions, blind via position, and ridge height. Therefore, by proper selection of these parameters, maximum miniaturization of folded ridge SIW cavity resonator can be achieved.

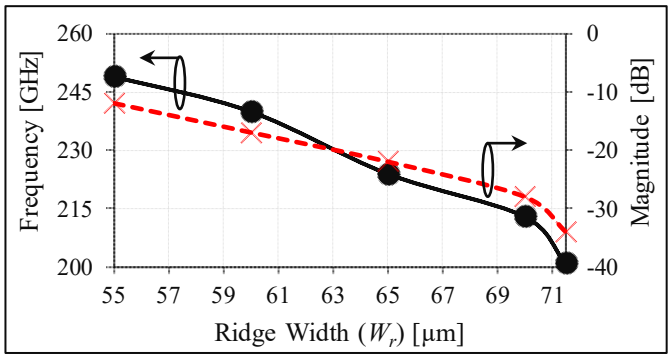


Fig. 2. A 200 GHz folded ridge QMSIW frequency and reflection coefficient magnitude by varying folded ridge width.

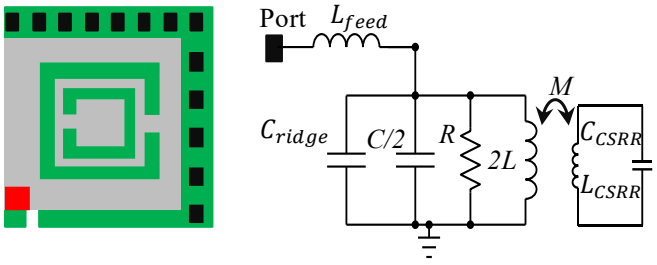


Fig. 3. Folded ridge QMSIW cavity with CSRR loading: (a) electromagnetic model; (b) equivalent circuit.

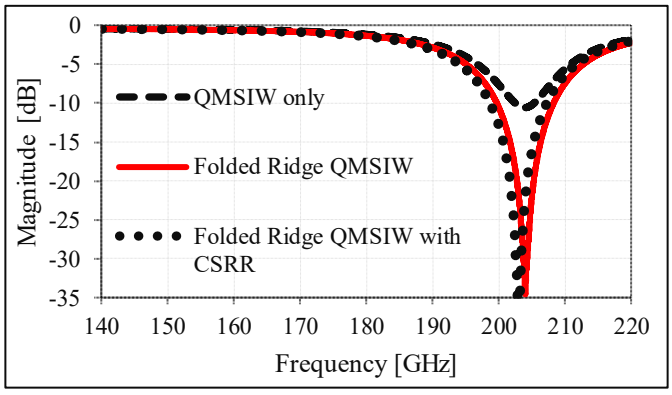


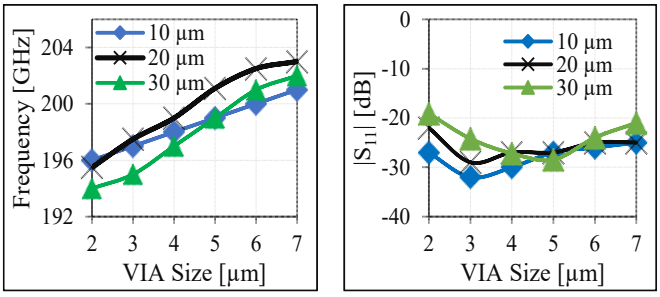
Fig. 4. Reflection coefficient of QMSIW cavities all designed at 200 GHz resonance frequency.

When a microwave structure is loaded with such loadings, additional losses start to appear because the frequency is very high, and the structures can radiate readily. To minimize such losses, external matching should be employed but that could introduce more losses. So, to improve by internal matching within folded ridge QMSIW cavity, a rectangular CSRR is loaded as shown in Fig. 1(d). CSRR loadings advantages (a) mode matching and (b) resonance frequency drop due to introduced couplings. The accumulated effect of the CSRR loadings is shown by couplings in Fig. 3(b) [11]–[12]. The effect of loading CSRR can be seen in the matching as shown in Fig. 4, which shows that a good matching is achieved by CSRR loadings in the folded ridge QMSIW structure.

B. Effect of Via Size and Spacing on Frequency, Reflection Coefficient, and the Radiation Efficiency

An array of vias in SIW structures acts as an electric wall so that the propagating signal is confined within the SIW cavity as in a conventional waveguide structure. The design of the via size (d) and the via spacing (p) is as in printed circuit board (PCB) technology [3]. However, the via size and the via spacing greatly affect the resonance and the reflection coefficient in on-chip SIW design at very high frequencies. This is because the total effective inductance from the via wall changes a lot in the on-chip design than in the PCB counterpart. The foundry available square vias are employed in this work. The effects of the square via with size ($d \times d$) and the via spacing are shown in Fig. 5. For our design, the optimal via size and spacing is selected as 4 μm × 4 μm and 25 μm, respectively.

The total radiation efficiency of the proposed folded ridge QMSIW cavity with varying via spacing is presented in Fig. 6. The efficiency is very low, confirming that the proposed design does not radiate at the desired resonance frequency.



(a) (b)

Fig. 5. Effect of square via size (side length) and via spacing of folded ridge QMSIW cavity on: (a) resonance frequency; (b) reflection coefficient.

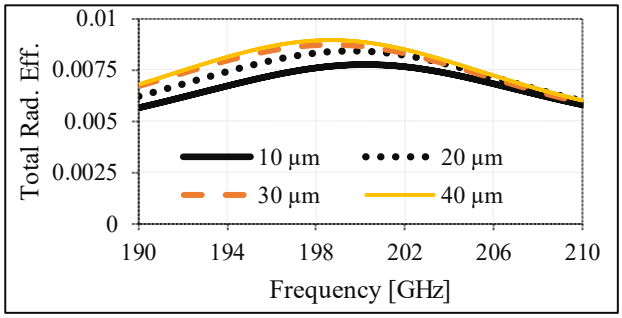


Fig. 6. Total radiation efficiency of folded ridge QMSIW cavity with CSRR loading with varying via spacing.

III. Implementation in CMOS Technology

C. Implementation and Fabrication

The proposed SIW cavity resonators are implemented in a commercial 1P6M CMOS technology. The top plate, folded ridge, and bottom plate are implemented with metal layers M6, M3, and M1, respectively. The metal stacks were used to create vias: (i) blind via (M3 to M6 via) and (ii) SIW sidewalls (M1 to M6 via) for connecting ridge and top metal, and top and bottom plates, respectively. The optimized dimensions of the two cavities are embedded in Fig. 7 and Fig. 8. The micrographs of the fabricated prototypes are shown in Fig. 9. The chips are fabricated with dummy pads in opposite of feeding port to stabilize chips during measurement.

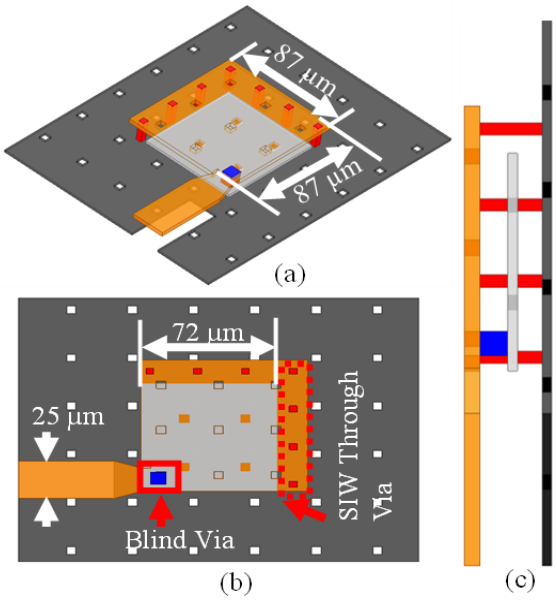


Fig. 7. EM model of the proposed folded ridge QMSIW cavity. (a) 3D view; (b) top view; (c) side view.

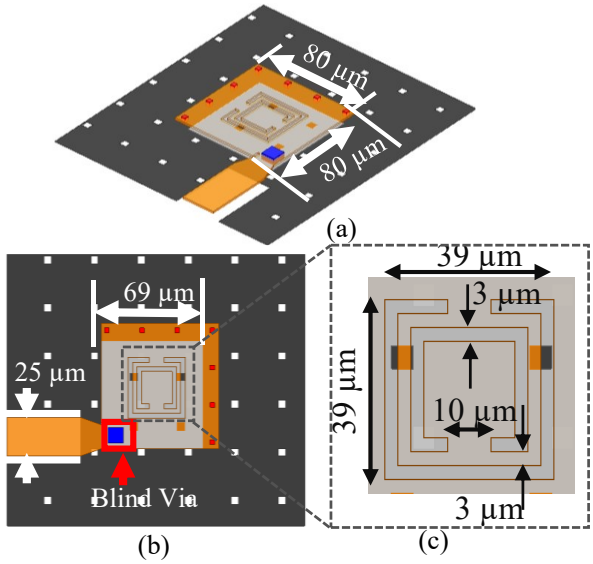


Fig. 8. EM model of the proposed folded ridge QMSIW cavity with CSRR loadings. (a) 3D view; (b) top view; (c) loaded CSRR dimensions.

D. Fabrication and Measurement Results

In Fig. 10, the measurement results of $|S_{11}|$ along with the simulated results are presented over the frequency range of 140 to 220 GHz. The simulated results are presented without including pads, whereas measured results are presented before and after performing de-embedding using multiline thru-reflect-line (m-TRL) structures [13]. After de-embedding, folded ridge QMSIW cavity resonator with and without CSRR loading shows resonance frequency of 207.2 GHz and 206.3 GHz, respectively. The reason of frequency shift after de-embedding is due to the removal of parasitic capacitance of the pads. The measured $|S_{11}|$ are –27.2 dB and –28.9 dB, respectively. Similarly, the computed external Q-factors are 142 and 158, respectively. The shift in the resonance frequencies in both the designs is presumably due mainly to the change in the effective active areas of the fabricated prototypes owing to effects of dummy metal fills and predetermined foundry via layout that are not fully possible to be included in the simulation. However, the shift in each design is only less than 3%.

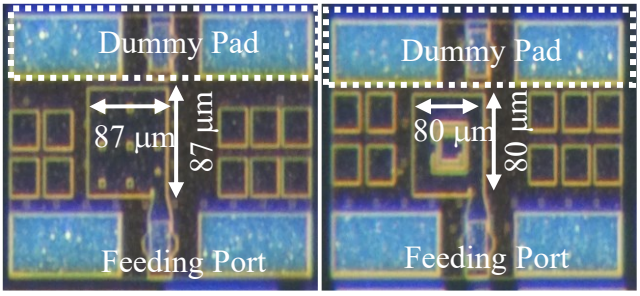


Fig. 9. Fabricated cavities chips micrographs: (a) QMSIW; (b) QMSIW with CSRR.

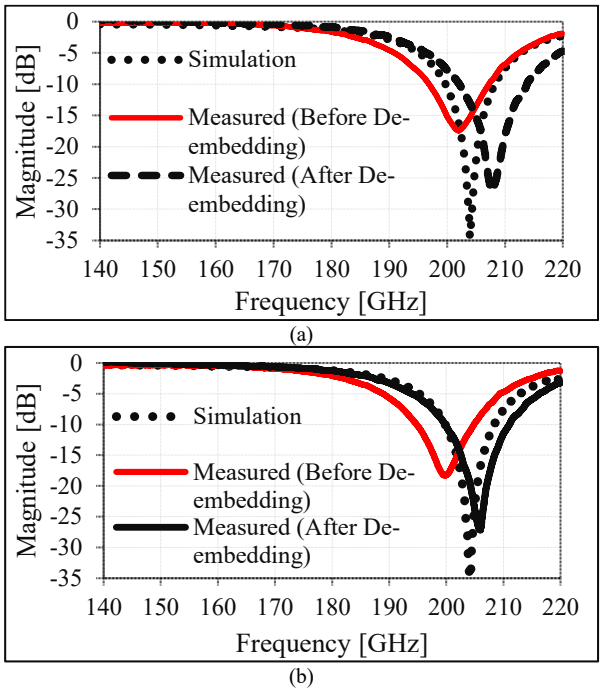


Fig. 10. Measurement $|S_{11}|$ of proposed folded ridge QMSIW cavities: (a) without CSRR loading; (b) with CSRR loading.

IV. Conclusion

This work presents low-loss sub-terahertz band SIW-based cavities implemented using a commercial 1P6M CMOS technology. Two prototypes of miniaturized cavities using folded ridge QMSIW and folded ridge QMSIW with CSRR loading were fabricated and tested. Effects of the via size and the via spacing is discussed in this work. The experimental results of both the designs shows a good return loss of greater than 27 dB with the measured external *Q*-factor greater than 140 at 200 GHz band resonance frequency. The cavity models presented in this work will be applicable to design components like filters, antennas, oscillators, and many more for sub-terahertz applications.

Acknowledgement

This work was supported in part by the Murata Science Foundation, and in part by the activities of VLSI Design and Education Center (VDEC), The University of Tokyo in collaboration with Cadence Corporation, the Mentor Graphics Corporation, and Keysight Technologies Japan, Ltd.

References

[1] E. Elsaidy, A. Barakat, A. B. Abdel-Rahman, A. Allam, and R. K. Pokharel, "Ultracompact CMOS 60-GHz Tapped-Line Combline BPF With Two Transmission Zeros Using Defected Ground Structures," in *IEEE Trans. Compon. Packag. Manuf. Techn.,* vol. 8, no. 9, pp. 1642-1649, Sept. 2018.

[2] R. K. Pokharel, X. Liu, R. Dong, A. B. A. Dayang, H. Kanaya and K. Yoshida, "60GHz-band low loss on-chip band pass filter with patterned ground shields for millimeter wave CMOS SoC," in *Dig. 2011 IEEE MTT-S Intl. Microw. Symp.*, Baltimore, MD, USA, 2011, pp. 1-4.

[3] S. K. Thapa, B. Chen, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "X-Band Feedback Type Miniaturized Oscillator Design With Low Phase Noise Based on Eighth Mode SIW Bandpass Filter," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 5, pp. 485–488, May 2021.

[4] T. R. Jones and M. Daneshmand, "Miniaturized Folded Ridged Half-Mode and Quarter-Mode Substrate Integrated Waveguides for Filter Design," *IEEE Trans. Microw. Theory Techn*., vol. 67, no. 8, pp. 3414–3426, Aug. 2019.

[5] S. K. Thapa, B. Chen, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "Miniaturized Slot-Loaded SIW Resonator and Its Application to C-band Low Phase Noise Oscillator," in *Proc. 2020 50th European Microw. Conf. (EuMC)*, Utrecht, Netherlands, 2021, pp. 161–164.

[6] T. R. Jones and M. Daneshmand, "Miniaturized Folded Ridged Quarter-Mode Substrate Integrated Waveguide RF MEMS Tunable Bandpass Filter," *IEEE Access*, vol. 8, pp. 115837–115847, 2020.

[7] D. E. Senior, A. Rahimi, and Yong-Kyu Yoon, "A surface micromachined broadband millimeter-wave filter using quarter-mode substrate integrated waveguide loaded with complementary split ring resonator," in *IEEE MTT-S Int. Microw. Symp. (IMS2014)*, Tampa, FL, 2014, pp. 1–4.

[8] M. Shahidzadeh Mahani, and G. W. Roberts, "A mmWave Folded Substrate Integrated Waveguide in a 130-nm CMOS Process," *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 8, pp. 2775–2788, Aug. 2017.

[9] B. Chen, S. K. Thapa, A. Barakat, and R. K. Pokharel, "A W-Band 0.01 mm² Cavity Resonator Employing Slot-Loaded Shielded Folded Ridged Quarter-Mode in CMOS Technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 2, pp. 113–116, Feb. 2022.

[10] B. Chen, S. K. Thapa, A. Barakat, and R. K. Pokharel, "A W-band Compact Substrate Integrated Waveguide Bandpass Filter With Defected Ground Structure in CMOS Technology," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 69. No. 3, pp. 889–893, March 2022.

[11] Y. D. Dong, T. Yang, and T. Itoh, "Substrate Integrated Waveguide Loaded by Complementary Split-Ring Resonators and Its Applications to Miniaturized Waveguide Filters," *IEEE Trans Microw. Theory Techn.*, vol. 57, no. 9, pp. 2211–2223, Sept. 2009.

[12] S. K. Thapa, R. K. Pokharel, B. Chen, T. Fukuda, and A. Barakat, "Millimeter-Wave High Q-factor Sixteenth Mode SIW Cavity Resonator Implemented in 0.18 µm CMOS Technology," in *Dig. 2022 IEEE MTT-S Intl. Microw. Symp.*, Denver, CO, USA, 2022, pp. 560-563.

[13] A. Orii et al., "On the length of THRU standard for TRL de-embedding on Si substrate above 110 GHz," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Osaka, Japan, Mar. 2013, pp. 81–86.