Optimization of Coplanar Waveguide Integrated PCM Switches

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***Abstract*—This paper presents the optimization of coplanar waveguide integrated PCM switches. PCM switches isolation efficiency is directly affected by distance between ground planes above and below the transmission line. Reducing this distance from 160 µm to 26 µm, while keeping exactly the same PCM switch core, dramatically improves measured isolation from -22.2 dB to —31.1 dB at 40 GHz using a single device. Without changing the switch geometry, its figure of merit is enhanced from 14.9 fsec to 5.9 fsec. The design technique presented in this paper can be re-used for designing CMOS integrated PCM switches.**

***Keywords*—GeTe, Reconfigurable Devices, Phase-Change Material, RF Switches.**

I. Introduction

Technology advances in telecommunication systems require efficient reconfigurable devices, to change antennas impedance [1], realize redundancy matrix or shift signal phase. Hence, RF switches are among the most critical components in these systems, requiring good RF performances and high integration. FET (Field Effect Transistor) made on SOI, SOS, GaN and RF-MEMS are well known and commonly used as RF switches to design reconfigurable components [2–4]. While FET are compact [5-6] RF-MEMS switches provide high-performance and endurance [7] but require complicated processing [8].

Phase-Change Material (PCM) switches are an emerging alternative, with high RF performances [9], compactness and endurance [10], with a simpler fabrication process. Moreover, PCM switches are bi-stable, retaining a given state without energy, or bias.

PCM are materials whose crystallographic structure can be either crystalline, providing high electrical conductivity, or amorphous, with high electrical resistivity. In this paper, switching from a state to the other one is realized using temperature stimulus and GeTe alloy is used in this study. Heating up GeTe above its melting temperature (> 700°C) [11], followed by a fast temperature quench (< 20 nsec) [12], maintains a disordered arrangement of matter, resulting in a high resistivity state. This amorphous phase persists until temperature reaches crystallisation level (between 172 and 186°C) [13-14]. Then GeTe crystallizes back and recovers its high electrical conductivity.

PCM-based Memories have retention time of 10 years at 86°C [13], but this time has been shown to be shorter once integrated in RF switches [15].

In this study, temperature is controlled by a Joule effect using a resistor underneath the GeTe layer.

This paper will present simulated and experimental optimization results of PCM RF switches. The fabrication process is presented in a first part, before operation principle. Then two circuit designs will be introduced, and it will be shown that off-state isolation can be dramatically improved by controlling the width of the coplanar waveguide surrounding the switch.

Indeed, compared to other competing technologies, PCM switches allow fabricating very high isolation switches using a single device, compared to stacked transistors or electrostatically actuated RF-MEMS switches. The idea developed in this paper is to take advantage of the compactness of PCM devices, and concentrate the electromagnetic fields around a small-section coplanar waveguide. We will show that reducing the section of the coplanar waveguide greatly improves isolation of a given PCM switch.

II. Fabrication process

Fabrication process steps are presented in Fig. 1. Switches are processed on a 600 µm thick high-resistivity silicon substrate, covered by a 100 nm thick layer of SiO_2. Cleaning steps are carried out all along fabrication.

First, a 55 nm thick layer of Mo is DC-sputtered. Successive optical lithography and wet etching are used to pattern Mo and fabricate the heater element, whose resistance value is measured from 107 to 118 Ω at the end of the process.

Above this Mo layer, a 100 nm thick layer of Si_3N_4 is deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) in order to constitute a dielectric barrier between heater and conductive materials above. Contacts for heater are opened by optical lithography and RIE etching.

Then, an 80 nm thick layer of GeTe is RF-sputtered. It is then annealed at 300°C for 5 minutes on a hotplate to fully crystallize PCM. GeTe is defined by optical lithography and RIE etching.

Finally, a 10/450 nm thick layer of Ti/Au is evaporated and lifted-off to create RF lines and contacts. There is no passivation layer and all measurements have been conducted in open laboratory environment and room temperature.

III. Operation Principle

Operation principle is presented in Fig. 2. In the ON state, RF signal can pass through the transmission line because of high electrical conductivity of GeTe. Applying a 100 mA for 500 nsec through heater element, melts the GeTe in the area above the heater. After a fast quench, GeTe remains amorphous, and switch is OFF thanks to its very low conductivity. To crystallize it back, 60 mA for 2 µsec pulse is sent. The measured fall-time of pulses in our setup is 14 nsec.

Most of GeTe layer is crystalline in both states, but the active area only, above the heater, is switched between amorphous and crystalline phases.

The two designs presented in next section exactly have the same PCM switch core, made of metallization connected to a 3 µm gap of GeTe, wide of 20 µm. This gap is very large compared to state-of-the-art photolithography, and the performances presented in this paper can be further improved by using more advanced photolithography.

To characterize RF switches, a Figure of Merit (FoM) is calculated by using the R_{On} x C_{Off} product. R_{On} is the equivalent series resistance in the ON-state and shows the resistivity of the switch. C_{Off} is the equivalent series capacitor in the off-state and corresponds to the isolation of the switch in the OFF-state. The lower R_{On} and C_{Off}, the lower FoM, and the better the switch is, since this FoM is directly related to the switch contrast between the two states.

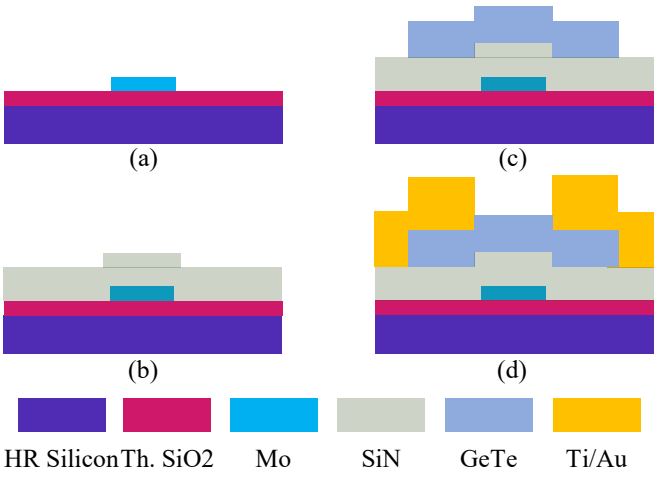

Fig. 1. Cross-section view of fabrication process steps.

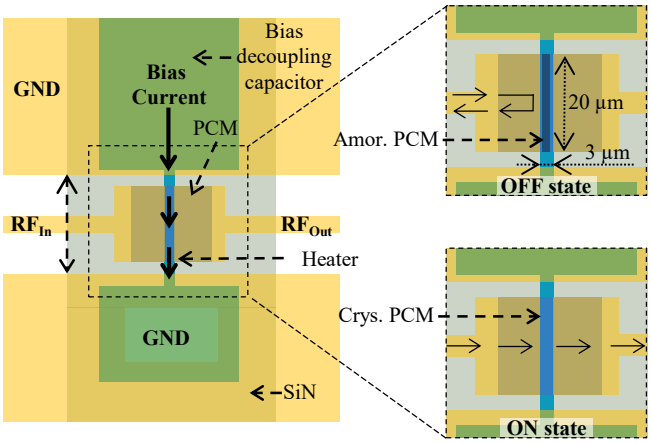

Fig. 2. Top-view of the PCM switch core.

In order not to consider metallization losses, device with Ti/Au above GeTe line is realized on the same substrate during fabrication process, with a corresponding R_{tru} = 2.4 Ω. This resistance is included in S-Parameters measurements presented in the paper, since no de-embedding was done on microwave measurements. The off-state capacitance values are extracted from off-state S-Parameters measurements.

The measurement setup is presented in Fig. 3. RF probes (GSG125 ACP65-A 125 µm) mounted on probe station are used to measure switches, with a ZVA67 Rohde & Schwarz Vector Network Analyzer. In order to avoid noisy measurements [16], the bias line is not connected with GSGSG probes, but with a DC probe (Cascade 122188), connected to the bias pad. Control pulses are generated by an Agilent 8114A pulse generator.

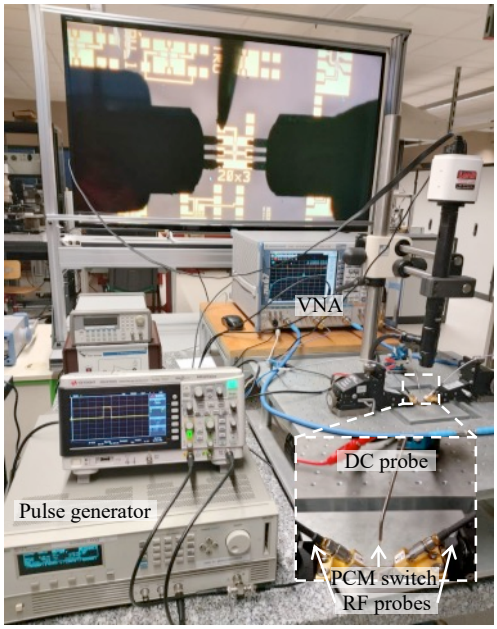

Fig. 3. Measurement setup.

IV. Design Optimization

Conventional and optimized PCM RF switches are presented in Fig. 4.a and 4.b. Both have a capacitor decoupling bias from RF lines, and enhancing isolation [16].

First design has a 160 µm ground plane distance and a 30 µm wide transmission line. The optimized one has ground-to-ground distance reduced down to 26 µm, and its transmission line is 5 µm wide. Moreover, the decoupling capacitor is twice times greater in the second design.

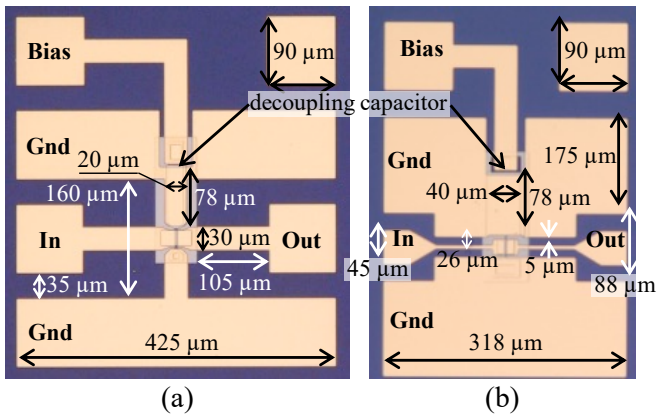

Fig. 4. Optical microscope view of conventional design (a) and optimized design (b) of PCM RF-switches.

S-Parameters of 20x3 conventional design is presented in Fig. 5. 20x3 switch presents insertion losses of -0.64 dB @ 2 GHz and -1.05 dB @ 40GHz, isolation greater than -22.4 dB up to 40 GHz and reflection losses lower than -16.4 @ 40 GHz. R_{on} (@ 100 MHz) is 4.8 Ω, (removing 2.4 Ω from input-output lines) and C_{Off} (@ 40 GHz) is 3.1 fF. This switch corresponding FoM is 14.9 fsec.

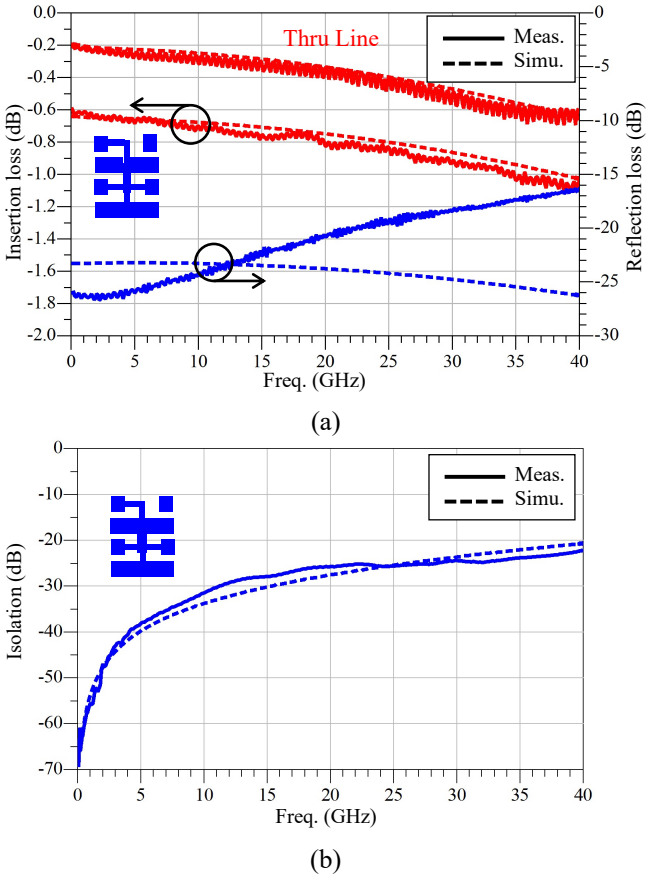

Fig. 5. Measured and Keysight Momentum simulated S-Parameters of the 20x3 PCM switch. On-State (a), Off-State (b).

S-Parameters of the Optimized 20x3 design are presented in Fig. 6. It shows insertion losses of -0.67 dB @ 2 GHz and -1.0 dB @ 40GHz, isolation greater than -31.1 dB up to 40 GHz and reflection loss lower than -17.9 @ 40 GHz. R_{On} (@ 100 MHz) is 5.4 Ω and C_{Off} (@ 40 GHz) is 1.1 fF. FoM is 5.9 fsec. FoM is reduced by 64% with a narrow section of coplanar waveguide while maintaining exactly the same PCM switch core. Simulations are obtained from Keysight Momentum.

Comparison of both designs is presented on the same plot in Fig. 7. Reflection losses are not plotted but they are 1.5 dB better at 40 GHz for the optimized design, and similar at low frequencies.

This specific coplanar design can be easily integrated into CMOS back-end process, where the multiple metallization layers allow for using small cross-section microstrip lines. In such process, designers can take advantage of the small size of PCM switches to improve their performances.

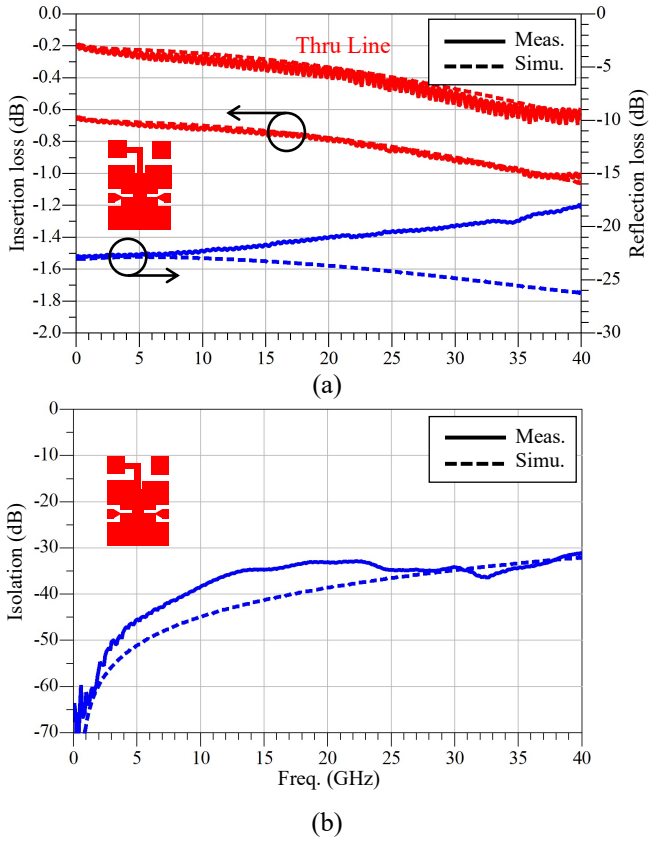

Fig. 6. Measured and Keysight Momentum simulated S-Parameters of the Optimized 20x3 PCM switch. On-State (a), Off-State (b).

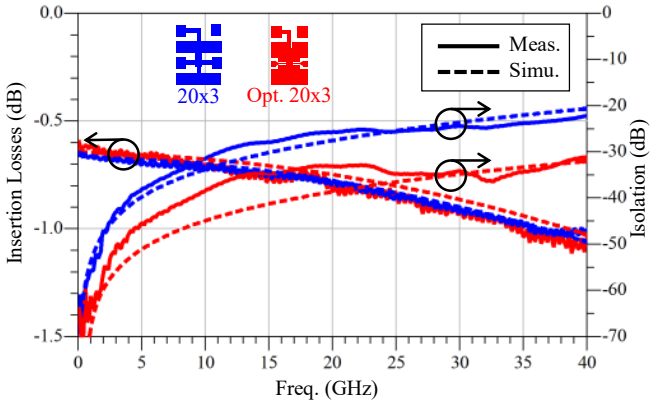

Fig. 7. S-parameters of 20x3 and Optimized 20x3 PCM switches.

V. Conclusion

This paper presents the optimization of coplanar waveguide integrated PCM switches, keeping the same PCM switch core. Reducing distance between ground planes below and above transmission line enhances isolation from -22.2 to -31.1 dB @ 40 GHz, without affecting significantly insertion losses, maintaining good reflection losses. FoM is improved from 14.9 to 5.9 fsec.

Moreover, in future fabrication runs, this design can be optimized by reducing GeTe width from 3 µm to 1.5 µm.

Electromagnetic simulation results show that this would further reduce R_{on} from 5.4 to 3.1 Ω, without impacting isolation, giving a FoM of 3.4 fsec.

In the future, integration of these designs into back-end CMOS processing, where the small-size of PCM switches will allow integration of high performance, wide band switches.

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