

A compact multi-channel CMOS frequency multiplier for millimeter-wave and terahertz signal generation

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Abstract—This paper presents a compact multi-channel CMOS active multiplier in a single chip which output generates the three different signals from V-to G-band frequencies. A meandered marchand balun and active power divider enable to minimize the overall chip size and achieve the wideband operation. The active power divider provides a wideband gain response as well as a constant gain variation according to the different load impedances. Therefore, the chip can provide independent output sources from 52 to 252 GHz with a Ka-band input signal in 40-nm CMOS technology. The proposed chip has achieved maximum output power of 2 dBm with 3-dB bandwidth of about 20% (52~66 GHz and 106~132 GHz). The peak output power at 208~252GHz is -4 dBm and the 3-dB bandwidth is 32 GHz. The chip consumes 275 mW (all paths turn on) with an area of only 1.17 mm² including bonding pads. This is the first demonstration of a multi-channel active multiplier operating up to G-band with a compact chip size.

Keywords—CMOS, frequency multiplier, millimeter-wave, terahertz.

I. INTRODUCTION

In recent years, millimeter to sub-millimeter wave circuits have been utilized for a variety of new applications such as short-range communication, radar, and imaging [1,2]. Besides, sub-terahertz integrated circuits offer a number of emerging applications, which include a new ultra-high data rate communication system such as B5G and 6G, a high-resolution imaging or gesture sensors. With the silicon technology scaling, advanced CMOS and SiGe technology result in the maximum oscillation frequency (f_{\max}) of the transistor over 300 GHz and 500 GHz, respectively. Therefore, the sub-terahertz source above 100 GHz can be implemented using a LC based fundamental oscillator, push-push oscillator, and passive or active frequency multipliers. The active multipliers provide a high output power and a stable source generation with a wide tuning range compared to the other methods, even though they exhibit a high-power consumption and a poor phase noise performance which degrades at the order of the square of the multiplication factor. Most commercialized millimeter-wave transceivers [3] and frequency extension modules [4] are adopted to the frequency multiplication method. But the extension modules generate only single output frequency using an input signal source.

In this paper, a multi-channel active multiplier is demonstrated in a single CMOS chip. The circuit generates V-to G- band signals simultaneously with sufficient output power and bandwidth.

II. CIRCUIT DESIGN

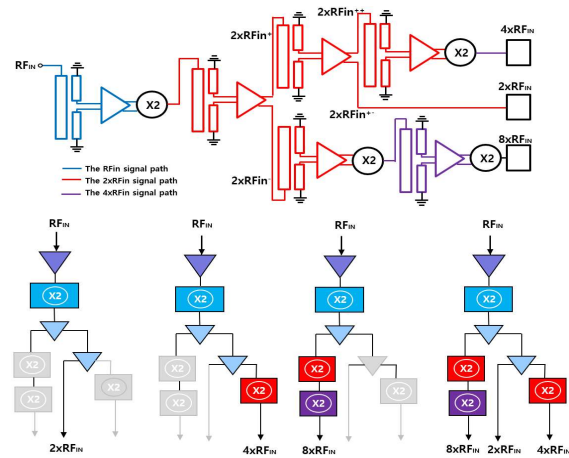


Fig. 1. The block diagram and four operation modes of the proposed multi-channel frequency multiplier.

The circuit converts the input frequency to three different output frequencies, corresponding to two times, four times and eight times the input frequency, as shown in Fig. 1. Initially, a center frequency of approximately 30 GHz is applied to the input port (RF_{in}), and the signal is first converted to 60 GHz through the first frequency doubler stage which comprises the 30 GHz driver amplifier and doubler core. The subsequent differential amplifier amplifies the 60 GHz signal and splits it into two differential signals, which can operate as an active power divider [5]. This configuration produces a broadband gain response due to the termination of each path with the input of the marchand balun.

The positive signal ($2xRF_{in+}$) is amplified by the same differential amplifier, and one of the outputs ($2xRF_{in-}$) is connected to the output pad ($2xRF_{in}$) using a 50Ω microstrip line. The other output ($2xRF_{in+}$) is then amplified and converted to the $4xRF_{in}$ frequency (120 GHz) through the frequency doubler. The negative 60 GHz signal ($2xRF_{in-}$) is applied to the two cascaded differential active frequency doublers, resulting in $8xRF_{in}$ output frequency (240 GHz). As a result, the circuit can provide three independent frequencies in parallel using a single input signal. Each active multiplier chain can be reconfigured depending on control of the amplifiers. Therefore, the outputs can be operated

simultaneously when all active components turn on. Alternatively, one or two outputs can be generated depending on the state of the differential amplifiers. For example, if the bottom path, which goes from $2xRF_{in-}$ to $8xRF_{in-}$, is turned off, the circuit will only provide $2xRF_{in}$ and $4xRF_{in}$ signals.

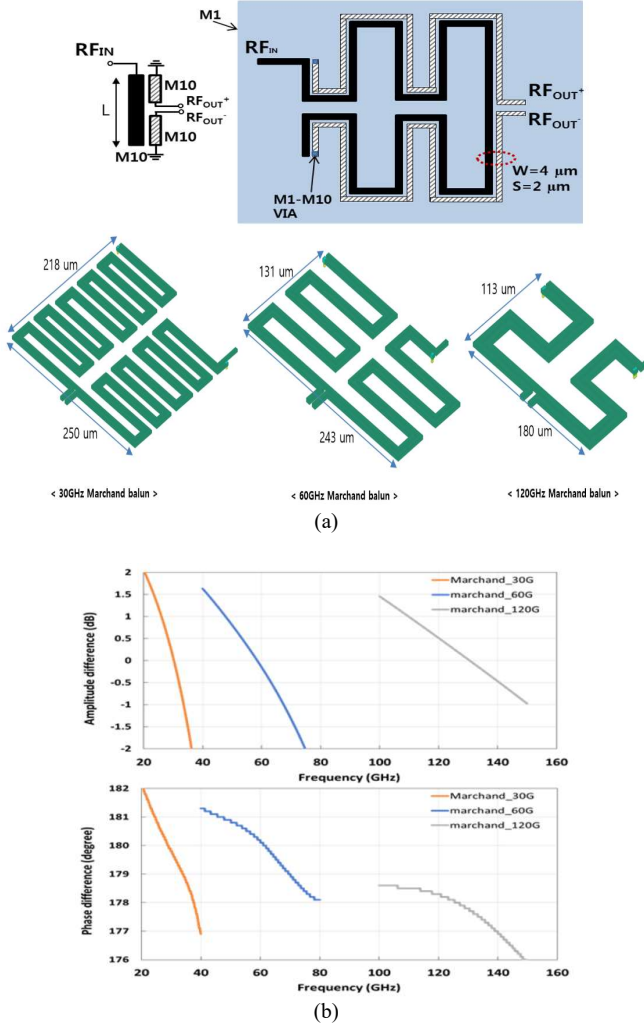


Fig. 2. (a) The meandered marchand balun structure (b) the simulated amplitude and phase differences for three marchand balun.

The circuit is implemented in a standard 40-nm RF CMOS process with 1-poly and 10-metal layers featuring a peak f_T of around 300 GHz. All passive components such as microstrip line, metal-oxide-metal (MOM) capacitor, and inductors are simulated using Keysight, ADS Momentum. As shown in Fig. 2(a), three different marchand baluns are designed with a meandered coupled microstrip using a top-level metal with the thickness of $3.5 \mu m$. The spacing between coupled lines is $2 \mu m$, which is limited by the design rule of the foundry. The coupled lines are meandered to minimize the circuit area; the effective length (L) of each balun, which represents half of the wave length, is around 2.8 mm, 1.4 mm, 0.7 mm for the designed frequencies of 30 GHz, 60 GHz, and 120 GHz, respectively. Fig.2(b) shows the simulated amplitude and phase imbalances

for each marchand balun. For a 20% fractional bandwidth, the amplitude and phase differences show maximum values of 0.8dB / 0.8° , 0.8dB / 0.6° , and 1.1dB / 2.4° in the frequency ranges of 27-33 GHz, 54-66 GHz, and 108-132 GHz.

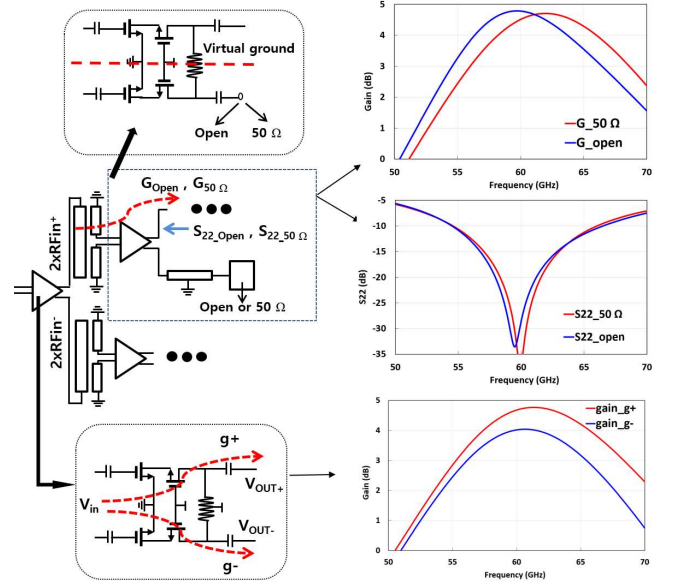


Fig. 3. The operation and simulation results of the active divider: nominal gain difference and port impedance/gain change depending on the condition of a termination.

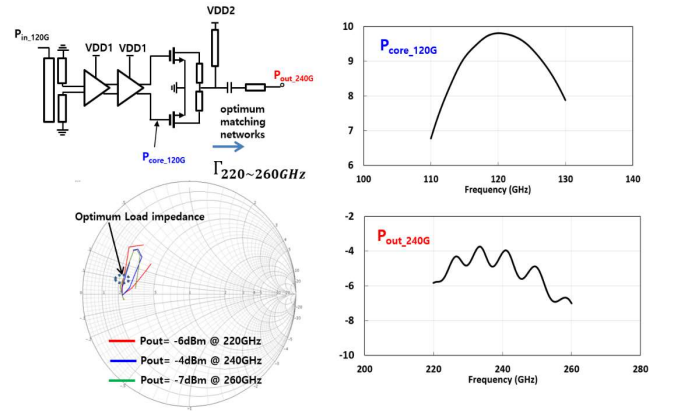


Fig. 4. The schematic of the 240 GHz doubler, harmonic load-pull simulation for optimum load impedance, and simulated driving (P_{core}) and output power.

The first active divider is a single-stage differential cascode amplifier, which exhibits a wideband gain response because the two outputs are terminated with a marchand balun. Fig.3 shows the simulated gain curves of the two paths when each output is terminated with a 50Ω load resistor. The active divider achieves a gain of 2~5 dB and a gain fluctuation of less than 2 dB over the range of 54 – 66 GHz.

The upper signal path ($2xRF_{in+}$), which is followed by another active divider, is split into two parts: one leads to the 60 GHz output pad, while the other goes through an additional doubler to produce a 120 GHz output. Since only one of the

three outputs can be activated at a time, the output pad of the 60 GHz path is either left open or loaded with a 50 Ω .

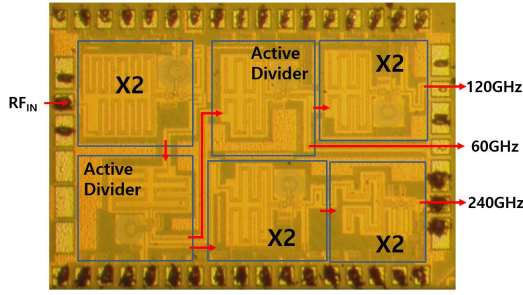


Fig. 5. The die photo of the multi-band active frequency multiplier. The size is 1.17mm² including the pads.

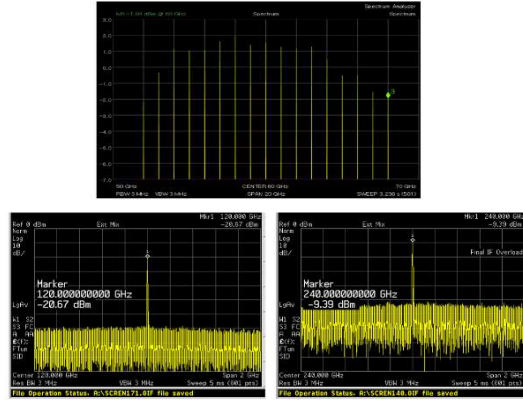


Fig. 6. The measured spectrum for each output path: 60 GHz, 120 GHz, and 240GHz.

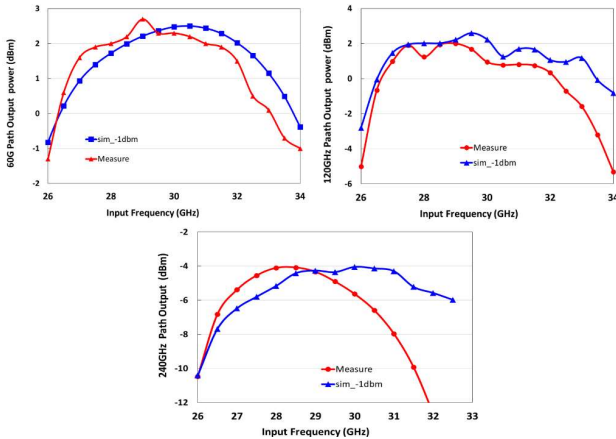


Fig. 7. The simulated and measured output power versus input frequency at the input power of around -1 dBm.

Conventional Wilkinson dividers are susceptible to changes in their loss and matching characteristics depending on the termination impedance of each port. In contrast, the two outputs of the active divider are ideally isolated from each other due to the differential inductor between the drain nodes that provides a virtual ground. As a result, one of the outputs maintains the gain and matching performance regardless of the load condition of the other port. Fig.3 shows the gain and matching variations of the output pad of the 60 GHz path, depending on the load impedance (open or 50 Ω). The gain variation is less than 1dB

and the output impedance is almost identical in the 50-70 GHz range. The simulated stability of the active divider indicates stable operation (k -factor > 1) for the both termination conditions.

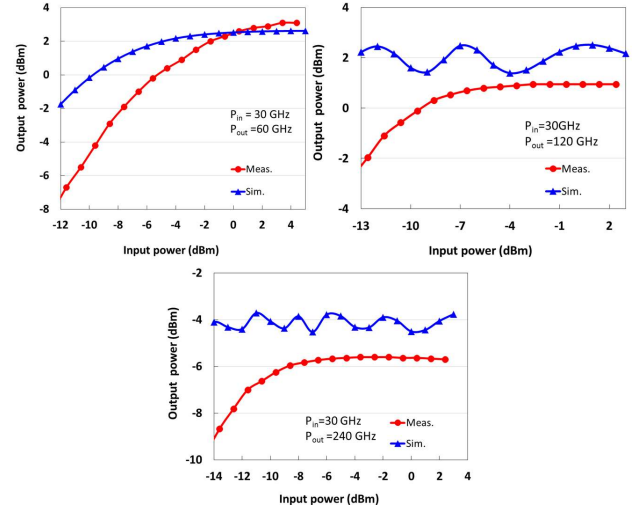


Fig. 8. The simulated and measured output power versus input power at the input frequency of 30 GHz.

All of the frequency doublers consist of a differential drive amplifier, a doubler core, and a 2nd harmonic matching network. Fig.4 shows the schematic and simulation results for the 240 GHz frequency doubler, which utilizes a two-stage differential amplifier to enhance the driving power delivered to the doubler core.

The doubler core operates in class B mode by setting the gate voltage to 0.3V. It is designed to cover wideband 2nd harmonic power in the designed frequency ranges. First, the driver stage provides enough fundamental power in a fractional bandwidth of 20%. Second, the optimum matching circuit of the doubler core is determined by conducting a harmonic load-pull simulation, which generates a load impedance curve for constant 2nd harmonic power. The simulation is carried out for three output frequencies: 220 GHz (-6 dBm), 240 GHz (-4 dBm), and 260 GHz (-7 dBm). The crossing point of the three different curves provides the optimum impedance for the half-power bandwidth. The simulation results show that the fundamental power delivered to the doubler core is less than 10 dBm and the 2nd harmonic power generates a maximum of -4 dBm in 220-260 GHz. The other two doublers (60 GHz and 120 GHz) have the same topology, but the driver amplifier uses a single stage cascode structure. The input port is matched to 50 Ω , and the simulated return loss is less than 16 dB from 26 GHz to 34GHz. Each output port is matched to the optimum load impedance to deliver the maximum output power.

III. MEASUREMENTS

The photo graph of the fabricated chip is shown in Fig.5, with the area of 1.3 x 0.9 mm² including bond pads.

This exhibits a multi-functionality and a high integration level compared to other conventional active frequency multipliers. The chip was on-wafer characterized using a GSG

Table 1. Summary and comparison table of active frequency multipliers over 100 GHz.

| Ref. | Process | Multiplication Factor | Frequency (GHz) | 3-dB bandwidth (%) | Pdc (mW) | Psat (dBm) | Chip area (mm ²) |
|-----------|-------------|-----------------------|-------------------------|----------------------------------|----------|------------|------------------------------|
| [6] | 130-nm SiGe | 6 | 115~144 | 22.3 | 310 | 4.5 | 0.55 |
| [7] | 65-nm CMOS | 9 | 117~129.3 | 10 | 328 | 6.3 | 0.49 |
| [8] | 130-nm SiGe | 16 | 235~275 | 15.6 | 300 | -8.5 | 0.7 |
| [9] | 130-nm SiGe | 4 | 250~260 | 5 | 22.4 | -8.4 | 1.02 |
| This work | 40-nm CMOS | 2, 4, 8 | 52~66, 106~132, 211~252 | 20(30 GHz, 60 GHz), 14 (240 GHz) | 275 | 2, 2, -4 | 1.17 |

coaxial probe for the 52 ~ 68 GHz band and waveguide (WR8.0 and WR3.4) probes for the 120 GHz and 240 GHz bands. Both the output power and spectrum of the 60 GHz path were directly measured using a MS2760A spectrum analyzer from Anritsu. Above the frequency range of 100 GHz, the power measurement was done with an Erickson PM5 calorimeter and the frequency spectrum was measured using a VDI sub-harmonic mixer, which down-converts the signal to the spectrum analyzer. The measured spectrum for each path is shown in Fig.6.

The circuit operates with 1.8 V power supply for all active divider and driver amplifiers and 1.1 V supply for each doubler core. When all paths turn on, the chip in total consumes only 275 mW (70 mA from 1.1 V and 110 mA from 1.8V). The circuit achieves maximum output power of 2 dBm, and 3-dB bandwidth of about 20% (52~66 GHz for the 60 GHz path, 106~132 GHz for the 120 GHz path).

The peak output power for the 240 GHz path is -4 dBm and the 3-dB bandwidth is 32 GHz corresponding to a fractional bandwidth of 14%. About -1 dBm of external signal source in 25 ~ 34 GHz is applied to the circuit for power versus frequency measurement, as shown in Fig. 7. There is excellent agreement between the simulation and the measurements. Fig. 8 presents the output power versus input power level at a fixed frequency of 30 GHz. The 60 GHz output begins to saturate at around -2 dBm of input power, whereas this saturation is at about -10 dBm of input power for the 120 GHz and 240 GHz output. All saturated power is almost the same as the simulation value, within a 1 dB error range. However, the output power is lower than the simulation for the low input power because the drive amplifier gain is shifted to a lower frequency. The simulated output power fluctuation results from the low harmonic number setup of the harmonic balance simulator due to the limit of the EM simulation frequency up to 300 GHz. Table I compares the results from active multiplier chains with different multiplication factors over 100 GHz. The proposed chip generates three independent frequencies simultaneously with sufficient output power over a wide bandwidth.

IV. CONCLUSION

A compact multi-channel frequency multiplier is presented for the signal generation from millimeter-wave to terahertz frequencies. Although the frequency multiplication degrades the phase noise of the input signal by $20\log_{10}N$ dB, where N is multiplication factor, which corresponds to 2,4 and 8 for each output port, respectively, the proposed chip exhibits three independent output frequencies in parallel from 54 to 252 GHz with a separate mode and simultaneous mode from the Ka-band input frequency. Each output frequency covers a fractional bandwidth of 14 ~ 20% with sufficient saturated output power. This is the first demonstration of multi-channel active frequency multiplier operating up to 252 GHz in a standard CMOS technology.

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