A 450W GaN-Based Limiter for S-Band Applications

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***Abstract*—This paper describes the design and characterization of a compact robust two-stage MMIC GaN Power Limiter using Cold FETs and Schottky Diodes. The limiter design is based on 0.15-µm GaN technology and can handle up to 450 W pulsed input power over the 2.6-3.6 GHz frequency band associated to a recovery time lower than 200 ns and a very low small signal insertion loss of 0.6 dB. To the authors knowledge, this is the highest power handling capability ever achieved on MMIC GaN based limiters.**

***Keywords*—High Power Limiter, Cold FET, GaN, S-Band, MMIC**

I. Introduction

The multiplication of MIMO systems to create beam-formers for various applications (telecommunications, radar systems, IoT...), leads to integrate multiple transceivers (Tx) closer to receivers (Rx).Therefore, receivers are more and more exposed to high input power levels caused by power leakage from Tx to Rx (antennas mismatches) or by aggressive signals of jammers (electronic warfare).

In usual frontend architectures, LNAs used in Rx channels are generally made of GaAs technologies to benefit from their low noise levels. However, these technologies cannot sustain high input power overdrive due to their low breakdown and need to be protected.

At the opposite, GaN transistors provide high power handling capability due to the GaN wide bandgap. Very high breakdown voltage can be achieved compared to GaAs counterparts. Considering the noise performance, GaN recent advents are starting to challenge GaAs Noise Figure performances [1]- [2]. The integration of GaN robust LNAs including a limiter stage upstream of the amplifier would be a disruptive solution to increase integration density. Furthermore, these GaN limiters would protect receivers from any unwanted high power level signals. Finally, the main objective would be the implementation of all Rx and Tx channels on the same MMIC to reduce the total cost of the system as well as increasing the integration density and chip performances.

This paper presents a compact 450-W S-Band MMIC Limiter developed on a 0.15-µm gate length technology showing state of art performances for S-band GaN integrated limiters. The technology used, the design methodology, the simulation and the measurement results are described.

II. GH15 GaN Technology

This technology is a space evaluated technology based on AlGaN/GaN epitaxy on 4-inch SiC substrate. It features a 150-nm T-shaped gate in combination with Source-Terminated Field-Plate transistors for power applications and single symmetrical T-shape gate transistors for switching operation. The substrate is thinned to 70 µm by means of a back-side process that ensures the compatibility with both soldering and high thermal conductivity epoxy based assembly processes. Nonlinear Cold-FET model for switching applications is available in the Design Kit, it uses an empirical model developed internally to ensure fast and accurate simulations. The key parameters are summarized in Table 1.

Table 1 . GH15 GaN Technology Main Characteristics

Parameter	**Typ. value**
Cut-off frequency (f_T)	35 GHz
RF power density @ 30 GHz	3.5 W/mm
IDS++@VD=7 V, VG=2 V	1.4 A/mm
GmMax@ VD=7 V	390 mS/mm
Vpinch-off@VD=7V Ids=Idss/100	-3.2 V
Drain-source voltage bias	25 V
Leakage current@VD=7V	< 200 µA/mm

III. Limiter design

A. Unit Limiter Cell

The GaN Power Limiter is based on a unit limiter cell represented in Fig. 1. This cell is composed by a cold FET with two serial diodes between the Drain and the Gate of the FET.

"Vg_block" is the biasing voltage of the cell and its value is selected to fix the trigger level of the limiter. This access is high impedance: the transistor must be pinched-off and the diodes must also be blocked by choosing the best trade-off between their knee voltage and their number in series.

"In_drain" is the input signal of the limiter and must be connected in parallel to the circuit to be protected, this access must be DC-grounded in order to keep the transistor characteristic (gate-controlled resistor) in large signal.

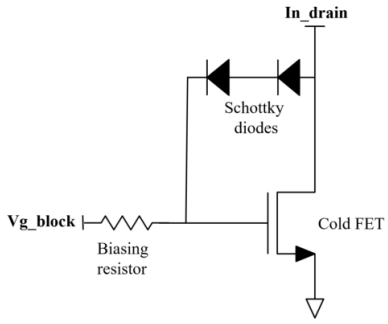

Fig. 1. Principle schematic of a GaN unit limiter cell.

The OFF-state of the unit limiter cell, in small signal mode, can be approximated by a resistor Roff in parallel with a capacitor Coff as depicted in Fig. 2 (a).

The ON-state of the limiter, in large signal mode, can be considered as a simple resistor (in the low impedance range) with a value decreasing when the input power increases. The final value (Ron, Fig. 2 (b)) is obtained when the maximum ratings of the transistor are reached

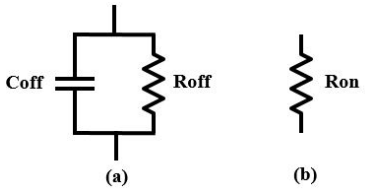

Fig. 2. Equivalent electrical schematic of the unit limiter (a) off- state (b) on-state.

B. Full-MMIC GaN Limiter Design

The principle schematic of the entire limiter is represented on Fig. 3. Two limiter stages are used in order to reach high isolation in large signal mode.

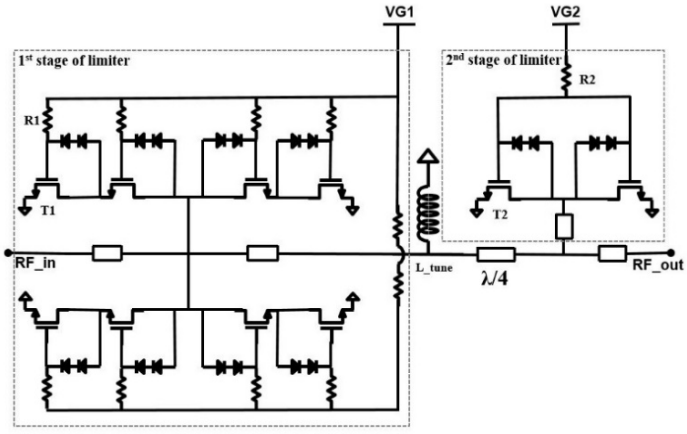

Fig. 3. Full-MMIC GaN limiter principle schematic.

The first design step consists in sizing the first limiting stage to handle the maximum input power targeted. One of the main objectives is to reflect the maximum of injected power to the source in order to protect the Rx chain without dissipating too much power.

For large signals, the limiter can be seen as a resistor Ron which value must be minimized to maximise the reflected power and by consequence to increase the isolation to LNA. As the main limitation of the limiter cell is the RF current density, the sizing consists in adapting the gate development to the necessary current induced by the maximum specified input power.

As seen in part III.A, the whole limiter, in off-state case, can be seen as a capacitance Coff with a parallel resistor Roff. As the first stage has the main contribution to the small signal performances, the design goal of the first stage is also to minimize Coff1, in order to obtain the widest frequency band, and to maximise Roff1 to obtain the lowest insertion losses.

A trade-off has then to be found between the power capability of the limiter, its bandwidth and its insertion losses. The most efficient solution was to minimize the gate development to support the RF current (vs maximum ratings) without too much margin and by consequence optimize Coff1 and Roff1. Because of the high total gate length of the first stage, sized to sustain at least 250W, the Coff1 is partly compensated by the inductor "Ltune". The power behaviour at 3 GHz of one of the transistor of the first stage is shown on Fig. 4. The current density does not exceed the saturation current density of the technology which is 1.5 A/mm and by consequence the peak drain voltages remain very low.

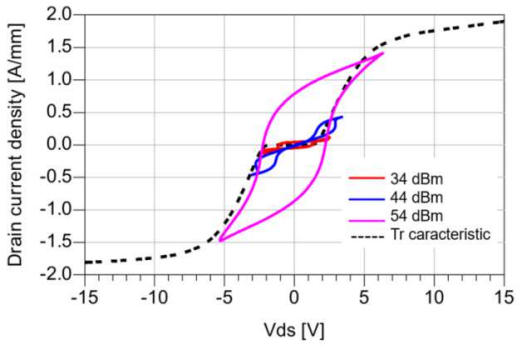

Fig. 4. 1st stage Transistor simulated load cycles for multiple input power.

In addition with the transistor load cycle, a simulation of the transistor junction temperature is shown on Fig. 5. Thanks to SiC thermal properties and a high reflection coefficient, the transistor junction temperature is, in CW mode, below the Recommended Operating Ratings of 200°C giving margin on power handling.

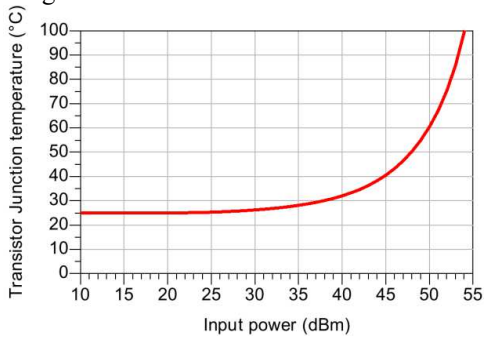

Fig. 5.Simulated First stage transistor junction temperature at 25°C backside temperature, in CW mode.

The next design step consists of second stage total gate development choice. The second stage (clean-up stage) dimension will define the flat power leakage level of the limiter. The objective is then to add isolation from the output first stage with less constraint from power. A quarter-Wavelength line (λ/4) is placed between the stages in order to maximize the impact of the second stage. During this step, another trade-off is made between insertion losses versus power leakage of the limiter.

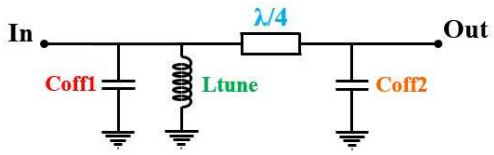

Fig. 6. Simplified small-signal schematic of the GaN limiter.

IV. LIMITER MEASUREMENT

A. *Small signal performances*

Small signal measurements have been performed directly on-wafer for accuracy purpose. Fig. 7 and Fig. 8 show S-parameters measurements of 10 dies obtained in CW mode compared to simulation with design kit in CW mode for VG1=VG2= -5 V at ambient temperature.

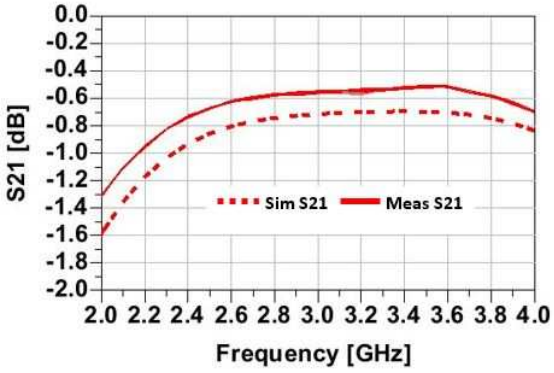

Fig. 7. Measurement and simulation of limiter insertion loss (S_{21}).

Over the 2.7 to 3.8 GHz, the GaN limiter exhibits insertion losses less than 0.6-dB (Fig. 7).

A difference inferior to 0.2 dB is observed between simulation and measurement results. This is partly due to the slight Roff discrepancy of the non-linear cold FET model used during the design phase.

In addition to these low insertion losses, a minimum of 13 dB of input Return Loss and 15 dB of output Return Loss are measured (Fig. 8).

Finally, the comparison between simulation and measurement shows excellent agreement thanks to a good model accuracy. Yet, excellent reproducibility is observed on 10 dies measured.

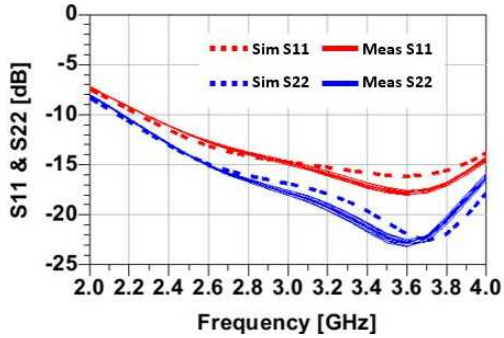

Fig. 8. Measurement and simulation of limiter S-parameter (S_{11}, S_{22}).

B. *Large signal performances – Robustness behaviour*

For large signal measurements, MMICs were mounted on a molybdenum carrier for thermo-mechanical purpose (Fig. 9). Chip size is 2.5mm × 2mm.

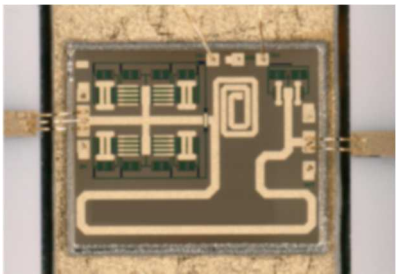

Fig. 9. GaN Limiter in test fixture.

Pulsed power measurements have been performed to confirm leakage, triggering and robustness performances of the limiter. Pulsed width used is 15% on a few millisecond period (<10ms). Fig. 10 shows the power measurements on one MMIC in test fixture at ambient temperature (25°C).

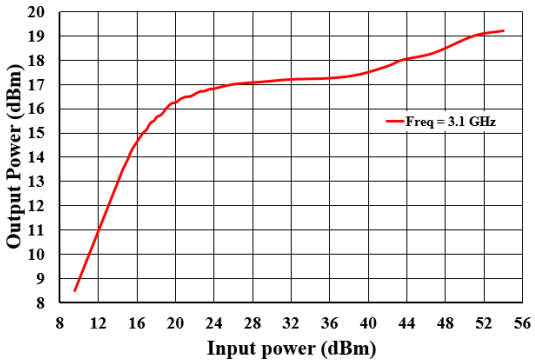

Fig. 10. Measurement of limiter power characteristic.

Limiter shows power leakage lower than 20 dBm all over the S-Band frequencies. Triggering level is around 16 dBm of input power and shows less than 1 dB variation over the bandwidth. During hard limiting, diode current do not exceed recommended operating region with a current lower than 8 mA.

An additional RF stress step test (RFSST) has been performed at 75°C to evaluate the robustness of the limiter. Input power has been increased from 150W to 450W (pulsed) in steps of 10W every 10 min without any performance or structural degradations. A small signal measurement has been

done after the RFSST to confirm nominal small signal performance.

Furthermore, amplitude recovery time has been measured and is shown on the Fig. 11. Recovery time characterizes the capability of the receiver to be operational after the triggering of the limiter. Significantly, recovery time is negligible until 440W and is around only 200ns at 450W which compare favourably well to traditional GaAs based PIN diode limiters.

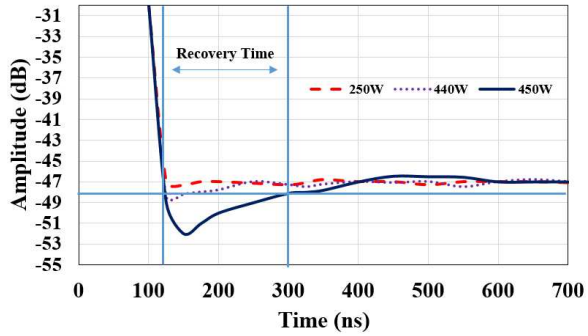

Fig. 11. Amplitude recovery time measurement.

This limiter achieves higher power performance in S-Band compared to State of the art GaAs limiter [3] and outperforms existing GaN limiter [6] in term of insertion loss, output power leakage, power handling and recovery time.

Table 2: State of the art of S-Band integrated limiters.

Ref.	Technology	Freq (GHz)	Limiting cell	Pmax (W)	Insertion Loss (dB)	Leakage (dBm)
[3]	GaAs	2-5	VPIN diodes	100 (CW)	0.5	16
[4]	BiCMOS	3	PIN diodes	63 (P)	0.5	20
[5]	GaAs	3-28	VPIN diodes	4 (CW)	0.39	17
[6]	GaN	1-6	FET	50 (CW)	0.6	22
This work	**GaN**	**2.6-3.6**	**Cold FET + Schottky diodes**	**450 (P)**	**0.5**	**<20**

V. Conclusion

The design and measurement results of a robust high power two stages GaN limiter processed on 0.15 µm gate-length GaN HEMT technology is presented.

On-wafer small signal measurements exhibit low insertion losses (< 0.6 dB) combined with good input and output return losses (> 13 dB and > 15 dB respectively). Pulsed measurements in text fixtures demonstrate a state-of-the-art power robustness around 450 W of input power with no degradation of the small signal performances and a very low recovery time <200 ns at 450W of pulsed input power. To the authors knowledge, this is the highest power handling capability ever achieved on MMIC GaN based limiters. These results are promising for the future of GaN integration in Rx/Tx systems.

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References

[1] K. W. Kobayashi, C. Campbell, C. Lee and J. Gallagher, "A Reconfigurable S-/X-Band GaN Cascode LNA MMIC," *IEEE Compound Semiconductor Integrated Circuit Symposium,* 2017.

[2] K. W. Kobayashi, V. Kumar, C. Campbell, S. Chen, Y. Cao and J. Jimenez, "Robust-5W Reconfigurable S/X-band GaN LNA using a 90nm T-gate GaN HEMT Technology," *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS).*

[3] J. Bouchez, T. Nguyen, V. Zomorrodian, R. Eli and D. Sturzebecher, "A 2-5GHz 100W CW MMIC Limiter using a Novel Input Topology," *IEEE Compound Semiconductor Integrated Circuit Symposium,* 2013.

[4] M. van Wanum and F. E. van Vliet, "A 58-dBm S-Band Limiter in Standard 0.25-um BiCMOS Technology," *IEEE Transactions on microwave theory and techniques,* 2013.

[5] J. M. Carroll, "Performance Comparison of Single and Dual Stage MMIC Limiters," *IEEE MTT-S Int. Microw. Symp. Dig.,* vol. 2, pp. 1341-1344, 2001.

[6] C. F. Campbell, J. C. Hitt and K. Wills, "Wideband GaN FET based limiter MMICs," *7th European Microwave Integrated Circuit Conference,* 2012.