Antenna-Coupled Terahertz Detectors in 16nm FinFET

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***Abstract*—This paper presents an on-chip antenna-coupled terahertz (THz) power detector implemented in a 16nm FinFET technology. The detector takes advantage of the transistor nonlinearity to output a rectified DC signal proportional to the input THz signal power. Both a dipole and a folded dipole antenna are designed on-chip to characterize the detectors from 170-700GHz. The detectors achieve a maximum responsivity of 88.8kV/W and NEP 8.7pW/$\sqrt{Hz}$ at 554GHz for the dipole-coupled detector and 41.7kV/W and 18.4pW/$\sqrt{Hz}$ at 502GHz for the folded-dipole-coupled detector.**

***Keywords*—16nm FinFET, THz detector, dipole antenna, folded dipole antenna, antenna-coupled detector.**

I. Introduction

Shrinking transistor dimensions has been a driving force in the development of faster and more power efficient electronics in silicon technologies. The fin field-effect transistor (FinFET) technology has enabled further channel shrinkage with better device performance in comparison to planar FET technology. Both transistor characteristics (f_T/f_{max}) and a dedicated back-end-of-line (BEOL) metal stack are required to demonstrate high performance mm-wave and sub-mm-wave systems.

Terahertz detectors were demonstrated with Schottky diode mixers [1] or SiGe BiCMOS devices [2], [3], and planner CMOS technology [4], [5]. Despite providing a lower responsivity compared with other technologies, silicon FET detectors allow for better integration with subsequent readout circuitry. Recently, direct CMOS detectors were shown to achieve a minimum noise-equivalent power (NEP) on the order of 10-100pW/$\sqrt{Hz}$ in the sub-mm-wave region [3].

For an ideal rectifier detector, the minimum NEP is inversely proportional to the input power, so the antenna must be carefully designed to boost the efficiency and maximize the delivered power to the detector. On-chip antenna performance often suffers from the lossy substrate below the antenna. The strict design rules in advanced CMOS technology nodes also limit the achievable antenna layouts. Multiple techniques have been developed to improve the antenna gain, such as back-side reflectance [6] and back-side radiation with a silicon lens [7], [8].

The simplest antenna is a dipole antenna, which consists of two quarter-wave strips of conductive material that are driven by a differential input; however, when the dipole is integrated with either the receiver or transmitter, a bias must be provided, which can make the matching network more complex. One solution is to use a folded dipole instead, which works in a similar fashion to the half-wave dipole. The folded dipole's symmetry can be exploited to provide DC biases at the AC ground without degrading the folded dipole performance.

In this paper, we present both a dipole-coupled and folded-dipole-coupled THz power detector in a 16nm FinFET process. The on-chip dipole and on-chip folded dipole antenna are designed in the top layer metal of the BEOL stack. Section II describes the detector and antenna design methodology and provides simulation results. Section III presents the measured performance results and Section IV draws a conclusion.

II. Design and Simulation

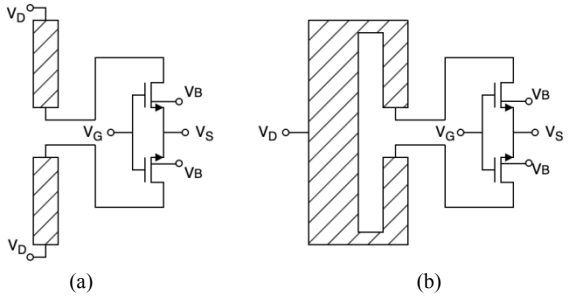
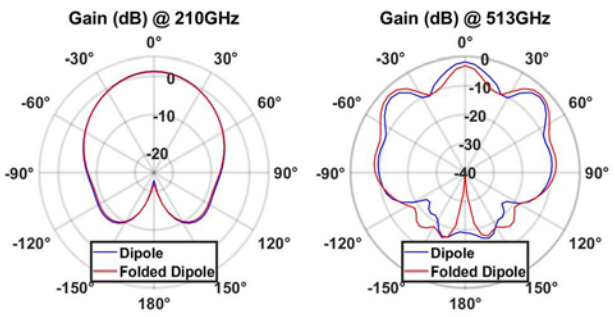


Fig. 1. Common gate detector coupled to (a) a dipole antenna and (b) a folded dipole antenna

Power detectors exploit the active device nonlinearity in order to extract a rectified DC output from the input RF signal. An N-FinFET common gate structure coupled to a dipole and a folded-dipole antenna is designed as shown in Fig. 1. The design symmetry introduces an AC ground at the output, eliminating the need for complex RF blocks. The other advantage of such a structure is the broadband response across a wide range of frequencies. Compared with a diode rectifier, the common gate architecture provides an additional tuning node at the gate. By tuning this gate bias node, we can reduce the effective V_T seen by the RF signal, thus optimizing the detector's responsivity.

Since the detectors' response is measured as antenna-coupled detectors, both the dipole and the folded dipole antenna are carefully modelled in a full-wave electromagnetic simulator. To accurately model the antennas, a ground plane is added below the substrate for all simulations, which models the PCB board that the chip will be on. The simulated gain peaks at 1.3dB for the dipole and 1.1dB for the folded dipole at 210GHz. Additional modes are apparent at higher frequencies because of the resonant nature of both antennas and substrate modes. This resonant behaviour enables the detector to measure up into the THz frequency range. The E-plane radiation pattern for both antennas at 210GHz and 513GHz is plotted in Fig. 2.



(a) (b)

Fig. 2. Simulated E-plane radiation for the dipole and folded dipole at (a) 210GHz and (b) 513GHz

III. Measurement Results

The main performance metrics for detectors are their responsivity (R_V) and NEP. At THz frequencies, it is not practical to electrically inject input signals to the detector because of the high cost of THz probes and the uncertainty of insertion loss from the source to DUT, which makes it difficult to accurately calibrate. Instead, THz detectors are generally configured as antenna-coupled detectors, where the free space loss from the THz source to the detector is calculated to measure the received power. Given a source power P_T, source antenna gain G_T, and receiver antenna gain G_R, the delivered power P_{in} received by the THz detector at a distance R in the far-field from the source is given by

$$P_{in} = \frac{P_T G_T G_R \lambda^2}{(4\pi R)^2}. \quad (1)$$

The responsivity of the detector, a measure of the detector gain, is defined as

$$R_V = \frac{V_{out}}{P_{in}}, \quad (2)$$

where V_{out} is the measured DC output voltage of the detector. The NEP, a measure of the sensitivity of the detector, is a ratio of the detector output noise V_n and its responsivity, which are both functions of the input power level and input frequency.

$$NEP = \frac{V_n}{R_V} \quad (3)$$

The chip microphotograph of the antenna-coupled detectors is shown in Fig. 3. Custom metal fills required by FinFET layout rules are manually added around the antennas in order to reduce their impact on the antenna performance. In order to measure the detector, a VDI WR9.0 AMC multiplier chain kit with horn antennas covering the entire frequency range of interest is used as the source. A chopping frequency of 1kHz is used to modulate the input source. The detector output is then amplified through an SR560 low noise voltage pre-amplifier and measured with an SR830 lock-in amplifier. The measurement setup is shown in Fig. 4.

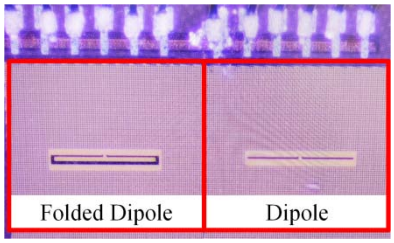


Fig. 3. Chip microphotograph

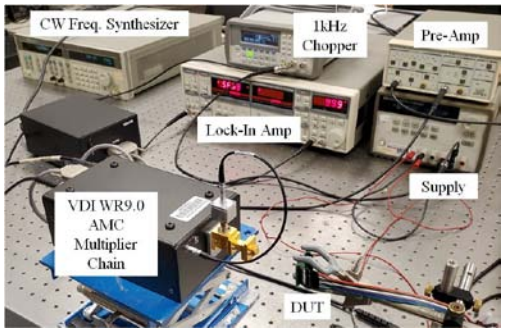


Fig. 4. Measurement setup

In order to calculate the received power of the detector, the source output power is measured with a VDI PM4 power meter at each frequency band. A summary of the VDI harmonic multipliers used, their corresponding antenna gain, and measured power are listed in Table 1. For the receiver gain of the detector, the antennas are carefully simulated in HFSS to model the metal conduction losses, effects of the ground plane below the antenna, the fringing boundary effects, and surface mode losses at the interface between the silicon chip and air.

Table 1. Source output power, horn antenna gain, and free space distance for detector characterization

Band	Frequency Range (GHz)	Output Power (mW)	Antenna Gain (dB)	Distance (mm)
WR4.3	170-250	1.26 - 3.66 (+/- 0.01)	21	129
WR2.8	260-400	0.263 – 1.252 (+/- 0.001)	26	49
WR2.2	330-500	0.023 – 0.21 (+/- 0.001)	26	42
WR1.5	500-750	0.0051 – 0.0617 (+/- 0.0005)	26	36

The bias point of the detector will heavily affect its responsivity. For a fixed frequency, the gate bias voltage is swept from 0 to 0.8V to find the optimum bias point (Fig. 5). Given this optimum bias, the responsivity over frequency is measured for the detector in Fig. 6, achieving a peak responsivity of 121kV/W at 589GHz for a dipole-coupled detector and 74.5kV/W at 560GHz for a folded-dipole-coupled detector.

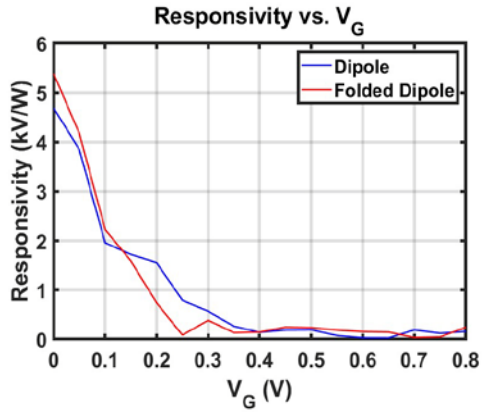


Fig. 5. Measured responsivity at different gate bias voltages at 460GHz

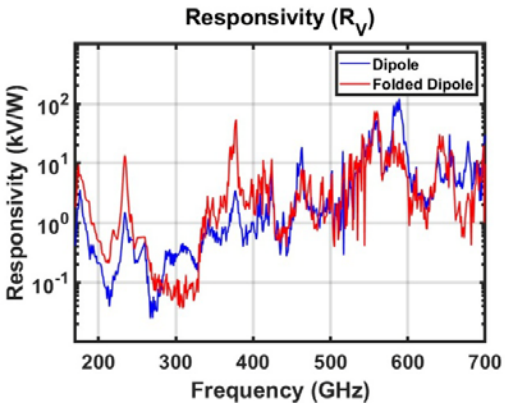


Fig. 6. Measured responsivity vs. frequency

The flicker and thermal noise of the transistor are both functions of the drain current, so when the bias voltage is tuned, the injected noise will change accordingly. The detector output noise at different bias voltages is plotted in Fig. 7. From the figure, there is a tradeoff between the detector responsivity and noise.

The detector antenna gain may be calculated using the effective area of the aperture or pixel size ($354.5\times5\mu m^2$ for the dipole and $354.5\times30\mu m^2$ for the folded dipole). For this work, we defined the effective area as the physical area of the antenna as:

$$G_R = \frac{4\pi}{\lambda^2} A_e \tag{4}$$

Using this gain, the measured responsivity and NEP of the dipole-coupled detector are 88.8kV/W and 8.7pW/$\sqrt{Hz}$ at 554GHz. The responsivity and NEP of the folded-dipole-coupled detector are 41.7kV/W and 18.4pW/$\sqrt{Hz}$ at 502GHz.

If the simulated antenna gain is considered, the measured minimum NEP of the detector across the entire frequency range is shown in Fig. 8, reaching an absolute minimum of 5pW/$\sqrt{Hz}$ at 589GHz for a dipole-coupled detector and 8.2pW/$\sqrt{Hz}$ at 560GHz for a folded-dipole-coupled detector, respectively. Their performance difference can be attributed to the higher impedance of the folded dipole compared to the half-wave dipole, which provides a greater impedance mismatch to the detector, effectively reducing the antenna efficiency. Comparing against prior terahertz detectors in Table 2, the presented detectors can achieve a higher responsivity and comparable NEP. This discrepancy in the frequency of the optimal performance can be explained by the resonant behavior of the antennas, which is not considered when calculating the effective area of the pixel. In addition, the drop in performance in this case is because of the reduced efficiency of the antennas in capturing the incident energy on the pixel area.

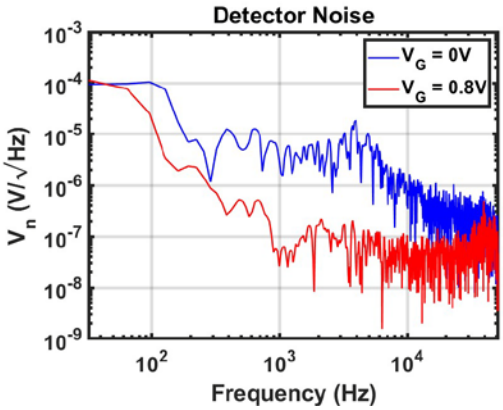


Fig. 7. Measured output noise at different gate bias voltages

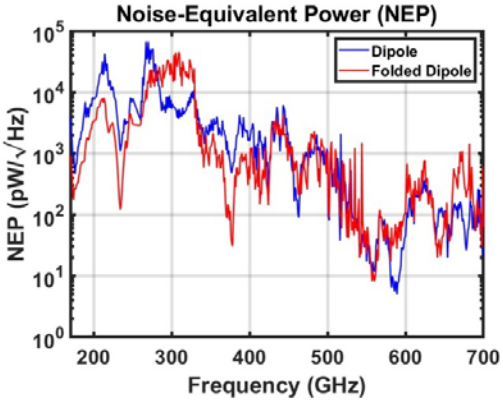


Fig. 8. Measured NEP vs. frequency

IV. Conclusion

In this paper, we have realized THz antenna-coupled detectors in 16nm FinFET technology between 170-700GHz. By taking advantage of the N-FinFET nonlinearity, the detectors can rectify the THz signal and produce a DC output proportional to the impinging THz signal power. On-chip dipole and folded dipole antennas are carefully designed and implemented for detector characterization to obtain a peak responsivity of 121kV/W and a minimum NEP of 5pW/$\sqrt{Hz}$ at 589GHz for a dipole-coupled detector, and a peak responsivity of 74.5kV/W and a minimum NEP of 8.2pW/ $\sqrt{Hz}$ at 560GHz for a folded-dipole detector. Accounting for the effective area, the dipole-coupled detector achieves a peak responsivity of 88.8kV/W and a minimum NEP of 8.7pW/$\sqrt{Hz}$ at 554GHz, while the folded-dipole-coupled antenna achieves a peak responsivity of 41.7kV/W and a minimum NEP of 18.4pW/$\sqrt{Hz}$ at 502GHz.

Table 2. Comparison table

	This work		IWMTS 2021 [9]	MIKON 2020 [10]	EuMIC 2019 [11]	EuMIC 2018 [4]	EDL 2016 [12]	IRMMW-THz 2016 [13]
Technology	**16nm FinFET**		InP Resonant Tunneling Diode	65nm CMOS	0.13μm SiGe HBT	22nm FDSOI	45nm CMOS	130nm NMOS
Antenna	**Dipole**	**Folded Dipole**	Spiral	Patch	Differential Ring + Lens	Differential Ring + Lens	Patch	Differential Ring + Lens
Frequency (GHz)	**589*/554**	**560*/502**	237.5	620	220-1000	855	781	650
Max R_V (kV/W)	**121*/88.8**	**74.5*/41.7**	1.248*	-	9	1.51/ 180mA/W[#]	0.558	0.45
Min NEP (pW/$\sqrt{Hz}$)	**5*/8.7**	**8.2*/18.4**	1.9*	12	1.9 @ 292GHz	22/12[#]	56	80

*Simulated receiver gain
[#]Current mode

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