A Compact *Ka*-Band Eight-Element Four-Beam Receiver for Low-Earth-Orbit Satellite Communications in 65-nm CMOS

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***Abstract*— This letter presents a *Ka*-band compact eight-element four-beam phased-array receiver to improve communication capacity for millimeter-wave satellite communications. To address the design challenge of the large area induced by the multibeam forming, the receiver utilizes a digital-assisted variable-gain phase shifting technique and an active combining scheme to enable compact implementation and facilitate array design. The receiver achieves a 360° phase shifting range with a 6-bit resolution and a 25-dB attenuation range with a 0.5-dB step. The measured root mean square (rms) phase and amplitude errors are 1.1° and 0.11 dB at 29.5 GHz, respectively. Each element achieves a gain of 26.7 dB, a minimum noise figure (NF) of 3.7 dB, and an input-referred 1-dB gain compression point ($IP_{1\ dB}$) of −32.5 dBm. The proposed receiver demonstrates the state-of-the-art number of simultaneously reconfigurable beams with a compact size among millimeter-wave silicon-based beamformers.**

***Index Terms*— Multibeam, phased array, receiver front end, satellite communication, variable-gain phase shifter (VGPS).**

I. Introduction

THE emerging low-Earth-orbit satellite communication (LEO SATCOM) employs low-cost large-scale *K*- and *Ka*-band transmit and receive phased arrays and enables global high-speed Internet access, especially in low-connectivity-density areas [1], [2]. Multibeam capability is highly desirable for satellite terminals to realize multiuser concurrent communication and seamless beam switching, as shown in Fig. 1(a). However, conventional analog phased arrays only support single-beam operation. High power consumption and large area occupation of the multibeam front ends impede their deployment. To realize a two-element four-beam receiver, Peng et al. [3] utilized a symmetrical beam-distribution network, which, however, would introduce large insertion loss (IL). The active phase-shifting and combining architecture proposed in [4] can support reconfigurable multibeam operation; however, the limited gain tunability could not meet the dynamic-range (DR) requirement in a large phased array.

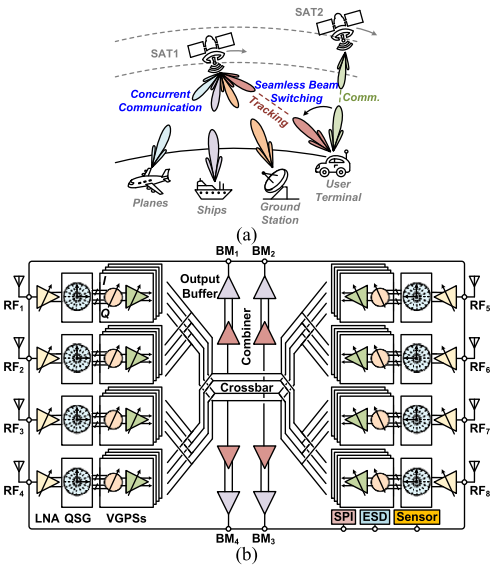

Fig. 1. (a) Multibeam forming enables concurrent communication and seamless beam switching. (b) Architecture of the proposed eight-element four-beam phased-array receiver front end.

Fully connected multibeam forming benefits the array performance by effectively utilizing the antenna aperture. Since the number of the integrated phase and amplitude tuning blocks (N_W) equals to the product of the number of elements (N_E) and the number of beams (N_B), it significantly expands the die size and mandates compact design. Besides, in the integrated phased arrays [1], [2], the pitch between adjacent elements (i.e., ≈λ/2) decreases as frequency rises. A smaller than half-wavelength die size is desired to facilitate the on-board signal routing and impedance matching. Hence, chip area occupation becomes a critical issue in the front-end design. To resolve this problem, we propose a digital-assisted variable-gain phase shifting technique and an active combining scheme and realize a compact *Ka*-band eight-element four-beam phased-array receiver in 65-nm CMOS.

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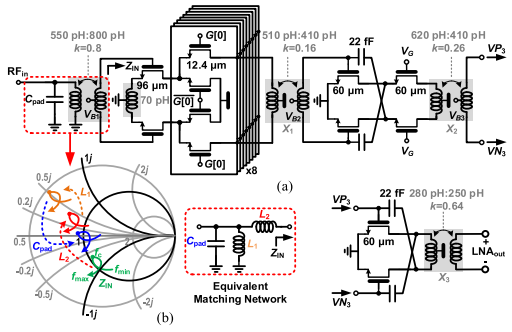

Fig. 2. (a) Schematic of the LNA. (b) Smith-chart representation of the wideband input matching scheme.

II. Eight-Element Four-Beam Receiver Design

A. Chip Architecture

Fig. 1(b) shows the block diagram of the proposed eight-element four-beam receiver front end. In each element, a high-gain low-noise amplifier (LNA) is employed to suppress the noise from the multibeam forming network. The quadrature signal generator (QSG) consists of a quadrature all-pass filter (QAF) and two buffer amplifiers and drives four parallel variable-gain phase shifters (VGPSs). Four active combiners and the tree-based crossbar connection network directly group and superpose 32 signals into four beams. Finally, four fixed-gain amplifiers serving as output buffers drive the OFF-chip 50 Ω. An environment sensor is integrated on the chip to monitor the process, voltage, and temperature (PVT) and compensate the receiver performance by programming bias currents and component values. A 256-byte serial peripheral interface (SPI) configures the receiver.

B. Low-Noise Amplifier

The complicated 32-to-4 beamforming matrix would inevitably induce large attenuation due to the transmission and combination loss. Therefore, a high-gain LNA is integrated in the front of each element, as shown in Fig. 2(a). The first stage adopts the source-degeneration cascode topology. Due to the loading effect of the magnetically coupled resonator (MCR) X_1, the input impedance $Z_{\rm IN}$ shows relatively lower value around the high and low end of the operating bandwidth, which facilitates the input matching [5], as shown in Fig. 2(b). The current-steering-based gain control scheme is applied to adjust the channel gain and input linearity. The second stage further boosts the voltage gain and utilizes the neutralized cascode topology to improve the reverse isolation and alleviate the stability concerns. The common-source (CS) third stage drives the QSG. Postlayout simulation shows that the LNA achieves a 30.5-dB gain and a 3.4-dB noise figure (NF) at 29.5 GHz. The simulated S_{11} is less than -20 dB from 25.9 to 35 GHz.

C. Digital-Assisted VGPS

In each element, the QAF of the QSG sets the reference for the four-beam phase interpolation and the buffer amplifiers isolate the QAF from the four parallel vector modulators (VMs) with large input capacitance. The entire receiver integrates 32 phase and gain control paths to render a fully connected multibeam forming. However, it is challenging to realize high-performance phase shifting and amplitude tuning with tight chip area and power consumption constraints. To address the issue, we propose a compact VGPS technique, as shown in Fig. 3.

1) Current-Compensated Vector-Modulation Scheme: Fig. 3(a) shows the schematic of the VM. Two 6-bit gm arrays $G_{1,2}$ (1-bit polarity control $P_{I/Q}$ and 5-bit binary-weighted gain control $\rm EN_{I/Q}\langle 4{:}0\rangle$) adjust the weights of I/Q paths. The normalized total transconductance of each gm array ranges from -31 to 31 with a step of 1. During operation, the combined output ac current of the two gm arrays rotates around a unit circle to achieve a gain-independent phase shifting capability. Under the situation, the combined output dc current would vary with phase shifting, inducing transconductance and parasitic variation of the following common-gate (CG) transistors ($M_{1,2}$). Maintaining a constant dc bias benefits the VM performance; hence, a 4-bit current-compensation programmable array (G_3) is employed. The normalized combined dc current is fixed to 44, compared with a varying value of 31–44 without G_3. Simulation indicates that with the default control codes, the root mean square (rms) gain error of a 6-bit phase shifting can be reduced from 0.55 to 0.34 dB at 29.5 GHz by using the proposed current-compensation scheme.

2) Stacked Gain Weighting Scheme: In phased array applications, sidelobe suppression, interchannel calibration, and gain compensation at different environment conditions demand variable-gain amplifiers (VGAs) with a high DR and resolution. At millimeter-wave frequencies, conventional digital-programmable active gain-control schemes are inherently linear in magnitude [6]. However, when a linear-in-dB gain is required, the attenuation step increases as the gain decreases. To achieve a 25-dB DR and 0.5-dB step, the calculated number of bit (NoB) would reach nine for a conventional single-stage binary-weighted gm array when the maximum gain error is within ± 0.25 dB. Practically, device mismatches would limit the achievable NoB, since the transistor sizes of the millimeter-wave gm array are normally small. To address the issue, the proposed VGA utilizes a stacked gain weighting scheme with two-stage CS and CG gm arrays ($G_{4/5}$), as shown in Fig. 3(b). The normalized ac output current of the 5-bit array G_5 ranges from 1 to 63 with a resolution of two, rendering a fine gain adjustment. The 2-bit array G_4 utilizes a nonradix-2 weighting scheme to realize a coarse gain adjustment with redundancy. The cancellation-based gm unit maintains state-independent input and output impedances, minimizing the phase variation at different gain settings. By using the stacked gain weighting scheme, the VGA attains a rms gain error of 0.21 dB with a 25-dB DR and a 0.5-dB step at 29.5 GHz in simulation.

D. Active Combiner

Traditional power-combining schemes demand dedicated matching networks with bulky passive components. However, the front-end dimension of the integrated phased arrays is strictly constrained to facilitate signal routing on the printed circuit board (PCB). To render a compact multibeam forming network, the receiver utilizes an active combining scheme. Fig. 4 shows the physical implement of the 32-to-4 tree-based crossbar connection network. Differential grounded coplanar waveguide (GCPW) and perpendicular intersection routing scheme can effectively minimize the cross coupling between routing paths. For each beam, eight phase- and gain-weighted signals are directly combined in the network and fed to the following current-sharing CG amplifier. Hence, the proposed active combining scheme also benefits the power consumption.

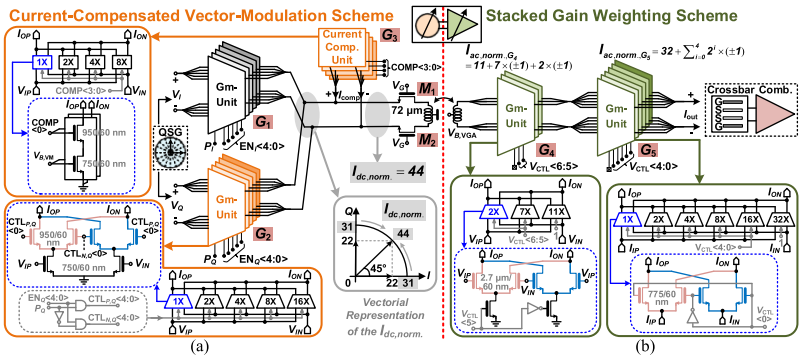

Fig. 3. Implementation of the proposed VGPS. (a) Current-compensated VM. (b) Two-stage VGA.

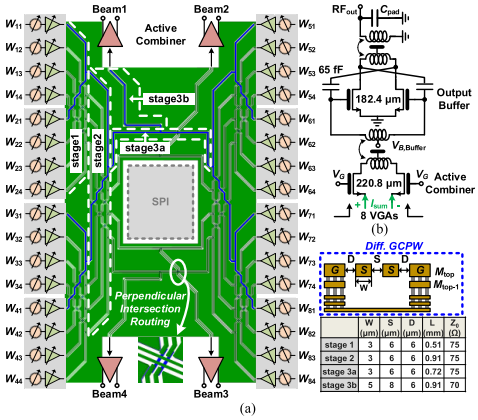

Fig. 4. (a) Physical implementation of the 32-to-4 tree-based crossbar connection network. (b) Schematic of the active combiner and output buffer.

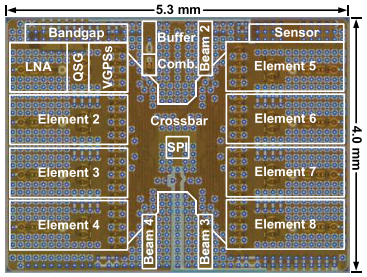

Fig. 5. Micrograph of the eight-element four-beam receiver in 65-nm CMOS.

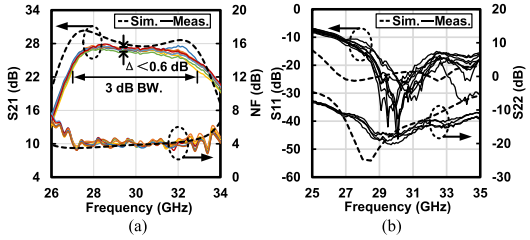

Fig. 6. Measured and simulated (a) S_{21} and NF from eight inputs to the BM2 and (b) S_{11} and S_{22} of all RF ports.

III. Measurement Results

Fig. 5 shows the micrograph of the proposed *Ka*-band compact eight-element four-beam receiver, which is fabricated in 65-nm CMOS and occupies 5.3 × 4.0 mm^2 area. The entire chip draws 1014 mA from a 1.1-V power supply.

As shown in Fig. 6(a), the gain from eight inputs to the BM_2 is 26.7 ± 0.3 dB at 29.5 GHz, where the 3-dB bandwidth is 27–33 GHz. To measure the single-element NF,

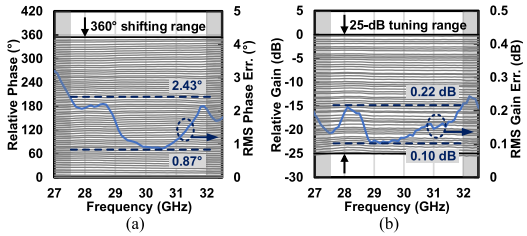

Fig. 7. Measured (a) relative phase response and rms phase error and (b) relative gain response and rms gain error.

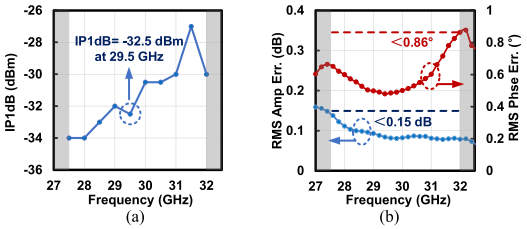

Fig. 8. Measured (a) $IP_{1\ dB}$ and (b) rms amplitude and phase errors of the BM_2 when sweeping the phase states of the BM_1.

TABLE I

Performance Summary and Comparison

Reference	This Work	[3]	[6]	[7]	[8]
Technology	65-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS
Architecture	RX	RX	TRX	RX	RX
Frequency (GHz)	27.5–32	27–31	24–28	17.7–20.2	17.7–19.2
Gain (dB)	26.7	3	27.2	20.3[a]	28
NF (dB)	3.7–4.5	10.8–11.7	4.5[b]	1.7–2.1[a]	3.2–4.1
IP_{1dB} (dBm)	−32.5	−22	−16.1	−42	−27.4
Phase Range/ Resolution (°)	360/5.625	360/5.625	360/0.8	360/5.625	360/2.8125
RMS Phase Error (°)	0.87–2.43	<4	<0.33	<1.6	<1.5
Gain Range/ Step (dB)	25/0.5	17/0.53	24/0.75	31.5/0.5	16.7/0.265
RMS Gain Error (dB)	0.10–0.22	<0.35	<0.4	<0.2	<0.22
$N_E \times N_B$	8 × 4	4 × 2	4 × 1	8 × 1	8 × 2
Power (mW)	1115.8	40	180	241.6	595.2
Power/($N_E \times N_B$) (mW)	34.9	5	45	30.2	37.2
Area (mm^2)	5.3 × 4	2.6 × 4	3.4 × 1.1[c]	9.5 × 6	4.65 × 2.77
Area/($N_E \times N_B$) (mm^2)	0.663	1.3	0.935	7.125	0.805

[a] With a 0.1-μm GaAs LNA. [b] The minimum NF. [c] Including TX area and excluding pads area.

other seven elements except for the measured one are powered off. Eight VGAs connected to the BM_2 are all powered on to

provide proper dc bias for the combiner. By using the Y-factor method, the chip demonstrates an NF of 3.7–4.5 dB from 27.5 to 32 GHz. S_{11} and S_{22} of all RF ports are below −11 dB from 27 to 32 GHz, as shown in Fig. 6(b).

From 27.5 to 32 GHz, a monotonic 360° phase shifting range with a resolution of 5.625° is achieved. Fig. 7(a) shows that the rms phase error at 29.5 GHz is 1.1°. The VGA can provide a 25-dB attenuation range with a step of 0.5 dB. Fig. 7(b) shows that the rms gain error is 0.11 dB at 29.5 GHz. The receiver exhibits an $IP_{1\ dB}$ of −32.5 dBm at 29.5 GHz, as shown in Fig. 8(a). Interbeam coupling is measured between the adjacent BM_1 and BM_2. The BM_2 holds a constant phase setting while sweeping the phase states of the BM_1. The rms amplitude and phase errors of the BM_2 are less than 0.15 dB and 0.86° from 27.5 to 32 GHz, respectively, as shown in Fig. 8(b).

Table I summarizes and compares the performance of the recent phased-array receivers. The proposed *Ka*-band receiver integrates the state-of-the-art number of simultaneously reconfigurable beams with a compact size among millimeter-wave silicon-based beamformers.

IV. Conclusion

This letter demonstrates a 27.5–32-GHz eight-element phased-array receiver with four simultaneously reconfigurable beams. The proposed variable-gain phase shifting technique and the active combining scheme facilitate the compact fully connected multibeam forming. This work paves the way for the deployment of silicon-based large-scale multibeam phased array systems for LEO SATCOM.

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