Compact 40% Fractional Bandwidth Doherty PA With Input Group Delay Engineering

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***Abstract*— This letter presents a wideband Doherty power amplifier (DPA) design based on the control of the relative input group delay between the carrier and peaking amplifiers. By reaching an appropriate input phase variation over the target bandwidth, frequency dispersion of load modulation is minimized and a less dispersive DPA at peak power is achieved. To validate this approach, a compact DPA with 50-dBm peak power is developed and shows 51%–57% drain efficiency at 8-dB output power back-off (OBO) with a small-signal gain of 14.4–17 dB over 1.8–2.7 GHz which represents 40% fractional bandwidth (FBW). Linearization of the prototype is proven using DPD correction with ACPR below −60 dBc measured in single-band scenarios. Moreover, under 400 MHz of instantaneous bandwidth, the proposed DPA achieves ACPR below −53 dBc with an average efficiency of 48%.**

***Index Terms*— Doherty power amplifiers (DPAs), load modulation, phase compensation, wideband amplifier.**

I. Introduction

WIRELESS telecommunications industry is currently deploying the new 5G standard to meet the high demand for data transmission rates and connection relay density [1]. Small cell coverage infrastructure uses a massive multiple input multiple output (MiMo) transmitter architecture (32T or 64T) which implies the presence of a compact power amplifier (PA) circuit (5–15 W average power) in each transmission path. In addition, as the number of frequency bands to be covered in a transmitter increases, the RF bandwidth of the amplifier becomes an important characteristic to move toward a broadband system with a single true multiband PA rather than a system with multiple narrowband PAs [2].

The Doherty PA (DPA) is the most common load-modulated amplifier technique used in the radio architectures. Several works have shown that the use of a post-matching inverted Doherty topology based on GaN transistors allows to obtain a PA with a large relative bandwidth but with an increase in the area occupancy [3], [4]. Other techniques such as distributed efficient PA (DEPA) [5] or load-modulated balanced amplifier (LMBA) [6] show very good broadband performances but their implementation remains large due to the use of multisection output combiner. In a DPA, compactness can be achieved with zero-phase offset compensating circuit for the peaking path and the use of dual RF-input topology with asymmetrical drain bias to extend the operational bandwidth [7] but tends to increase the transmitter architecture complexity.

This letter shows that the input phase difference and its deviation across the frequency band can also be used to optimize the load impedance dispersion characteristics in the full power (FP) state and thus enabling a better tradeoff between back-off and peak power bandwidth. The optimal relative group delay found analytically is then obtained by manipulating the input phase deviation of the carrier path. To validate this methodology, a compact prototype has been designed and realized. The measurement shows broadband Doherty performances over 40% of fractional bandwidth (FBW). The characterization is completed by evaluation of the linearity capability using digital predistortion (DPD) for multiband test case scenarios.

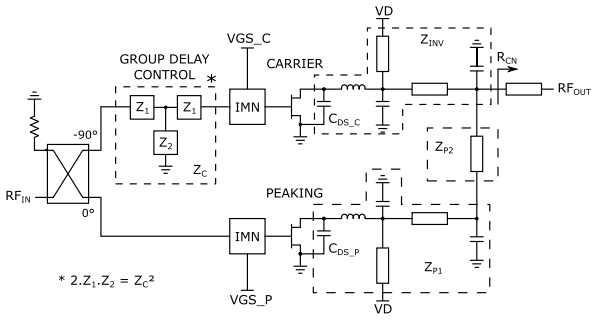

Fig. 1. Simplified schematic of the proposed DPA.

II. Wideband DPA Design

A. Doherty Amplifier Configuration

A simplified schematic of the proposed DPA is shown in Fig. 1. To improve the bandwidth, an inverted topology is used with 90°/180° Doherty combiner. DPA is based on the carrier and peaking amplifiers, using GaN HEMT transistors with r the peaking/carrier gate periphery ratio.

The quarter-wave length section of the carrier and the first quarter-wave length section of the peaking are designed in a quasi-transmission line (TL) network which absorbs the nonlinear parasitic output capacitance of each transistor. The equivalent reactance at the common node between the inductive drain bias stub and the parallel capacitance is chosen to present, in series with bond wires, a low capacitive impedance in current source reference plane at the second harmonic, to maintain the amplifier's class of operation in a BJ design space [8].

Manuscript received 23 February 2023; revised 5 April 2023; accepted 5 April 2023. *(Corresponding author: Manuel Cavarroc.)*

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This article was presented at the IEEE MTT-S International Microwave Symposium (IMS 2023), San Diego, CA, USA, June 11–16, 2023.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWT.2023.3266095.

Digital Object Identifier 10.1109/LMWT.2023.3266095

Carrier's quasi-TL network is set to an impedance $Z_{\text{inv}} = ((r+1)\cdot R_{\text{CN}}\cdot R_{\text{OPT},C})^{1/2}$ [9] to perform the impedance inversion, with $R_{\text{OPT},C}$ and R_{CN}, respectively, the optimum impedance presented to drain current source of the carrier amplifier at high level and the resistance at the output combining node. For the peaking amplifier, the two-section matching network Z_{P1} and Z_{P2} follows a binomial distribution law [10] to improve the bandwidth. At the output of the Doherty combiner, a simple quarter-wave TL is used to perform the final transformation between R_{CN} and 50 Ω.

To increase the low input impedance, silicon-based integrated passive devices (IPDs) are designed for wideband input matching networks (IMNs) using integrated capacitors while inductors are realized with bonding wires.

To complete the design, a commercial quadrature hybrid coupler is selected for its compactness and used for even input power splitting and phase delay. A constant 90° phase shift, between the carrier and peaking path over the frequency band, results in the loss of phase coherency between the output and the input, and thus a decrease in the peak power bandwidth. To extend the broadband capabilities on this Doherty amplifier configuration, a passive network is introduced to control the group delay on the carrier input path.

B. Broadband Load Modulation Optimization

To demonstrate the interest of the proposed group delay control, the combiner at the output is simplified to its $\lambda/4$ TL representation. The complex I_P/I_C current ratio changes with frequency and modifies the frequency behavior of the amplifier. At low power state (BO), the peaking amplifier is off ($I_P = 0$), so the impedance seen by the carrier current source is a function of the combining node impedance R_{CN}. During load modulation, the peaking current source reaches its nominal value $I_P = r\cdot I_C\cdot e^{-j\Delta\Phi}$ so the bandwidth is also dependent of the input phase difference $\Delta\Phi$. Considering a linear phase variation around f_C, $\Delta\Phi$ could be expressed as

$$\Delta\Phi(\omega) = -\frac{\pi}{2} - \Delta\tau_{\text{gd}}\cdot(\omega-\omega_c) \tag{1}$$

where $\Delta\tau_{\text{gd}}$ is the relative group delay between the carrier and peaking input paths. To evaluate the benefits of adjusting the group delay, the voltage standing wave ratio presented by the output network in the plane of current sources for the carrier and peaking amplifiers is calculated as

$$\text{VSWR} = \frac{1+\left|\Gamma\left(R_{\text{CN}}, |I_P/I_C|\cdot e^{-j\Delta\Phi}\right)\right|}{1-\left|\Gamma\left(R_{\text{CN}}, |I_P/I_C|\cdot e^{-j\Delta\Phi}\right)\right|}. \tag{2}$$

The VSWR at FP of the carrier and peaking amplifiers is modified by the group delay. We consider $\Delta\tau_{\text{gd}} = 0$, corresponding to a hybrid coupler constant 90° phase difference case, or $\Delta\tau_{\text{gd}} = 1/(\alpha.2f_C)$, with α adjusted to improve the VSWR for the band edge frequencies ($0.8f_C$ or $1.2f_C$ for 40% FBW).

To illustrate the performances, a 100-W Doherty is considered with a peaking/carrier gate periphery ratio $r = 1.5$ to maintain efficiency at back-off, on 8 dB theoretically. From DCIV analysis, with a nominal drain bias $V_{\text{D}} = 48$ V, the optimal load line is $R_{\text{OPT},C} = 18$ Ω for the carrier amplifier and $R_{\text{OPT},P} = 12$ Ω for the peaking amplifier.

Fig. 2 shows the VSWR results for different values of the combining node impedance, purely real, R_{CN} with $\Delta\tau_{\text{gd}} = 0$ and $\alpha = 1.13$. By adopting an over-compensation strategy ($\alpha = 1.13$) on the input relative group delay between the carrier and peaking paths, it is possible to reduce the output frequency load dispersion difference at FP to an optimum point, which equals the frequency dispersion at low power. In this example, a VSWR = 1.16 at $R_{\text{CN}} = 28$ Ω is achieved on 40% FBW, allowing wideband behavior for a conventional and size-reduced output matching network.

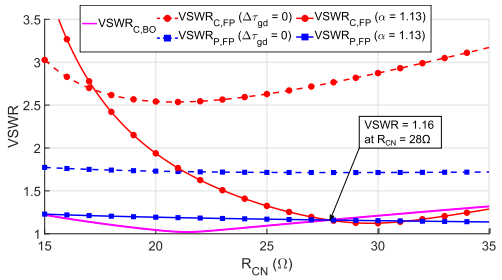

Fig. 2. Comparison between calculated VSWR with and without relative group delay engineering at band edge frequencies.

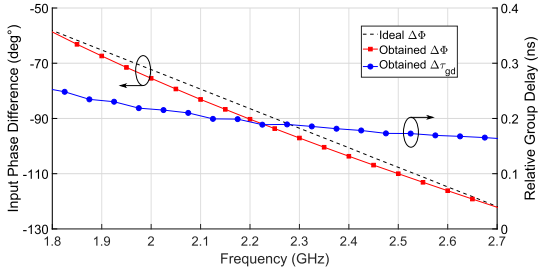

Fig. 3. Ideal and obtained phase difference resulting in relative group delay.

C. Input Group Delay Engineering

From the analytical study, around the 90° phase shift at $f_C = 2.25$ GHz, the ideal and linear input phase difference follows a deviation from −58° at 1.8 GHz to −122° at 2.7 GHz which results in a relative group delay $\Delta\tau_{\text{gd}} = 0.2$ ns.

The input phase of the carrier amplifier is shaped to track this specific deviation from the constant 90° phase shift difference provided by the quadrature hybrid coupler. Based on the bandpass filter synthesis theory, a network with flat group delay response and a sufficient order of $n = 3$ is selected to minimize the transmission and return loss.

Fig. 3 shows the phase difference and relative group delay which result in input carrier path shaping. The obtained relative group delay deviates from 0.25 to 0.16 ns at the band edges. Thus, it results in a closely linear phase deviation which matches the required values at 1.8 and 2.7 GHz.

III. Fabrication and Experimental Results

The proposed Doherty amplifier was fabricated on a multilayer and low insertion loss RF substrate ($d_k = 3.35$) with 1-mm total thickness. The circuit takes the form of a multi-chip module assembly with 50 Ω input–output in a 20 × 16 mm LGA type of package as shown in Fig. 4. GaN dice and IPDs were attached to a copper coin inserted through the substrate for thermal management. The dice are bonded directly onto the circuit RF traces and protected by glob-top. To perform measurements, the module is soldered to an evaluation circuit board (EVB) with RF and dc access through a reflow process. Considering RF bypass capacitors' location on EVB, the total area taken by the Doherty amplifier circuit is 30 × 30 mm.

A. Small- and Large-Signal Measurement

The carrier gate bias voltage is set to −2.5 V and the peaking gate bias voltage is set to −5.4 V. Also, the carrier

TABLE I
RF PERFORMANCES' COMPARISON WITH RECENTLY PUBLISHED WIDEBAND LOAD-MODULATED PAS

Year / Ref.	Architecture	Size (mm x mm)	Freq. (GHz)	P_{max} (dBm)	Gain (dB)	OBO (dB)	DE@OBO (%)
2018 [7]	Dual RF-input Doherty	51 x 51	1.8 - 2.7	53.5	12 - 14*	7.5	45 - 53*
2019 [5]	DEPA	140 x 120	2.55 - 3.8	48.8 - 49.8	9.3 - 12.7	8	47 - 60
2021 [11]	asym. Doherty	170 x 100	1.4 - 2.5	44 - 45.9	12.1 - 16.3	9	44.6 - 54.6
2022 [6]	S-LMBA	328 x 155	1.8 - 2.75	44.6 - 45.8	9.4 - 11.7	8	51.8 - 69
TW	inverted Doherty	30 x 30	1.8 - 2.7	49.8 - 50.7	14.4 - 17	8	51 - 57

* Graphically estimated

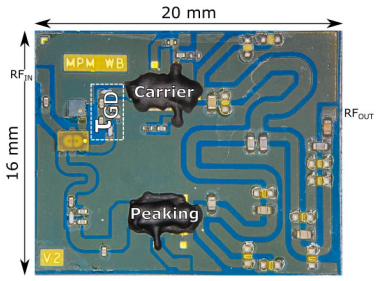

Fig. 4. Photograph of the multi-chip module DPA.

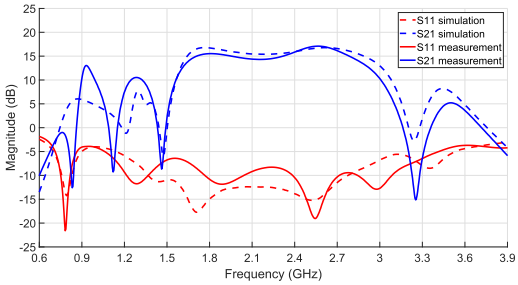

Fig. 5. Measured and simulated S-parameters' comparison.

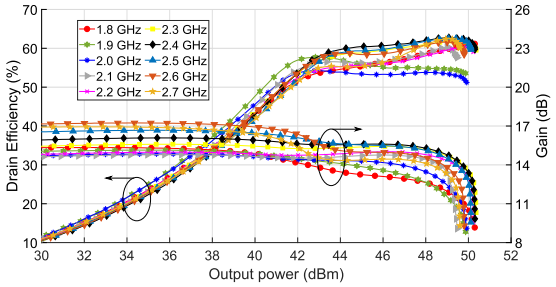

Fig. 6. Measured drain efficiency and gain performances under CW stimulus.

and peaking amplifiers share the same drain bias voltage $V_D = 48$ V.

Fig. 5 shows a comparison between the measured and simulated S-parameters with a good location match of the peaking OFF-state zeroes in transmission response and a small-signal gain of 14.4–17 dB within the targeted RF bandwidth.

Fig. 6 depicts the measured efficiency and gain versus output power under continuous wave (CW) stimulus. It can be seen that the dynamic behavior of the fabricated DPA is well maintained over 1.8–2.7 GHz with a relatively good AM/AM linearity. Drain efficiency of 51%–57% is achieved at 8-dB output power back-off (OBO) throughout the entire operation band.

Fig. 7 shows RF performances measured with a single-carrier LTE 20-MHz unclipped test signal. Using a CCDF at 0.01% probability, the measured output peak power ($P_{3\ dB}$) is close to 50 dBm with excellent flatness (±0.5 dB) across

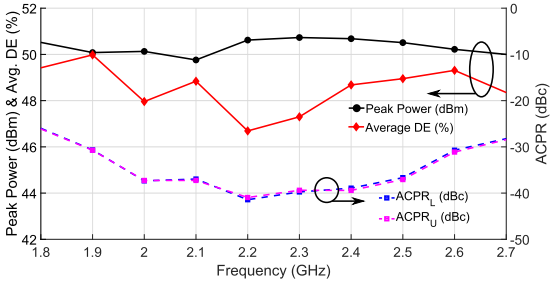

Fig. 7. Measured peak power, average drain efficiency, and ACPR performance at 8-dB OBO using a single-carrier LTE 20-MHz unclipped test signal.

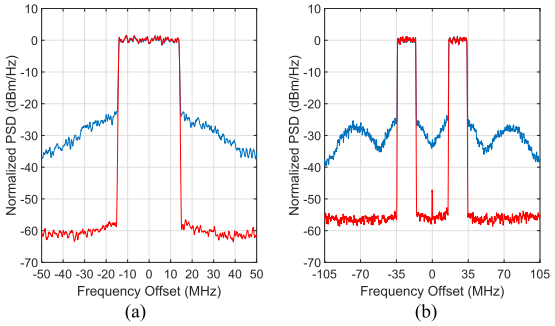

Fig. 8. Output spectrum before (blue) and after (red) DPD correction of fabricated DPA with (a) 1C-LTE 20-MHz and (b) 2C-LTE 20-MHz (70-MHz SBW) test signals at 2655-MHz center frequency.

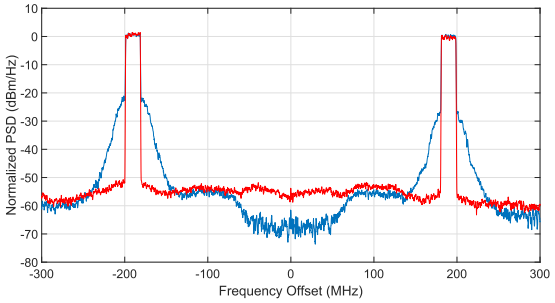

Fig. 9. Output spectrum before (blue) and after (red) DPD correction of fabricated DPA with a 2C-LTE 20-MHz (400-MHz SBW) test signal at 2002.5-MHz center frequency.

the whole bandwidth. The measured average drain efficiency, at 8-dB OBO from minimum peak power ($P_{avg} = 41.8$ dBm), is greater than 46.6%. Uncorrected lower and upper ACPRs evolve from −41 dBc around the center frequency to −26 dBc at the band edges. The measured performances are compared, in Table I, with recent wideband load-modulated PAs.

B. Linearization and Multiband Test Cases

To demonstrate the linearizability of the fabricated DPA, DPD is performed first under single-band scenarios to cover B7 band. The measured output spectra at 41.8-dBm average output power, with and without DPD, are shown in Fig. 8.

Using a single-engine DPD based on the generalized memory polynomial (GMP) model with 107 coefficients, the fabricated DPA is linearized with ACPR level below −60 and −56 dBc for 1C-LTE 20-MHz 7.5-dB PAR and 2C-LTE 20-MHz (70-MHz SBW) 7.5-dB PAR, respectively.

For multiband test case scenarios, the generated signal consists of two noncontiguous LTE 20-MHz 7.5-dB PAR carriers with 400-MHz SBW to cover B3–B66 bands. Using a dual band with indirect learning DPD, ACPR is reduced below −53 dBc, as shown in Fig. 9, with an average efficiency measured at 48%.

IV. Conclusion

In this letter, the control of the input group delay at the input carrier path has been proposed to enhance the broadband capabilities. Through a preliminary study, the necessary input phase deviation is calculated to serve as a starting point for the wideband DPA design. As proof-of-concept, a compact form factor DPA is fabricated which demonstrates 50-dBm peak power across 40% of FBW (1.8–2.7 GHz) with an average drain efficiency greater than 46.6% at 8-dB OBO and a small-signal gain greater than 14.4 dB. With DPD correction, ACPR is reduced below −60 dBc which demonstrates the linearization of the prototype in a single-band case. In case of large-signal bandwidth, the amplifier achieves 48% average efficiency and ACPR below −53 dBc during 2C-LTE 20-MHz with 400-MHz SBW in B3–B66 concurrent transmission bands. These results prove the reliability of the methodology to design broadband DPA for mMiMo transmitter applications and multiband operations.

References

[1] S.-Y. Lien, S.-L. Shieh, Y. Huang, B. Su, Y.-L. Hsu, and H.-Y. Wei, "5G new radio: Waveform, frame structure, multiple access, and initial access," *IEEE Commun. Mag.*, vol. 55, no. 6, pp. 64–71, Jun. 2017.

[2] S. Bassam, W. Chen, M. Helaoui, and F. Ghannouchi, "Transmitter architecture for CA: Carrier aggregation in LTE-advanced systems," *IEEE Microw. Mag.*, vol. 14, no. 5, pp. 78–86, Jul. 2013.

[3] J. Wong, N. Watanabe, and A. Grebennikov, "High-power high-efficiency broadband GaN HEMT Doherty amplifiers for base station applications," in *Proc. IEEE Topical Conf. RF/Microw. Power Model. Radio Wireless Appl. (PAWR)*, Jan. 2018, pp. 16–19.

[4] J. Pang, S. He, C. Huang, Z. Dai, J. Peng, and F. You, "A post-matching Doherty power amplifier employing low-order impedance inverters for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4061–4071, Dec. 2015.

[5] P. Saad, R. Hou, R. Hellberg, and B. Berglund, "An 80W power amplifier with 50% efficiency at 8dB power back-off over 2.6–3.8 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1328–1330.

[6] C. Chu et al., "Waveform engineered sequential load modulated balanced amplifier with continuous class-F-1 and class-J operation," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 2, pp. 1269–1283, Feb. 2022.

[7] H. Jang and R. Wilson, "A 225 Watt, 1.8–2.7 GHz broadband Doherty power amplifier with zero-phase shift peaking amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 797–800.

[8] S. Boutayeb, A. Giry, A. Serhan, J.-D. Arnould, and E. Lauga-Larroze, "Output matching network design for broadband class B/J power amplifier," in *Proc. 13th Conf. Ph.D. Res. Microelectron. Electron. (PRIME)*, Jun. 2017, pp. 41–44.

[9] R. McLaren and H. J. de la Rosa, "Doherty architecture for wideband power amplifier design," U.S Patent 996 690 3B1, May 8, 2018.

[10] Z. Ahmed, "Revisiting the binomial multisection transformer [application notes]," *IEEE Microw. Mag.*, vol. 22, no. 2, pp. 58–65, Feb. 2021.

[11] Y. Xu, J. Pang, X. Wang, and A. Zhu, "Enhancing bandwidth and back-off range of Doherty power amplifier with modified load modulation network," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2291–2303, Apr. 2021.