2.6- and 4-W *E*-Band GaN Power Amplifiers With a Peak Efficiency of 22% and 15.3%

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***Abstract*— In this letter, we report two high-power gallium nitride (GaN) power amplifiers (PAs) in the Satcom *E*-band (71–86 GHz) with an output power of 2.6 and 4 W, designed by incorporating an ultralow-loss ON-chip integrated power combiner. The first one is a three-stage four-way combining (unit) PA, and the second one is an eight-way combining balanced PA. The unit PA produces a saturated output power (P_{SAT}) of 34.2 dBm (2.6 W), a peak power-added-efficiency (PAE) of 22%, and an associated power gain of 16.2 dB at 74 GHz. This performance was partly made possible by the design and optimization of the low-loss integrated power combiner, which minimized the losses in the matching networks. In addition, the balanced PA produces a P_{SAT} of 36 dBm (4 W), $P_{1\,dB}$ of 35.6 dBm (3.63 W), with an associated PAE of 15.3% at 80 GHz. To the best of the authors' knowledge, this is the highest output power (4 W) and the highest PAE (22%) for a PA > 2.5 W reported in any of the III–V technologies at *E*-band.**

***Index Terms*— *E*-band, gallium nitride (GaN), high efficiency, high frequency, high output power, low-loss, mm-wave, monolithic microwave integrated circuit (MMIC), ON-chip, power amplifier (PA), power combining, *W*-band.**

I. Introduction

THE recent rollout of fifth-generation (5G) mobile communications has led to a massive increase in data traffic of mobile backhaul networks. Traditional microwave bands (6–42 GHz) are already congested and do not have sufficient bandwidth to handle the growing volume of data transmissions. To overcome this, the *E*-band (71–76 and 81–86 GHz) allows wide bandwidth channels and multiGbps capacity, enabling 5G new radio (NR) capacities in microwave backhaul [1]. Despite the high-data rates, the long-haul radio links are hindered by semiconductor technologies with limited output power generation capability. Advances in compound semiconductor technologies, particularly gallium nitride (GaN) high-electron-mobility transistors (HEMTs) made it possible to design highly efficient watt-level power amplifiers (PAs) at *E*-band. These higher-efficiency amplifiers will further reduce the system footprint and operating costs.

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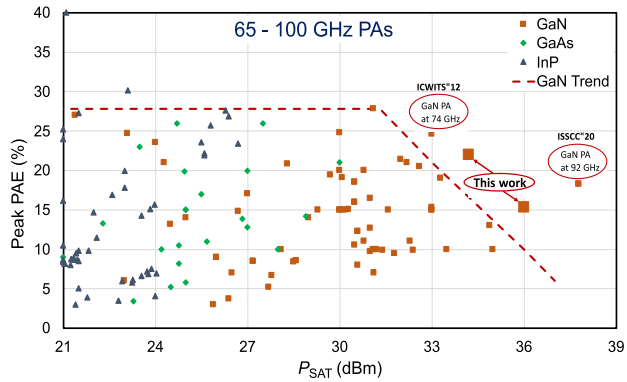

Fig. 1. PA survey in III–V technologies.

Recently, a 10-km hop with a data rate of 10 Gb/s has been demonstrated [2] using a GaN PA [3]. To achieve this, two PAs are combined to generate 4 W of output power at the PA module. Fig. 1 shows the survey of all the high-power PAs between 65 and 100 GHz using III–V technologies [4]. It can be seen that there are a limited number of PAs that demonstrate watt-level output power with an efficiency of more than 20%. Moreover, there are no PAs that deliver an ON-chip output power of 4 W at the *E*-band. This work demonstrates a three-stage four-way combining (unit) PA of 2.6 W output power with a peak efficiency of 22% and utilizes this unit PA to further design an eight-way combining balanced PA that produces 4 W of output power.

This letter is organized as follows. first, we discuss the characteristics of the GaN technology used in this design, followed by the monolithic microwave integrated circuit (MMIC) design of a three-stage four-way combing (unit) *E*-band PA, including the design and evaluation of a low-loss power combiner. Finally, the measurement results of the unit PA and balanced PA are reported and compared with the state-of-the-art GaN PAs.

II. GaN Technology

An advanced AlGaN/GaN HEMT technology with a gate length of 100 nm (GaN10–20) from Fraunhofer IAF [5] was used to design this MMIC. The epitaxial layers of this technology are grown on 4-in silicon carbide (SiC) substrates. For the realization of the high-frequency MMICs, the technology offers passive circuit elements such as thin-film NiCr resistors, metal-insulator-metal (MIM) capacitors, via holes, coplanar waveguide (CPW), and microstrip transmission lines

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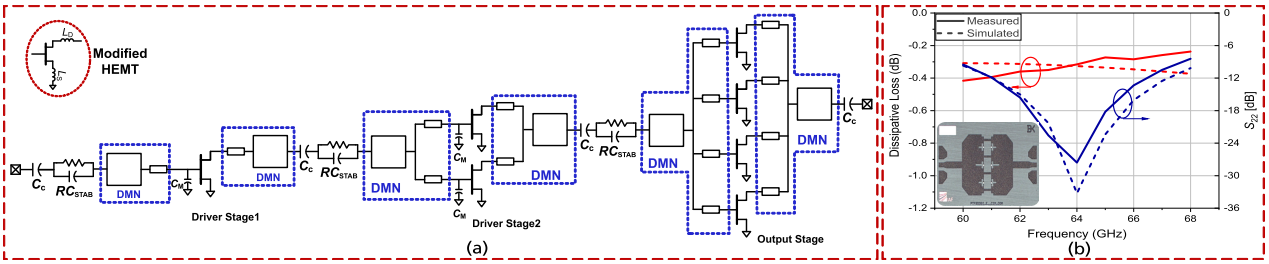

Fig. 2. (a) Simplified schematics of the unit E-band PA with DMN. (b) Measured (solid) and simulated (dashed) results of the combiner test structure.

(MSLs) in a process design kit (PDK) library. Scalable small-signal and large-signal HEMT models are also available in the PDK. The small-signal RF characterization of a 4 × 45 μm HEMT reveals a peak current-gain cut-off frequency (f_{T}) of about 90 GHz at 15 V, along with an extrapolated maximum oscillation frequency (f_{MAX}) of around 300 GHz.

III. MMIC Design

A simplified schematic of a three-stage four-way combining (unit) E-band PA is shown in Fig. 2(a), along with the distributed matching network (DMN) and the modified HEMT model. Based on the load–pull simulations, to achieve a targeted output power of 2 W, the outputs of four transistors with a gate width of $W_{\mathrm{g}} = 6 \times 45$ μm are combined at the last stage. Two driver stages with a driving ratio of 1:2.25 are utilized to provide sufficient gain to drive the output stage into saturation. Each stage is prematched to 50 Ω using a DMN to optimize the losses in the matching network carefully. In addition to that, the low-frequency RC_{STAB} circuit at the gate was added at the high impedance (50 Ω) side of the matching network to further minimize the loss.

To avoid losses in the traditional corporate combiners, this circuit employs DMNs, which integrate both matching and power combing functionalities. In its simplest form, the DMN is a cascade of a short (typically high-impedance line of an approximate length of $\lambda/8$) and a long (low-impedance line of length $\lambda/4$) transmission lines, which both transform the complex optimum impedance (obtained from load-pull simulations) at the drain/gate of the HEMT to 50 Ω. The short high-impedance line transforms the complex impedance to an intermediate real impedance, and the $\lambda/4$ line further transforms it to 50 Ω [6]. Since the impedance transform ratio is high at the gate, a preimpedance matching element (C_{M}) is used at the gate of driver stages to improve the frequency bandwidth of the matching network and have enough margin to drive the output stage. However, for the input matching network (IMN) at the output stage where four MIM capacitors would be needed, a tradeoff has been made to minimize the high-frequency parasitic losses of the MIM capacitor for bandwidth. The output DMN is further modified to minimize the dissipative loss (DL) and mismatch loss (due to an imbalance in phase and magnitude between the ports). Chamfered bends are introduced to compensate for the discontinuities, and slits are introduced to avoid the propagation of higher-order modes and increase the inductive impedance (seen from a pair of adjacent HEMTs) to dampen the odd-mode operation. The DL of the combiner is computed using the following equation:

$$\mathrm{DL}_{\mathrm{OMN}} = -10 \ \log \frac{|S_{21}|^2}{|1 - S_{22}|^2}. \tag{1}$$

The results of the electromagnetic (EM) simulations and the back-to-back test structure measurement results are plotted in Fig. 2(b). Given the minimum uncertainty in measuring the low-loss passives of the calibrated measurement setup of about ±0.1 dB [7], the measured loss of the combiner test structure is still better than 0.45 dB in the targeted band, which is in close agreement with the expected results.

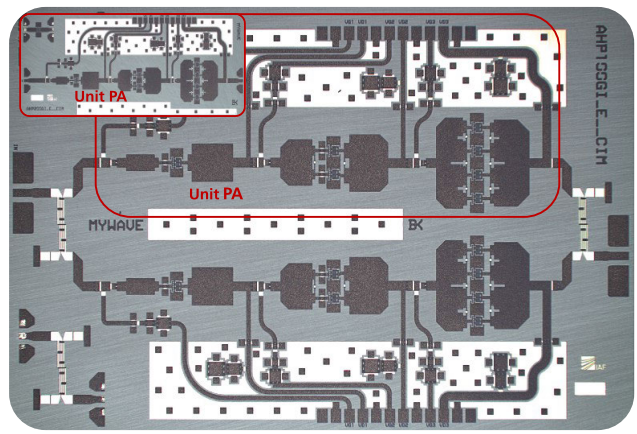

Fig. 3. Chip photograph of the balanced E-band PA (with the unit PA highlighted). Chip size = 4.75 × 3.25 mm^2 (unit PA size = 4.25 × 1.75 mm^2).

IV. Measurement Results

The chip photograph of the unit PA and the balanced PA are shown in Fig. 3, along with the chip dimensions. Firstly, to identify the best working cells, the small signal S-parameter measurements of all the cells on the wafer are performed using a HP8510-XF vector network analyzer with the circuit biased at a drain voltage of $V_D = 15$ V and a nominal quiescent current of $I_{\mathrm{DQ}} = 250$ mA/mm. The results of the unit PA are plotted in Fig. 4, along with the simulated ones. The measured small-signal gain is more than 17 dB across 71–84 GHz, with a maximum gain of 19.6 dB measured at 80 GHz and its 3-dB bandwidth is 15 GHz (69–84 GHz). A good agreement with simulated and measured results for input reflection (S_{11}) is observed. However, a notable shift in the center frequency for the gain (S_{21}) and the output reflection (S_{22}) could be observed. This difference is attributed to two reasons: 1) using a standard CPW HEMT (due to lack of MSL HEMT model at the time of the design) in MSL design and 2) underestimating the parasitics at the transition of the CPW HEMT to microstrip environment. Further analysis shows that a MIM capacitor at the gate with two ground vias would still provide a CPW-like environment, whereas the drain connection is quickly transitioned from CPW to MSL environment. The CPW-MSL transition parasitics can be described by two modifications to the standard HEMT models: 1) a series inductance at the drain and 2) a series inductance at the source (which also considers the effective via inductance as a result of via sharing). The

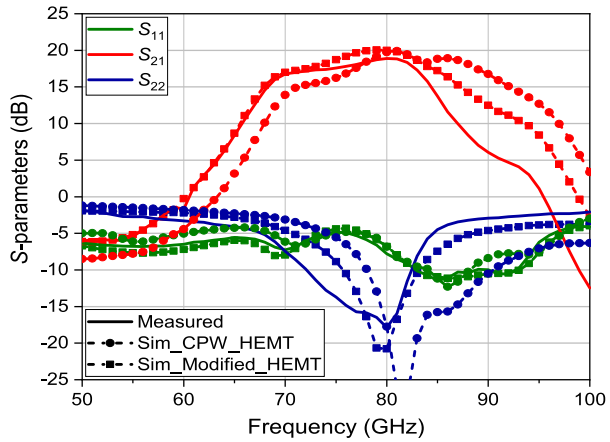

Fig. 4. Measured (solid) and simulated (dashed) S-parameters of three-stage E-band PA. $V_D = 14$ V, $I_{DQ} = 250$ mA/mm.

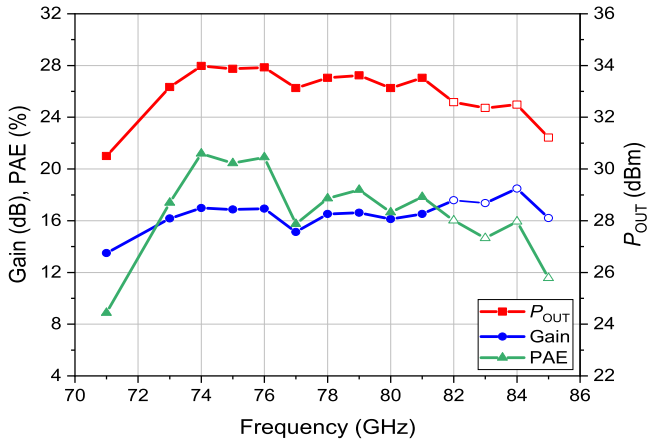

Fig. 5. Measured large signal frequency sweep of unit PA. $P_{in} = 17$ dBm (= 15 dBm beyond 81 GHz).

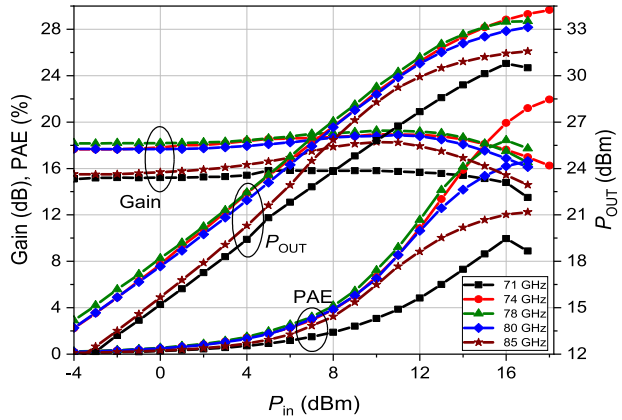

Fig. 6. Measured large signal input power sweep of a unit PA. $V_D = 15$ V, $I_{DQ} = 400$ mA/mm.

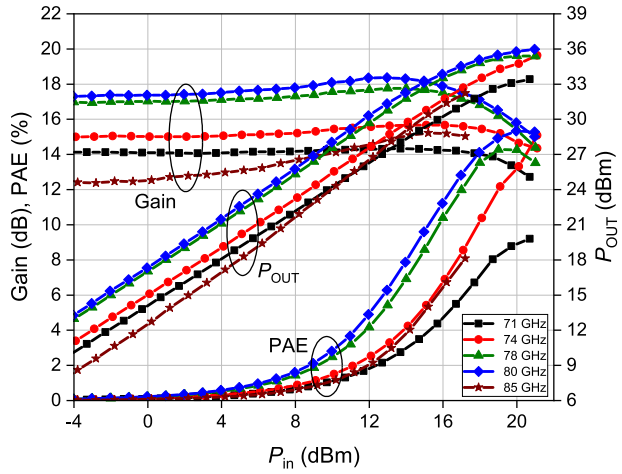

Fig. 7. Measured large signal input power sweep of a balanced PA. $V_D = 15$ V, $I_D = 450$ mA/mm.

resulting simulated results of the MMIC design with the modified HEMT have a close agreement with the measured results. Similarly, with this modified HEMT model, a close agreement for the small-signal simulation and measurement results were also obtained for the balanced PA, which has S_{11}, S_{22} better than -15 dB, and S_{21} of 14.1–17.3 dB in the targeted band.

Secondly, the on-wafer continuous wave (CW) large-signal measurements are initially performed at a nominal quiescent current of $I_{DQ} = 250$ mA/mm. After dicing the wafer, a few selected chips are glued onto a heat sink, enabling us to conduct measurements at a higher quiescent current. Fig. 5 shows the frequency sweep response across 71–85 GHz with an input power P_{in} of 17 dBm (and 15 dBm beyond 81 GHz) at the bias condition of $V_D = 15$ V, $I_{DQ} = 400$ mA/mm. The measured unit PA produces an output power of 33.6 $\pm$ 0.4 dBm in 73–81 GHz, with an associated power gain of more than 15.8 dB and power-added-efficiency (PAE) greater than 15%. The results for the input power sweep at various frequencies between 71 and 85 GHz are also shown in Fig. 6. A peak output power of 34.2 dBm (2.6 W) is measured at 74 GHz, with an associated PAE of 22% and a power gain of 16.2 dB. The resulting power density of this PA is 2.45 W/mm. While the PA is stable at the desired bias condition, we encountered a low-frequency stability issue at 3 GHz, when biased at a reduced supply voltage of 10 V. This could be fixed with an OFF-chip component. Furthermore, the large-signal performance of the balanced PA is plotted in Fig. 7 with input power sweep at various frequencies between 71 and 85 GHz. The peak output power of 36 dBm (4 W) is measured at 80 GHz, with an associated PAE of 15.3%, power gain of 15 dB, and $P_{1\,dB}$ of 35.6 dBm (3.63 W). The peak power density of balanced PA is 1.85 W/mm. Across the 74–81 GHz, the PA achieves an output power of more than 35 dBm (3.2 W) with available input drive power as a major limitation to push this amplifier into saturation, especially beyond 81 GHz.

V. State-of-the-Art E-Band PAs Beyond 1 W

The current state-of-the-art of E-band GaN PAs beyond 1 W of output power (CW measurements only) are listed in Table I. The results presented in this letter (for unit PA) outperform all the previously reported PAs (with P_{SAT} beyond 2.5 W) in terms of PAE. We also present the first 4 W PA in E-band (at 80 GHz) with a PAE of 15.3%. While the unit PA records peak P_{SAT} at 74 GHz, the balanced PA is not driven completely into saturation at this frequency due to limitation in the available input power. The PA presented in [9] produces an output power of 3.1 W with the highest power density of 3.23 W/mm, when biased with 20 V. The highest efficiency for a watt-level PA of 27% is reported by Brown et al. [9] using an advance 40-nm T3 HEMT technology from HRL. Overall, this work demonstrates the feasibility of designing wideband, highly efficient watt-level PAs for E-band communication systems.

TABLE I
COMPARISON OF STATE-OF-THE-ART GaN PAs (P_{OUT} >1 W) AT E-BAND

Ref.	Freq (GHz)	Gain (dB)	Max. PAE (%)	P_{SAT} (W)	GaN (Technology)
[8]	67 – 80	6	7	1.3 (CW)	Fujitsu 120nm
[9]	71 – 76	9.5	14.2	3.1 (CW)	Raytheon 150nm
[9]	81 – 86	11.6	15.3	2.0 (CW)	Raytheon 150nm
[10]	80 – 100	8	10	2.0 (CW)	HRL 140nm
[11]	79 – 95	17	27	1.3 (CW)	HRL 40nm
[12]	75 – 100	9	12	3.0 (CW)	HRL 140nm
[13]	78 – 89	12	12.3	1.15 (CW)	Fujitsu 80nm
[5]	71 – 86	18	9.5	1.5 (CW)	IAF 100nm
[3]	81 – 86	17	10	2.2 (CW)	IAF 100nm
[14]	71 – 83	16.3	20.8	1.35 (CW)	IAF 100nm
This work	**71 – 85**	**16.2** **15**	**22** **15.3**	**2.6 (CW)** **4.0 (CW)**	**IAF 100nm**

VI. CONCLUSION

This work presents two high-power E-band MMIC PAs with a saturated output power of 2.6 and 4 W with a peak PAE of 22% and 15.3%, respectively. This performance was partly enabled by the design and optimization of the low-loss integrated power combiner, which minimizes the losses in the matching networks. These results demonstrate the feasibility of implementing highly efficient, long-hop, high data rate E-band radios.

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