GaN SLCFET Technology for Next Generation mmW Systems, Demonstrating P_{out} of 10.87 W/mm With 43% PAE at 94 GHz

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***Abstract*— We report on the development of the super-lattice castellated field effect transistor (SLCFET) technology as a candidate for the next generation of mmW and *W*-band systems, leveraging the high carrier density and a high degree of charge control offered by this device topology for mmW and *W*-band power amplification. The SLCFET is built using a superlattice of stacked AlGaN/gallium nitride (GaN) heterostructures that are etched into nanoribbons between epitaxial regrown n+ GaN source and drain contacts and controlled with a 100 nm length T-gate that electrostatically actuates the stacked channels from the sidewalls. The 2 × 20 μm amplifier cells of SLCFET devices were measured using load–pull at 94 GHz using a 12-V bias, demonstrating amplifier output power densities of 10.87 W/mm with 43% power added efficiency (PAE) at peak power and a maximum linear gain of 5.4 dB. The SLCFET amplifier process attains this power density due to its extremely high current density, with a maximum current (IMAX) of 4.8 A/mm, along with its minimal dispersion, with current collapse measured using pulsed *I–V* at <7%. The SLCFET technology, with its previously demonstrated world-class radio frequency (RF) switch performance and now record *W*-band amplifier performance, is ideal for use in next-generation mmW and *W*-band systems.**

***Index Terms*— Gallium nitride (GaN), millimeter wave devices, monolithic microwave integrated circuit (MMIC), power amplifiers, superlattice, *W*-band.**

I. Introduction

NEXT-GENERATION communication systems demand ever greater data rates with larger bandwidth, while next-generation radio frequency (RF) sensing applications have a similar desire for greater resolution over longer distances. These factors combined with the desire to operate in less congested portions of the electromagnetic spectrum have created a significant demand for high power densities at higher power efficiencies to enable mmW and *W*-band communication and sensing applications on smaller platforms. The advantages of gallium nitride (GaN)-based transistors for achieving higher powers with greater efficiency and in a smaller footprint at *W*-band were demonstrated nearly two decades ago [1], and significant improvements in the performance of GaN-based amplifier technologies through gate scaling and material improvements such as incorporating Sc into the GaN heterostructure have been developed since then to further improve upon mmW and *W*-band power performance [2], [3], [4]. Some of the most significant reported improvements have changed from the use of typical Ga-polar GaN epitaxial structures to instead using an N-polar GaN epitaxy and device structure. Recent advances with N-polar GaN devices have redefined the upper limits of power densities achievable at mmW frequencies and *W*-band, reaching 8.84 W/mm at *W*-band with an associated power added efficiency (PAE) of 27% [5], more than twice the power densities reported for Ga-polar technologies. The N-polar approach achieves this by creating the transistor's electron channel farther from troublesome surfaces and interface states, while also enabling the growth of those interfaces in an in situ process along with the rest of the device epitaxy, using a GaN cap to passivate the device and reduce surface depletion. This has the effect of reducing current collapse, while also increasing the active region conductivity to improve overall power amplification performance at mmW and *W*-band [6].

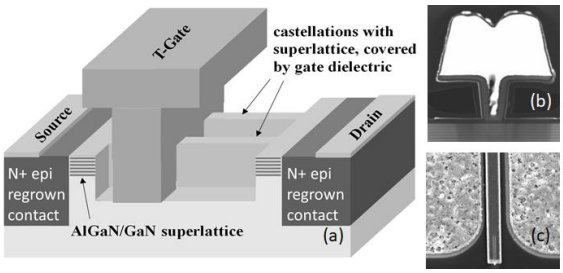

Fig. 1. (a) Structure of SLCFET amplifier device. (b) Cross-sectional STEM of 0.1 μm T-gate. (c) scanning electron microscope (SEM) of SLCFET.

II. SLCFET Technology

An alternate approach to the conventional planar N-polar or the Ga-polar transistor structures is to utilize a 3-D device architecture, maximizing current capability through the use of a superlattice to stack several AlGaN/GaN heterostructures on top of each other. The superlattice castellated field effect transistor (SLCFET) uses this type of stacked AlGaN/GaN heterojunctions and etches these layers into parallel nanoribbons between source and drain. To control the charge within each of the stacked heterostructures, a 3-D gate structure is used to provide control of the resulting transistor, simultaneously addressing the charge in each individual 2DEG layer of the stacked heterostructures through the sidewalls

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of the nanoribbons. Fig. 1(a) illustrates the structure of the SLCFET device. Using a superlattice structure in the channel region allows for a significant increase in channel charge density per unit layout area, increasing as a function of the number of stacked heterostructures in the superlattice. The increased charge density minimizes the parasitic access resistances within the device and decreases the knee voltage while maximizing the available current density, all desirable for maximizing power and efficiency performance in mmW and *W*-band amplifiers. The 3-D gate enhances device output impedance for improved matching, power efficiency, and bandwidth of operation. The stacked structure of the 2DEG channels also serves to shield the majority of the channel charge from the deleterious effect of surface and buffer traps, as the inner stacked channels are surrounded by the charge of the outermost stacked channel layers.

The SLCFET technology was first invented and demonstrated as a device structure that bypasses the fundamental limits of transistor RF switch performance [7], [8], [9], but this device structure has since also been demonstrated as a capable mmW amplifier [10], achieving a P_{out} of 9.5 W/mm with an associated PAE of 41% and an OIP3/$P_{1\ \text{dB}}$ = 14 dB at 30 GHz [11]. Similar, closely related device structures have also lately been proposed as kV power switches [12] and for mmW amplification [13]. The SLCFET type of device structure offers a number of device and process parameters to optimize mmW and *W*-band performance not available in conventional planar HEMT structures (e.g., nanoribbon width, length, and pitch), as has been discussed previously in the literature [14]. The combination of increased opportunities for device performance optimization and the inherent attributes of high channel charge densities that are self-shielding from the effect of surface and buffer states makes SLCFET attractive as a *W*-band high-power density amplifier.

III. Results and Discussion

A. FET Characteristics

The SLCFET metal organic chemical vapor deposition (MOCVD) AlGaN/GaN superlattice is composed of six heterostructures grown on 100 mm diameter semi-insulating SiC wafers, providing an epitaxial sheet resistance of 70 Ω/□. Very low contact resistance is achieved in the process by using selectively n+ GaN regrown source and drain contacts, achieving <0.05 Ω-mm. An insulated T-gate structure is used with the SLCFET, minimizing current leakage between the gate and the stacked heterostructures. A T-gate with a 100 nm gate length, as shown in Fig. 1(b), is used to build the SLCFET amplifier cells.

A typical transfer characteristic of a SLCFET amplifier cell is shown in Fig. 2. Note that all normalized current and power levels in this letter use the layout gate periphery in the same fashion as a conventional planar HEMT structure, so that all SLCFET normalizations incorporate both nanoribbon and castellated trench regions. The SLCFET amplifier has a pinchoff voltage of –3.8 V and a device breakdown of ∼60 V. It's I_{DS} increases from 2 A/mm at $V_{\text{GS}} = 0$ V to 3.5 A/mm at $V_{\text{GS}} = 2$ V with $V_{\text{DS}} = 5$ V. This substantial increase in current under forward bias is a result of additional charges introduced into the device, both from counteracting the effects of the gate work function's partial depletion of the nanoribbons, as well

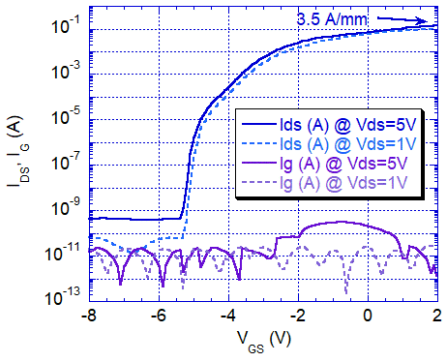

Fig. 2. Typically measured transfer characteristics of the SLCFET amplifier cell. The SLCFET employs a gate dielectric, minimizing gate leakage while supporting high I_{DS} current densities.

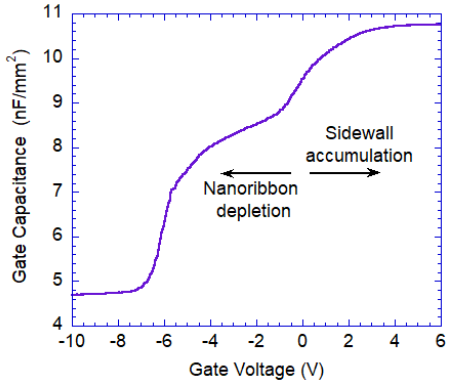

Fig. 3. *C–V* plot of a SLCFET device, demonstrating the presence of the normally ON the charge from the stacked 2DEG layers in the nanoribbons, and the normally-OFF charge from charge accumulation at the sidewall semiconductor–dielectric interfaces.

as accumulation of charge that forms along the sidewalls of the SLCFET that adds to the existing 2DEG charges in the stacked heterostructures. This behavior can be observed in the *C–V* characteristics of a SLCFET device that is measured with source and drain shorted and a bias sweep applied to the gate, as shown in Fig. 3. It is observed that there are two distinct charge groupings centered slightly off the 0 V bias point (an offset due to the gate work function), with the charge on the positive bias side being associated with the sidewall accumulation charges and the charge on the negative bias side associated with the charge being depleted from the nanoribbon 2DEG layers.

These two charge regimes within the device can also be observed in the SLCFET transconductance (g_m), derived from the transfer characteristic and plotted in Fig. 4. The g_m versus gate bias demonstrates a double peak characteristic which combines one peak associated with the nanoribbon depletion effect under negative bias with another peak from the sidewall accumulation under positive bias. The result provides a maximum g_m = 605 mS/mm, but also a broad g_m response >500 mS/mm for gate biases between –1.5 and 1 V.

The high charge density of both stacked 2DEG layers and sidewall accumulation charge provides extremely high available current densities. Fig. 5 shows the pulsed output characteristics of a 2 × 20 μm SLCFET amplifier cell, exhibiting an I_{MAX} of 3.75 A/mm with a V_{GS} of 2 V and an I_{MAX} of 4.8 A/mm with a $V_{\text{GS}} = 4$ V at $V_{\text{DS}} = 10$ V. The

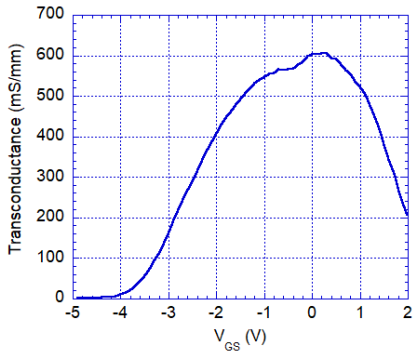

Fig. 4. Transconductance versus gate bias of the SLCFET amplifier cell, with a peak $g_m = 605$ mS/mm. The double peak behavior reflects the nanoribbon depletion and sidewall accumulation effect on either side of ~0 V gate bias.

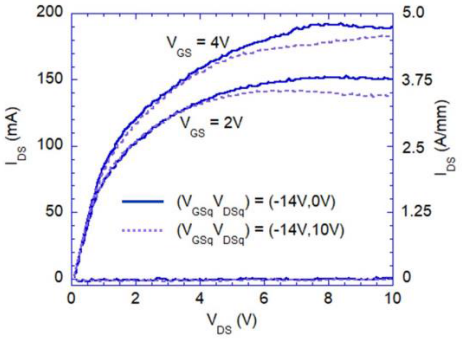

Fig. 5. Pulsed I–V measurement of a 2 × 20 μm SLCFET amplifier cell, demonstrating $I_{MAX} = 3.75$ A/mm at $V_{GS} = 2$ V and $I_{MAX} = 4.8$ A/mm at $V_{GS} = 4$ V. Pulse testing with 0.2 μs pulse lengths and 2 ms pulse separation, demonstrates a current collapse of <7% over the sweep and <1% at the knee voltage.

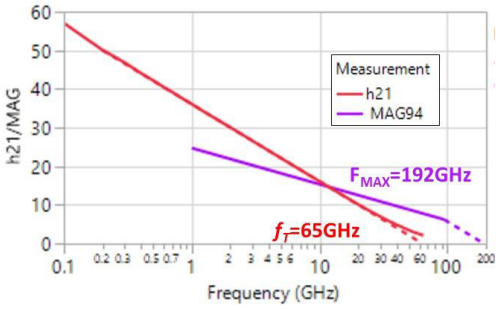

Fig. 6. Small signal h21/maximum available gain (MAG) plot of 2 × 20 μm SLCFET amplifier cell with a 0.1 μm T-gate. F_{MAX} extrapolated from a –20 dB/decade line extended from the maximum frequency of testing, to capture a lower bound to F_{MAX} for the SLCFET amplifier cell.

dispersion effects observed in the gate and drain lag testing of the SLCFET structure are minor, with this example showing current collapse from drain lag <1% at the knee voltage and <7% at saturation. The current at higher drain bias is also minimally affected by thermal effects, due to the thermal advantages that the castellated gate structure provides [15].

The small signal RF performance of the SLCFET amplifier measured using a parameter network analyzer (PNA-X) and a drain bias of 12 V is shown in Fig. 6, with an extrapolated $f_t = 65$ GHz and $F_{MAX} \geq 192$ GHz, providing useful gain at W-band frequencies.

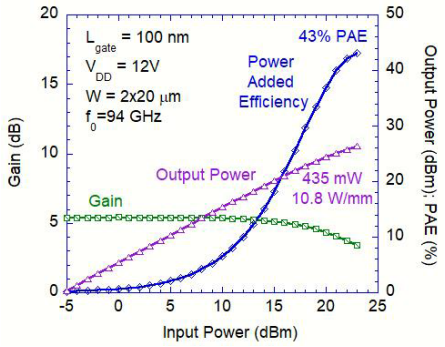

Fig. 7. Load–pull of SLCFET 2 × 20 μm amplifier cell, tested at 94 GHz with $V_{DSq} = 12$ V and $I_{Dq} = 30$ mA. The amplifier demonstrated a maximum output power of 435 mW (10.87 W/mm), with a PAE of 43%.

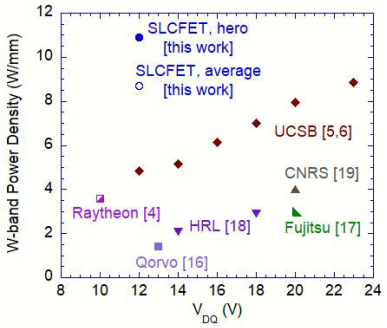

Fig. 8. Comparison from the literature of W-band power densities under load pull against quiescent drain bias.

B. Large Signal RF Characteristics

Large signal characteristics of a 2 × 20 μm SLCFET amplifier cell with no prematching were generated using a Maury load–pull system to tune the input and output loading of the device under CW drive, testing at 94 GHz with no external cooling, with the best device results shown in Fig. 7. This device was biased at $I_{Dq} = 750$ mA/mm and $V_{DS} = 12$ V, with the measured results of:

1) maximum $G_T = 5.4$ dB;
2) $P_{out} = 435$ mW, 10.87 W/mm; and
3) PAE at P_{out} maximum = 43%.

The average measured results of ten of these 2 × 20 μm SLCFET amplifier cells from the same wafer were:

1) average maximum $G_T = 5.6$ dB;
2) $P_{out} = 349$ mW, 8.7 W/mm; and
3) PAE at P_{out} maximum = 38%.

The extremely high current density of the SLCFET structure, combined with its low levels of current collapse under pulsed conditions and its low gate leakage current supports both very high power densities along with high power efficiency operation even at W-band (94 GHz) operation.

These power density and PAE values compare favorably against previously reported GaN technology power density and PAE levels measured at W-band. Fig. 8 plots reported W-band GaN transistor load–pull power densities as a function of quiescent drain bias, and Fig. 9 illustrates the reported PAE versus W-band power densities reported in the literature. The 10.87 W/mm demonstrated by the (Ga-polar) SLCFET is more than 2.5× greater than the highest previously reported W-band power density when using a Ga-polar GaN approach [19], and is 24% greater than the highest reported power density using an N-polar-based device [5]. At the same time, the

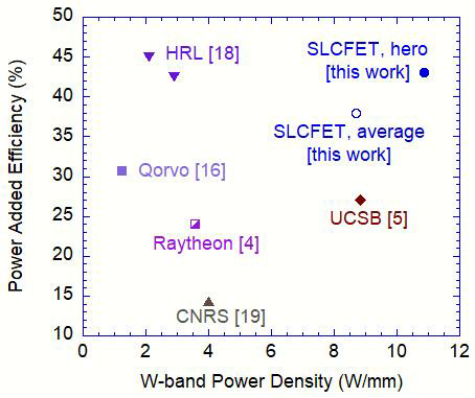

Fig. 9. Comparison from the literature of GaN W-band (94 GHz) power densities versus their reported PAEs.

SLCFET's high PAE is comparable to the highest W-band PAE reported in GaN, but at $>3\times$ the power density [18]. The stacked multichannel structure of the SLCFET that both increases the available current density while also minimizing current collapse effects provides this dramatic improvement in state-of-the-art W-band amplification capability.

IV. Conclusion

The SLCFET amplifier has demonstrated, to the best of our knowledge, the highest W-band power density from a GaN technology reported to date, with a $P_{\text{out}} = 10.87$ W/mm and PAE $= 43\%$ measured at 94 GHz. The SLCFET's unique multichannel structure and 3-D castellated gate support the extremely high current densities necessary to achieve this, in a structure that minimizes dispersion and current collapse effects that otherwise would limit power densities and efficiency at mmW/W-band amplification. By employing the same device structure previously demonstrated as the best-in-class RF switch, the SLCFET is positioned to enable the next generation of high-performance mmW and W-band communication and sensing applications.

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References

[1] M. Micovic et al., "GaN HFET for W-band power applications," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–3.

[2] D. F. Brown et al., "W-band power performance of AlGaN/GaN DHFETs with regrown n+ GaN ohmic contacts by MBE," in *IEDM Tech. Dig.*, Dec. 2011, p. 19.

[3] J.-S. Moon et al., "Power scaling of graded-channel GaN HEMTs with mini-field-plate T-gate and 156 GHz fT," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 796–799, Jun. 2021.

[4] E. M. Chumbes et al., "ScAlN-GaN transistor technology for millimeter-wave ultra-high power and efficient MMICs," in *IEDM Tech. Dig.*, Jun. 2022, pp. 295–297.

[5] B. Romanczyk et al., "W-band power performance of SiN-passivated N-polar GaN deep recess HEMTs," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 349–352, Mar. 2020.

[6] S. Wienecke et al., "N-polar GaN cap MISHEMT with record power density exceeding 6.5 W/mm at 94 GHz," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 359–362, Mar. 2017.

[7] R. S. Howell et al., "The super-lattice castellated field effect transistor (SLCFET): A novel high performance transistor topology ideal for RF switching," in *IEDM Tech. Dig.*, Dec. 2014, p. 11.

[8] R. S. Howell et al., "Low loss, high performance 1–18 GHz SPDT based on the novel super-lattice castellated field effect transistor (SLCFET)," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2014, pp. 1–5.

[9] R. S. Howell et al., "Advances in the super-lattice castellated field effect transistor (SLCFET) for wideband low loss RF switching applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–3.

[10] J. Chang et al., "The super-lattice castellated field-effect transistor: A high-power, high-performance RF amplifier," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1048–1051, Jul. 2019.

[11] J. Chang, S. Afroz, B. Novak, J. Merkel, K. Nagamatsu, and R. Howell, "Advances in the super-lattice castellated field effect transistor (SLCFET) for high power density, energy efficient RF amplification," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 576–579.

[12] J. Ma et al., "1200 V multi-channel power devices with 2.8 Ω•mm ON-resistance," in *IEDM Tech. Dig.*, Dec. 2019, p. 4.

[13] K. Shinohara et al., "Tu4E-4 multi-channel Schottky-gate BRIDGE HEMT technology for millimeter-wave power amplifier applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 298–301.

[14] S. Afroz et al., "Frequency performance improvements for SLCFET amplifier through device scaling," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Dec. 2021, pp. 1–4.

[15] C. Middleton et al., "Thermal transport in superlattice castellated field effect transistors," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1374–1377, Sep. 2019.

[16] Y. Cao et al., "Qorvo's emerging GaN technologies for mmWave applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 570–572.

[17] K. Makiyama et al., "Collapse-free high power InAlGaN/GaN-HEMT with 3 W/mm at 96 GHz," in *IEDM Tech. Dig.*, Dec. 2015, p. 9.

[18] J.-S. Moon et al., "W-band graded-channel GaN HEMTs with record 45% power-added-efficiency at 94 GHz," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 2, pp. 161–164, Feb. 2023.

[19] K. Harrouche, R. Kabouche, E. Okada, and F. Medjdoub, "High performance and highly robust AlN/GaN HEMTs for millimeter-wave operation," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1145–1150, 2019.