Realization of Low-Loss Fully Passive Harmonic Rejection N-Path Filters

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***Abstract*— This work presents a low-loss fully passive harmonic rejection (HR) N-path filter that performs finite impulse response (FIR) filtering within its core by sequentially charging the baseband capacitors and exploiting combined charge sharing and capacitor stacking techniques. The proposed HR N-path filter achieves an in-band (IB) gain of −2 to +0.5 dB across the 0.25-2 GHz frequency range while consuming 2.3–15.7 mW of power. It achieves an HR ratio (HRR) of >46/48 dB with >+8/+11 dBm third/fifth-order harmonic blocker P1dB.**

***Index Terms*— CMOS silicon-on-insulator (SOI), finite impulse response (FIR) filter, harmonic rejection (HR), linear periodically time-varying (LPTV) circuit, N-path filters, switched capacitor circuit.**

I. Introduction

HIGHLY TUNABLE integrated bandpass filters (BPFs) are required for various wireless applications such as wideband sub-6-GHz receivers and spectrum scanners [1], [2]. Aside from tunability, such applications demand high signal rejection at close-in and far-off frequencies. Traditional microwave filters have limited tunability and occupy a large footprint to implement inductors/transmission lines. Furthermore, many of these filters are transparent at odd harmonics of the center frequency and are far from being true BPFs [3].

In the past decade, N-path filters have gained a lot of attention due to their full reconfigurability, allowing their bandwidth and center frequency to be programed independently [4]. Active gyrators [5], ON-chip inductors [6], and rotating clock phases [7] have been used to develop higher order N-path filters in an attempt to improve close-in rejection. However, due to the comb-like filtering nature of N-path filters, blockers located near or at the local oscillator (LO) harmonics do not receive enough suppression and can cause saturation of the following circuitry. Because of the extended alias-free frequency range, more number of paths within the N-path filter are desirable. However, harmonic blockers become more problematic as N increases. This necessitates the addition of a comb-notch finite impulse response (FIR) filter with notches positioned at the harmonics of LO within the N-path circuit. Approaches that have been proposed thus far to realize harmonic rejection (HR) in N-path circuits have relied on active circuitry resulting in degrading noise, linearity, power consumption, area, and frequency tuning range [8].

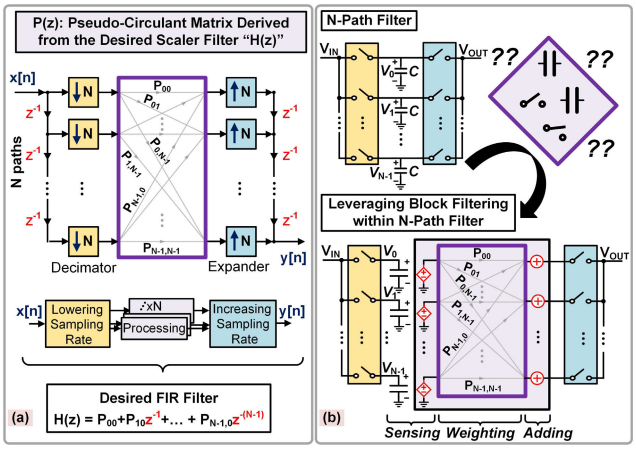

Fig. 1. (a) Digital block filtering concept and (b) its conceptual implementation in N-path filters.

In [9], a low-loss fully passive HR mixer and an interferer-tolerant receiver have been proposed that can eliminate blockers at or around the harmonics of the LO (up to the seventh harmonic). The proposed structure in [9] has built-in frequency translation and cannot be used as a standalone BPF. In this work, a new circuit architecture has been proposed to implement a low-loss fully passive N-path BPF that rejects harmonics up to the $N-1$ harmonic. For this purpose, capacitor stacking and charge-sharing techniques have been exploited in concert to create an FIR filter to null signals around LO harmonics.

II. Design of the HR N-Path Filter

Digital block filtering, shown in Fig. 1(a), is a technique to increase parallelism and create high-speed digital FIR filters [10]. For a given scalar FIR transfer function, $H(z)$, a corresponding Toeplitz pseudo-circulant block matrix, $P(z)$, can be constructed that enables an alias-free polyphase implementation of $H(z)$. Translating this technique to the analog domain within the N-path structure is not straightforward since it requires ideal sensing and summation of voltages stored on the baseband capacitors across multiple paths without creating undesired interactions [Fig. 1(b)]. Fig. 2 shows the evolution of the proposed low-loss fully passive HR N-path filter. Unlike the 8-path conventional filter, each path's capacitor, C, is divided into three capacitors, C_a, C_b, and C_a, and they are all charged in parallel when connected to the input such that different weights of the input signal can be obtained at different points in time. The special arrangement shown in

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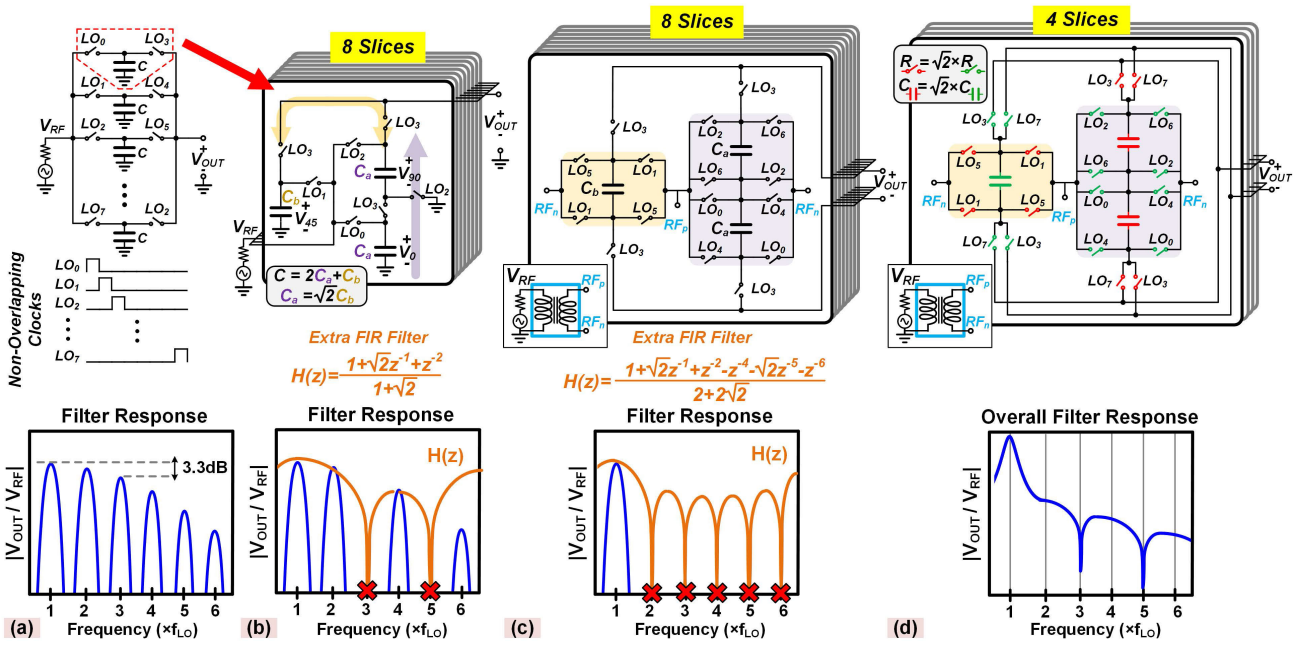

Fig. 2. Evolution of the proposed low-loss fully passive HR N-path filter and its frequency response. (a) Traditional 8-path filter. (b) 8-path filter with odd harmonic rejection. (c) 8-path filter with HR below the seventh harmonic. (d) Simplified 4-path HR filter with eight-phase clocking.

Fig. 2(b) allows these precharged capacitors to interact with one another to form the summing function when unblocking output switches are turned on. The two stacked capacitors form an equivalent capacitor with a value of $C_a/2$ and a stored voltage of $(1+z^{-2})V_{\mathrm{RF}}$. The charge sharing resulting from C_b being parallel to this effective capacitor ensures third and fifth HR if a properly sized $C_b = C_a/\sqrt{2}$ is chosen. Note that realizing the desired three-tap HR filter with charge sharing alone would suffer from substantial insertion loss, especially for high-Q filtering schemes with large capacitor values. In Fig. 2(b), instead of invoking charge sharing three times, capacitor stacking is applied to generate the first and third taps thus minimizing the number of charge sharing occurrences required during each summing operation. Moreover, the passive voltage gain of the stacked capacitors partially offsets the loss of the single charge-sharing event, resulting in low-loss filter realizations even when large capacitors are required for sharp bandpass filtering. Once the third/fifth harmonics are eliminated, using anti-phase switching of the differential input as shown in Fig. 2(c) takes care of even order harmonics. Furthermore, the eight parallel slices in Fig. 2(c) do not all represent independent switching patterns. For every other four slices, the switching pattern repeats, with the only difference being that the core sampling capacitors are flipped when connected to the differential RF input. It is, therefore, possible to modify the circuit in Fig. 2(c) so that the common capacitors and switches are shared, as shown in Fig. 2(d). By reusing capacitors and switches, the entire layout becomes more centralized, reducing layout mismatches.

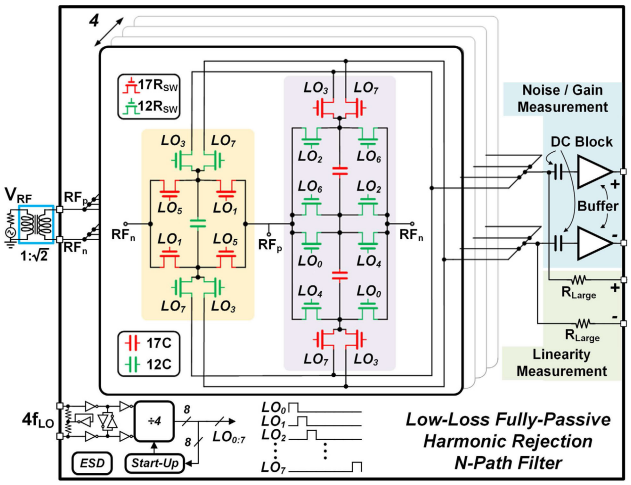

Fig. 3. Block diagram of the low-loss fully passive HR N-path filter with HR up to the seventh harmonic.

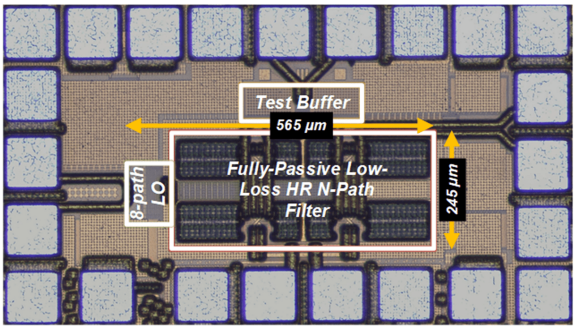

Fig. 4. Die micrograph.

III. Implementation

A filter prototype is designed and fabricated in 45-nm CMOS SOI technology. The architecture of the proposed low-loss fully passive HR N-path filter is illustrated in Fig. 3. For the purpose of the gain/noise measurements, a pseudo-differential test buffer is used to drive the 50 Ω load of the spectrum analyzer. The dc block capacitors allow independent biasing of the filter and the test buffer. The output of the HR N-path filter is tapped with two large resistors for the linearity measurements, such as IIP3 and blocker P1dB. An OFF-chip wideband RF balun performs the single-to-differential signal conversion. An HR rejection technique discussed in Section II

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

	JSSC 2015 [1]	RFIC 2016 [2]	JSSC 2011 [4]	TMTT 2014 [3]	IMS 2016 [5]	JSSC 2019 [6]	IMS 2022 [7]	This Work
Type	Receiver	Receiver	Filter	Filter	Filter	Filter	Filter	Filter
Architecture	Noise-Cancelling Receiver with HR-TIAs	Filtering by Aliasing	N-Path Filter	λ/2 Resonator with Center-Tapped Open-Stub	Dual Adaptive TRZ Using N-Path Circuit	Coupled N-Path Resonators	Rotary Clocking N-Path Filter	Low-Loss Fully-Passive HR N-Path Filter
CMOS Technology	28nm	65nm	65nm	PCB Rogers 4350B	65nm	65nm	65nm	45nm SOI
RF Input	Differential	Differential	Differential	Single-Ended	Differential	Differential	Single-Ended	Differential
Frequency Range [GHz]	0.1-3.3	0-1	0.1-1.0	0.58-0.91	0.2-1.2	0.8-1.1	0.2-0.8	0.25-2
IB Gain [dB]	NR	NR	-2	-1.53	+21	-4.6 ~ -3.8	+10.2	-2 ~ +0.5
BW [MHz]	0.2-3	10, 20	35	115-315[1]	6.2	30-50	40	80
NF [dB]	1.7[2]	32	3-5	1.53	4.5-6.2	5.0-8.6	3.7-6.4[2]	3.1-5.0[2]
OOB Blocker P1dB [dBm]	0 (Δf/BW=40)	NR	+2	NR	+8	+9 (Δf/BW=1)	-1 (Δf/BW=2.5)	+2.5 (Δf/BW=1) +8 (Δf/BW=2)
IB/OOB IIP3 [dBm]	+11.5	+31 (Δf/BW=5)	+14	+13-+19[3]	-1[4] (Δf/BW=0.32) +18 (Δf/BW=7.25)	+24 (Δf/BW=1)	+4.5 +12.9 (Δf/BW=2.5)	+27.8 (Δf/BW=1) +29.4 (Δf/BW=2.5)
Power Consumption [mW]	36.8-62.4	8	2-16	0	30-70	80-97	5.5-38	2.3-15.7
Supply Voltage [V]	1	1.2/1	NR	0-28[5]	1.2	1.0/2.5	NR	1.1
Active Area [mm^2]	5.2	1.68	0.07	1338[6]	2.2	1.9	0.56	0.14
$3f_{LO}/5f_{LO}$ HR [dB]	60/60[7]	27 @$3f_{LO}$ 36 @$5f_{LO}$	10 @$3f_{LO}$[4] 17 @$5f_{LO}$[4]	3 @$3f_0$[4,8]	NR	22 @$3f_{LO}$[4]	NR[8]	>46 @$3f_{LO}$ >48 @$5f_{LO}$
Harmonic B_{1dB} [dBm]	-6.5 @$3f_{LO}$ -3 @$5f_{LO}$	NR	NR	NR	NR	NR	NR	>8 @$3f_{LO}$ >11 @$5f_{LO}$

[1] Tuning of seven separate varactors is required. [2] Buffer noise contribution is de-embedded. [3] Limited to the tuning varactors. Numbers are estimated based on datasheets of the varactors. [4] Estimated from measurement plots. [5] Used for varactor tuning. [6] Estimated from fabrication plot. [7] Harmonic rejection is performed in two stages. [8] Filter is transparent around $3f_0$ and $5f_0$.

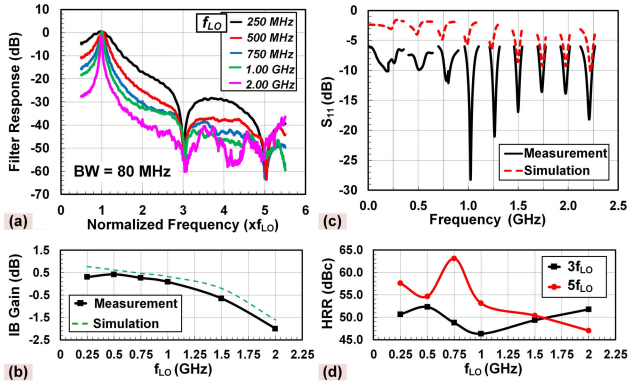

Fig. 5. (a) Measured filter response up to sixth harmonics of clock frequency for multiple LO. The bandwidth of the filter is kept constant at 80 MHz for all measurements. (b) Measured and simulated IB gain for multiple LO. In the simulation, ideal switches with zero ON-resistance are assumed. (c) Measured and simulated S_{11} versus RF frequency for multiple LO. (d) Measured third and fifth HRR for multiple LO.

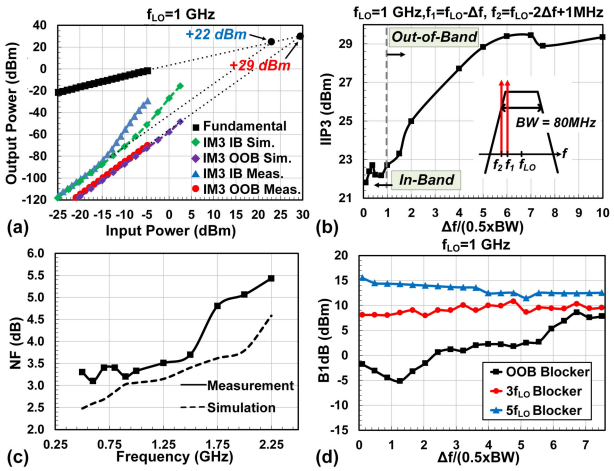

Fig. 6. (a) Measured and simulated IB and OB IIP3 for $f_{LO} = 1$ GHz demonstrating a high level of linearity. The 3-dB voltage gain of the input balun is not de-embedded for all linearity measurements. (b) Measured IIP3 versus offset frequency for $f_{LO} = 1$ GHz. (c) Measured and simulated NF for multiple LO. (d) Measured B1dB and HB1dB versus the offset frequency for $f_{LO} = 1$ GHz.

is embedded in the 8-path filter to eliminate LO harmonics up to the seventh harmonic. In the implemented HR filter, the nonrational ratio of $1{:}\sqrt{2}$ is approximated by 12:17. The switches in Fig. 3 are scaled to ensure equal time constants in sampling and summation periods for all capacitors. The switches within the filter are driven by eight-phase 12.5% nonoverlapping clocks.

IV. MEASUREMENT RESULTS

Fig. 4 shows the die micrograph with an active area of 0.14 mm^2. Fig. 5 illustrates the measured performance of the proposed low-loss fully passive HR 8-path filter response across the frequency range of 0.25–2 GHz. For all of these measurements, the BW is kept constant at 80 MHz. As can be seen, out-of-band (OB) rejection increases monolithically and no spur exists in the plot. In fact, distinct deep notches can be observed at $3f_{LO}$ and $5f_{LO}$ in the filter response. The in-band (IB) gain is 0.5 dB for low clock frequencies, and as Q increases, it drops to -2 dB at high clock frequencies. In addition, measured values of IB gain are in good agreement with simulations. It should be noted that the 3-dB voltage gain of input balun is de-embedded here. An HR ratio (HRR) of >46 and >48 dB has been achieved for the third and fifth harmonics, respectively. S_{11} does not show a perfect match at low frequencies. This is to be expected since the filter's output is not resistively terminated and only sees the test buffer's capacitive loading. Due to the parasitic capacitances and loss caused by charge sharing, S_{11} falls below -10 dB for higher clock frequencies.

Fig. 6 shows the large-signal and noise figure (NF) measurement results. The NF varies between 3.1 and 5.0 dB across the

frequency range of 0.25–2 GHz. B1dB at close-in frequencies is -5 dBm and increases up to $+8$ dBm at large blocker offsets measured at the 1-GHz clock frequency. The harmonic B1dB (HB1dB) for the third harmonic is $>+8$ and $>+11$ dBm for the fifth harmonic, regardless of the offset frequency. An IB IIP3 of $+22$ dBm and a maximum OB IIP3 of $+29.6$ dBm are achieved.

Table I compares the performance with prior N-path filters and mixer-first receivers. This work demonstrates the first fully passive HR N-path filter that achieves >46 dB HRR with high linearity and low loss. Compared to [2] and SongJSSC2019, this work achieves a much higher HRR. The harmonic B1dB of this work is the highest of any reported value for prior filters/receivers.

V. Conclusion

In this letter, a low-loss fully passive HR N-path filter structure is presented. The proposed HR N-path filter offers high linearity, tunability, and high rejection of signals around the harmonics while operating with low power in a small form factor. Furthermore, the proposed structure requires no additional circuitry beyond extra switches and benefits from technology scaling.

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References

[1] D. Murphy, H. Darabi, and H. Xu, "A noise-cancelling receiver resilient to large harmonic blockers," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1336–1350, Jun. 2015.

[2] N. Sinha, M. Rachid, and S. Pamarti, "An 8 mW, 1 GHz span, passive spectrum scanner with $>+31$ dBm out-of-band IIP3," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 278–281.

[3] X. Luo, S. Sun, and R. B. Staszewski, "Tunable bandpass filter with two adjustable transmission poles and compensable coupling," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2003–2013, Sep. 2014.

[4] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

[5] M. N. Hasan, Q. J. Gu, and X. Liu, "Tunable blocker-tolerant RF front-end filter with dual adaptive notches for reconfigurable receivers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.

[6] P. Song and H. Hashemi, "RF filter synthesis based on passively coupled N-path resonators," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2475–2486, Sep. 2019.

[7] M. Khorshidian, S. L. N. Garimella, A. Nagulu, and H. Krishnaswamy, "An inductor-less all-passive higher-order N-path filter based on rotary clocking in N-path filters," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 241–244.

[8] Y. Xu, J. Zhu, and P. R. Kinget, "A blocker-tolerant RF front end with harmonic-rejecting N-path filter," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 327–339, Feb. 2018.

[9] S. Araei, S. Mohin, and N. Reiskarimian, "An interferer-tolerant harmonic-resilient receiver with $>+10$ dBm 3^{rd} harmonic blocker P_{1dB} for 5G NR applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 18–20.

[10] P. P. Vaidyanathan and S. K. Mitra, "Polyphase networks, block digital filtering, LPTV systems, and alias-free QMF banks: A unified approach based on pseudocirculants," *IEEE Trans. Acoust., Speech Signal Process.*, vol. ASSP-36, no. 3, pp. 381–391, Mar. 1988.