A $K_a$-Band Transformer-Based Switchless Bidirectional PA-LNA in 90-nm CMOS Process

Tzu-Yang Chiu¹, Yunshan Wang, and Huei Wang²

Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan

¹k0989480678@gmail.com, ²hueiwang@ntu.edu.tw

Abstract—This paper presents a switchless bidirectional power amplifier-low noise amplifier (PA-LNA) in 90-nm CMOS process for millimeter-wave (mm-wave) phased-array front-end chip. This PA-LNA uses current-type transformer (TF) as a bidirectional matching network for PA and LNA inputs/outputs without using lossy T/R switches. As a side benefit, avoiding the use of the T/R switches not only saves the chip area, but also prevents performance degradation in PA and LNA modes. The proposed PA-LNA achieves peak small-signal gain of 18.3 dB and 17.6 dB in PA and LNA mode, respectively. In the PA mode, it achieves the measured peak saturated output power ($P_{\text{sat}}$) of 15.1 dBm with 29 \% peak power-added efficiency (PAE$_{\text{MAX}}$) and 13.3 dBm peak 1-dB output power (OP$_{\text{MAX}}$) at 33 GHz, while LNA mode achieves minimum noise figure (NF) of 4.7 dB at 36 GHz. The reverse isolation in both modes is better than 43 dB. The core size without pads is 0.21 mm$^2$.

Keywords—CMOS, millimeter wave (mm-wave) phased-array systems, Front-end, T/R switch, bidirectional amplifier, low-noise amplifier (LNA), power amplifier (PA), transformer.

I. INTRODUCTION

The $K_a$-band phased-array systems are widely used for satellite communications, close-range radars, and fifth-generation (5G) applications. In the phased-array system, the most critical part is the T/R front-end, which usually consists of a low-noise amplifier (LNA), power amplifier (PA) and using T/R switches with high isolation to prevent leakage signal problem in PA or LNA modes. However, the T/R front-end usually suffers from switches insertion loss, which deteriorates the noise performance in LNA mode and degrades the output power in PA mode. To resolve this issue, the switchless bidirectional amplifiers by directly connecting the PA and LNA inputs/outputs have been proposed without adopting lossy T/R switches [1]-[3].

In this paper, a new topology of the switchless bidirectional power amplifier-low noise amplifier (PA-LNA) is proposed. The current-type transformer (TF) is used as the bidirectional matching for both input and output parts. In addition, it is also a high impedance transformation network for off-state PA/LNA in LNA/PA modes without affecting on-state matching. This switchless PA-LNA achieves a measured small signal gain of 18.3 dB, a peak saturated output power ($P_{\text{sat}}$) of 15.1 dBm with peak power-added efficiency (PAE$_{\text{MAX}}$) of 29 \% at 33 GHz in PA mode. In LNA mode, it achieves a small-signal gain of 17.6 dB and a minimum noise figure (NF) of 4.7 dB at 36 GHz. The reverse isolation in both modes is better than 43 dB.

Fig. 1. Complete schematic of the proposed switchless bidirectional PA-LNA.

II. CIRCUIT DESIGN

Fig. 1 shows the complete schematic of the proposed PA-LNA. The PA and LNA are composed of two-stage pseudodifferential NMOS pairs with cross-coupled neutralization capacitors adopted to enhance the gain performance and eliminate the parasitic capacitance $C_{gd}$ that causes circuit instability. The capacitive neutralization is implemented using metal layers M6 to M9 interdigital structure for reducing chip area. The proposed PA-LNA uses TF-based-baluns for compact inter-stage matching. Furthermore, the PA-LNA applied current-type TF as a bidirectional matching network to share the same input and output ports to achieve bidirectional function.

For PA design, the drain bias voltages ($V_{d1}, V_{d2}$) of the power and driver stage are set to 1.2 V for maximum output voltage-swing. The power stage with 256-\mu m total gate width is biased in high class-AB ($V_{g2} = 0.65$ V) for the trade-off between the output power and power-added efficiency performances. The driver stage with a total gate width of 128 \mu m is biased in the deep class AB region ($V_{g1} = 0.32$ V) to make OP$_{\text{MAX}}$ close to $P_{\text{sat}}$ [4]. For LNA design, the gate voltages ($V_{g2}, V_{g3}$) of the first and second stage are biased at 0.5 and 0.6 V under drain voltage ($V_{d3}$=1V, $V_{d4}$=0.5V) for optimum noise performance, sufficient gain and save dc-power.

In the PA mode, the PA core is activated by setting the gate and drain bias voltages ($V_{g1}, V_{g2}, V_{d1}, V_{d2}$) to the designed value,
while the LNA core is deactivated by turning off the gate and drain bias voltages ($V_{g3}$, $V_{g4}$, $V_{d3}$, $V_{d4}$) to prevent the risk of the positive feedback, which will cause the oscillation problem. In LNA mode, the working principle is also a relative, that is, the LNA core is activated and PA core is turned off by switching the gate and drain bias voltages.

The most important specifications in the bidirectional PA-LNA design are the PA output power and LNA noise performance. Therefore, the PA output network and LNA input network need to be carefully designed.

In millimeter-wave (mm-wave) frequency, the off-state input and output impedance of the PA and LNA are not ideally open due to its parasitic capacitances which leads to signal leakage problem from the PA to LNA path or LNA to PA path. Therefore, how to avoid signal leakage in a switchless bidirectional PA-LNA is a challenge. To tackle this issue, the current-type TF is used to achieve high impedance transformation at the input and output of the off-state PA when the circuit operates in LNA mode, and off-state LNA when the circuit operates in PA mode, respectively, without affecting the on-state matching conditions. Fig. 2 shows the simplified equivalent circuit of the proposed PA-LNA in PA mode. The original input/output impedance of the off-state LNA is (6-j88) and (11-j131) Ω, which causes signal leakage problem and hence degrades the power performance in PA mode. By applying the current-type TF with capacitor in parallel ($C_{1}$, $C_{2}$), the impedance is transformed to (148-j3) and (141+j48) Ω at input and output of the off-state LNA, hence the signal leakage issue is alleviated in PA mode. Fig. 3 shows the simplified equivalent circuit of the proposed PA-LNA in LNA mode, the input and output impedance of the off-state PA is only (9-j74) and (5-j43) Ω. After passing through the current-type TF, the impedance becomes (190-j27) and (240+j59) Ω. Therefore, by adopting current-type TF, the noise performance can be optimized and the signal leakage is reduced in LNA mode.

III. MEASUREMENT RESULTS

Fig. 4 shows the chip micrograph of the proposed K-ν-band switchless bidirectional PA-LNA which is fabricated in 90-nm CMOS process. The core area of this circuit is 0.21 mm² (0.65 mm x 0.33 mm) excluding bypass capacitors, dc- and RF- pads. All measurement results were performed on-wafer using GSG RF probes and PGPPGP dc probes. The $S$-parameters are measured with an Agilent E8361A PNA network analyzer. Fig. 5(a) shows the measured and simulated $S$-parameters of the PA-LNA in LNA mode. The measured peak gain under $P_{dc}$ of 25 mW is 17.6 dB and the 3-dB bandwidth is 4.1 GHz covers from 34 GHz to 38.1 GHz. Compared with simulations, the measured $S$-parameters agree reasonable with simulation. Fig. 5(b) exhibits the measured and simulated NFs in LNA mode. The minimum NF is 4.7 dB at 36 GHz. Compared with simulation, the measured NF is shifted to the lower frequency by about 2 GHz, which may be caused by the imperfect ground condition due to the hollow grounds of the transformers. Fig. 6(a) shows the measured and simulated $S$-parameters of the PA-LNA in PA mode. The measured results agree reasonable with simulations and achieve a peak gain of 18.3 dB with a 3-dB bandwidth from
30 to 39.2 GHz. The large-signal measurement is through Keysight E8267D signal generator and an Agilent E4448A spectrum analyzer. Fig. 6(b) shows the measured and simulated continuous-wave (CW) large-signal characteristics in PA mode at 33 GHz. At 33 GHz, the proposed PA-LNA achieves 29 % peak PAE\textsubscript{MAX}, 15.1-dBm peak P\textsubscript{sat} and 13.3-dBm peak OP\textsubscript{1dB} with 16.2-dB power gain. The measured PAE\textsubscript{MAX}, P\textsubscript{sat} and OP\textsubscript{1dB} across measured frequencies are shown in Fig. 7. From 32 GHz to 38 GHz, the PA-LNA achieves >14.5-dBm P\textsubscript{sat}, >12-dBm OP\textsubscript{1dB} and >22.5-% PAE\textsubscript{MAX}. Fig. 8 shows the measured reverse isolation in PA and LNA modes. It is found that the implemented PA-LNA has good reverse isolation which is better than 43 dB.

Table 1 summarizes the performance of this PA-LNA and recently published bidirectional PA-LNAs and front-ends. The proposed PA-LNA shows comparable P\textsubscript{sat}/PAE\textsubscript{MAX} in PA mode and good NF in LNA mode. This work shows comparable performance comparing with those works implemented in better process and operates at higher frequencies.

IV. CONCLUSION

In this paper, a fully integrated switchless bidirectional PA-LNA in 90-nm CMOS process for mm-wave phased-array front-end chip is presented. The proposed PA-LNA uses current-type TF as a bidirectional matching network for PA and LNA input/output without adopting lossy T/R switches. Due to this topology, the chip area can be minimized and the influence of the T/R switches loss is avoided so as not to degrade the performance in PA and LNA modes.

ACKNOWLEDGMENT

The radio frequency integrated circuit (RFIC) chip is fabricated by Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan through Taiwan Semiconductor Research Institute (TSRI) in Taiwan.

REFERENCES


