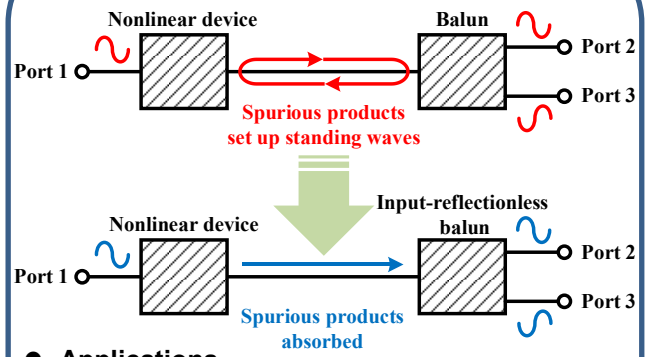
Input-Reflectionless 2.4-3.8 GHz Balun With Low Phase/Amplitude Imbalance Using Stacked-Coupled Microstrip Line

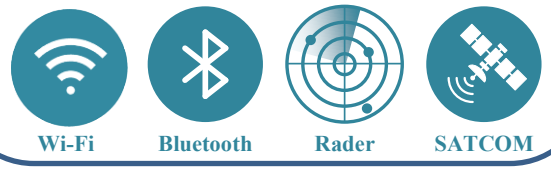
S. Zhang, Y. Rao, Y. Dong, X. Luo

STATUS QUO

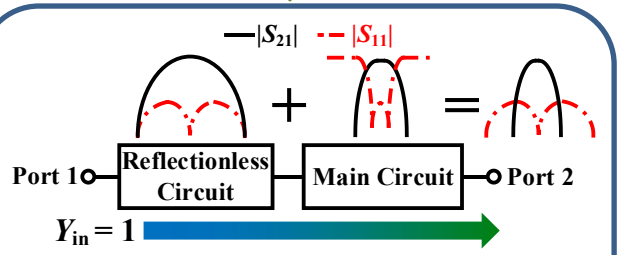
- **Background and motivation**



- **Applications**



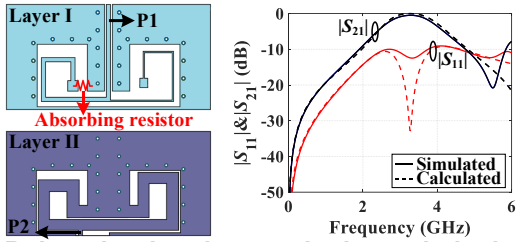
NEW INSIGHTS



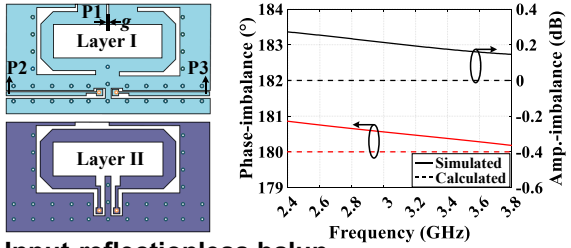
- **Reflectionless Circuit**
  Wide reflectionless range
- **Main Circuit**
  Low phase/amplitude imbalance

DESCRIPTION

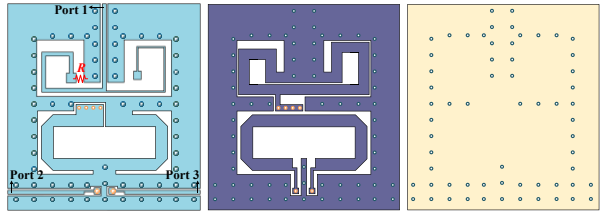
- **Reflectionless circuit using stacked-coupled microstrip line**
  A resistor is loaded to absorb the power at stopband



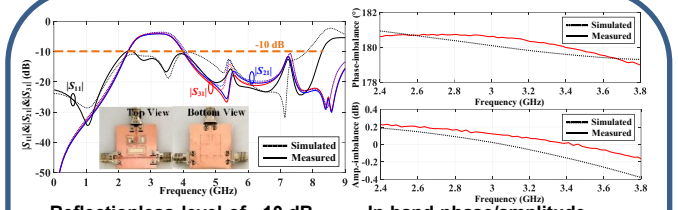
- **Balun circuit using stacked-coupled microstrip line**
  Two symmetrical U-shape couplers ensure high balance and miniaturized size



- **Input-reflectionless balun**
  Cascade reflectionless- and balun-circuits



QUANTITATIVE IMPACT



Reflectionless level of −10 dB from DC to 8.2 GHz

In-band phase/amplitude imbalance: ±1° /±0.22 dB

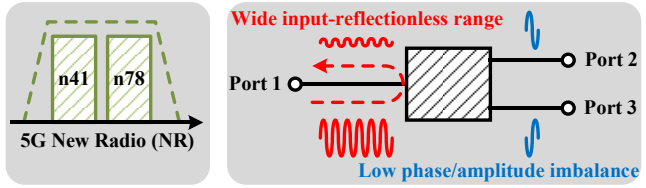
- **Comparison with state-of-the-arts**

Ref.	2021 MWCL	2019 EuMC	2022 TMTT	This Work
Technology	Coupled line	Microstrip & slot-line	Microstrip & slot-line	**Stacked-coupled microstrip line**
f_0(GHz)	3.6	2	0.988	**3.1**
IL*(dB)	1.8	0.5	0.67	**1.1**
FBW(%)	19	98.8	56.78	**45**
A.-Im(dB)/ P.-Im(°)**	0.3/3	0.16/1	0.35/2.61	**0.22/1**
Reflectionless Range (GHz)	N/A	0.01 to 5	0.01 to 3	**0.01 to 8.2**
Core Size	0.0558 (λ_g^2)	2133 mm^2	N/A	**0.0504 (λ_g^2) 170.8 mm^2**

*: Insertion loss. **: Amplitude-Imbalance/Phase-Imbalance.

PROPOSED CONCEPT GOALS

- **Feature**



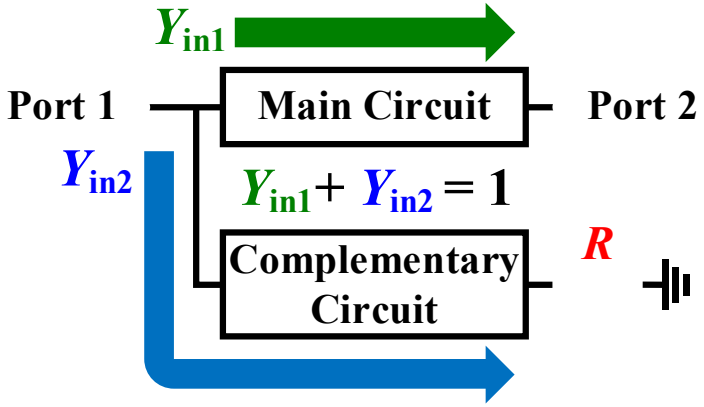
- **Next step**
  Expand reflectionless range and achieve three-port reflectionless balun

Input-Reflectionless Balun Scheme

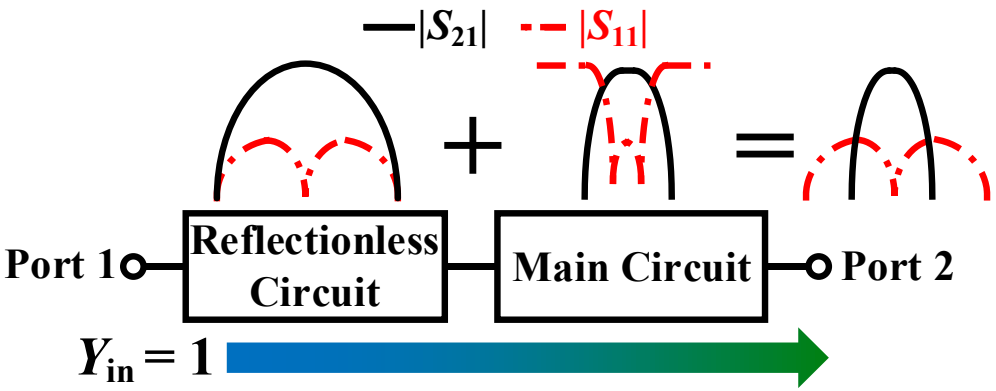
- **Conventional reflectionless scheme**
  - An additional path to absorb the power at stopband
  - Condition: $Y_{in1} + Y_{in2} = 1$

Simplify the implementation

- **Proposed reflectionless scheme**
  - Reflectionless circuit is located at the front-end of main circuit
  - Condition: $Y_{in} = 1$



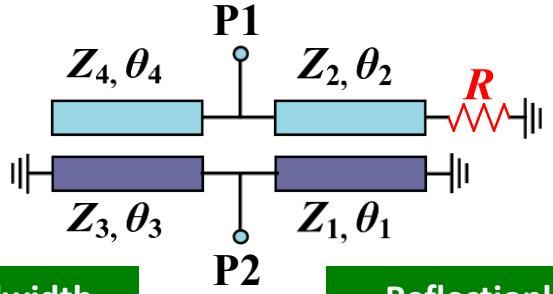
Conventional scheme

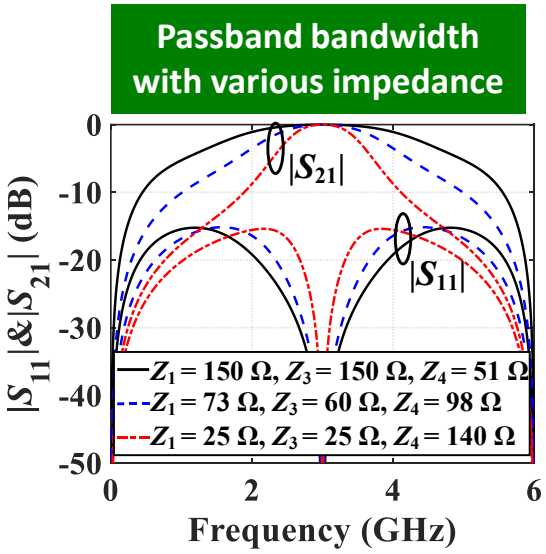


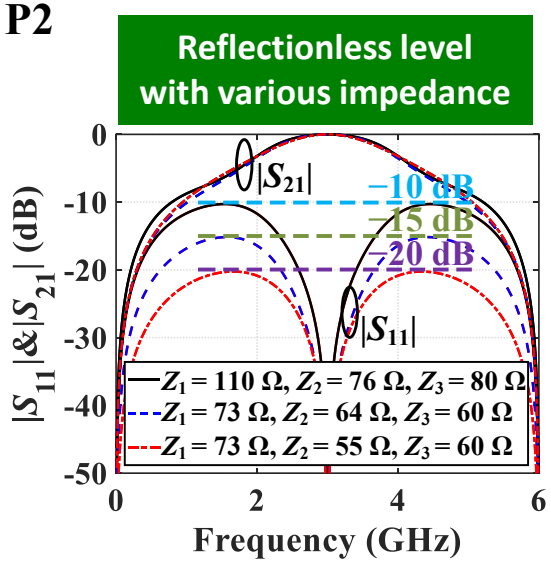
Proposed scheme

Reflectionless Circuit

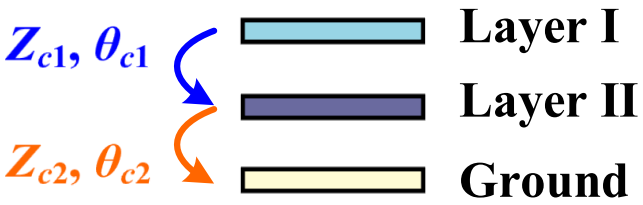
- **Ideal equivalent circuit model**
  - A resistor is located at the end of microstrip line to absorb power at stopband
  - Optimize passband bandwidth and reflectionless level by adjusting impedance of microstrip

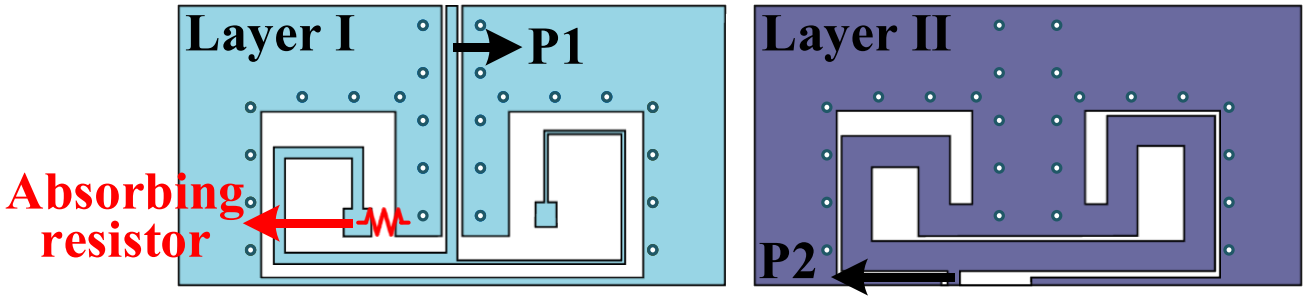






- **Reflectionless circuit using stacked-coupled microstrip line**

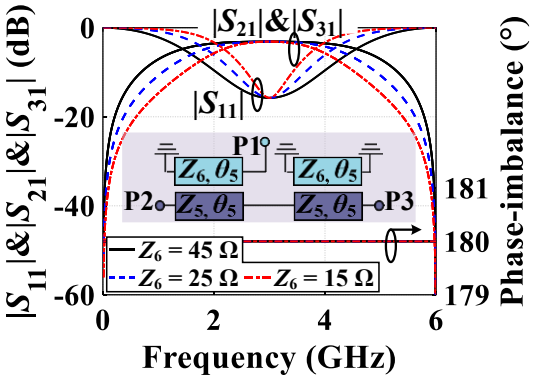




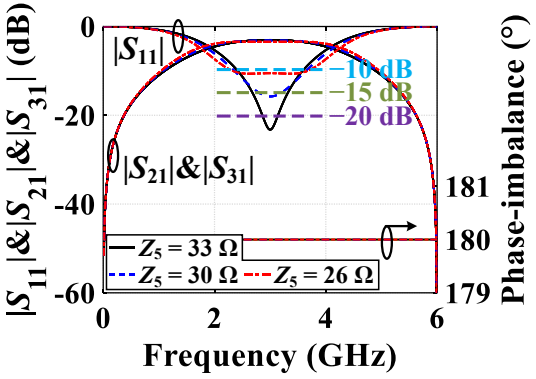
Balun Circuit

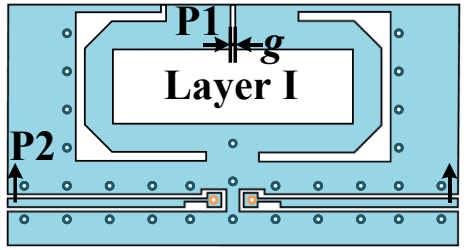
- **Ideal equivalent circuit model**
  - ➢ Consists of two symmetrical couplers
  - ➢ Optimize passband bandwidth and return loss by adjusting impedance of microstrip
- **Balun circuit using stacked-coupled microstrip line**
  - ➢ Set two symmetrical couplers as U-shape for size miniaturization
  - ➢ Optimize the Imbalance of the balun by adjusting the gap *g*

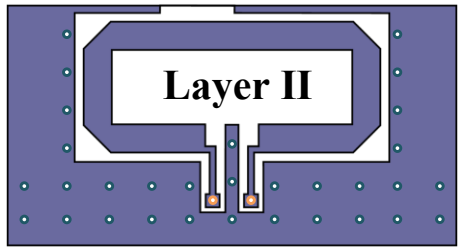
Passband bandwidth with various impedance

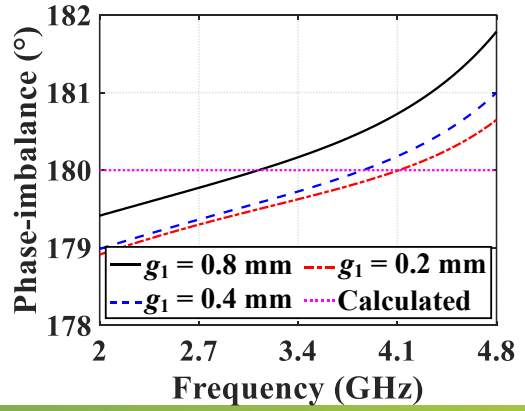


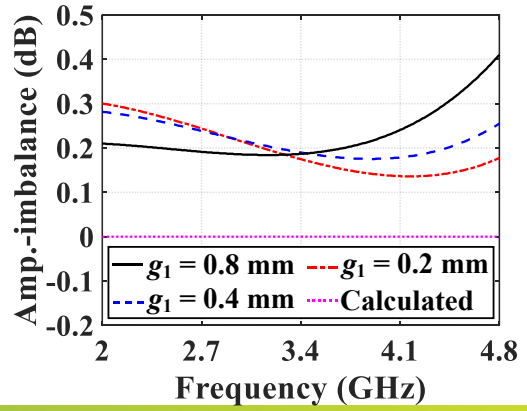
Return loss with various impedance







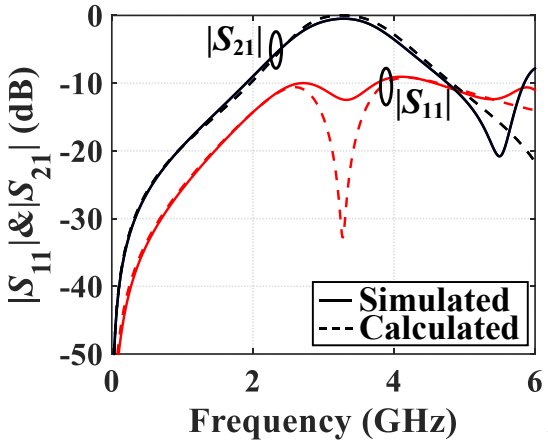




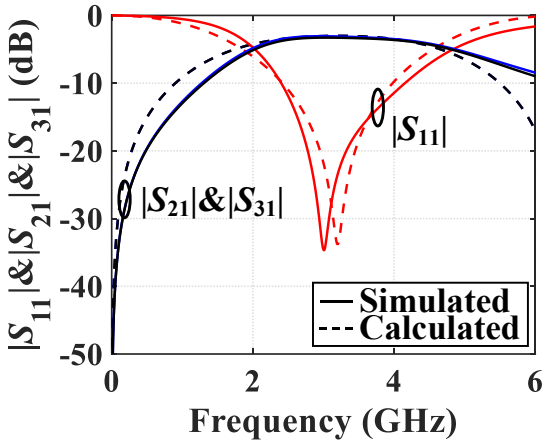
Input-Reflectionless Balun

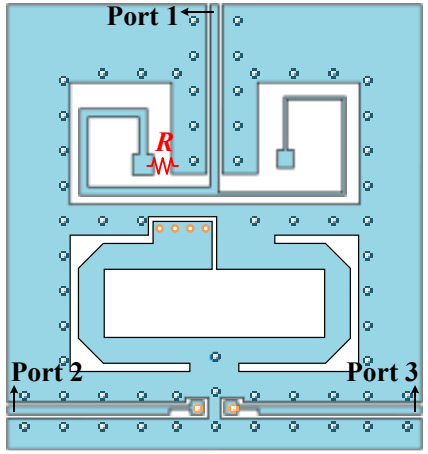
- **Input-reflectionless balun using stacked-coupled microstrip line**
  - Adjust the bandwidth and center frequency of the proposed reflectionless and balun circuits simultaneously
  - Cascade these two circuits

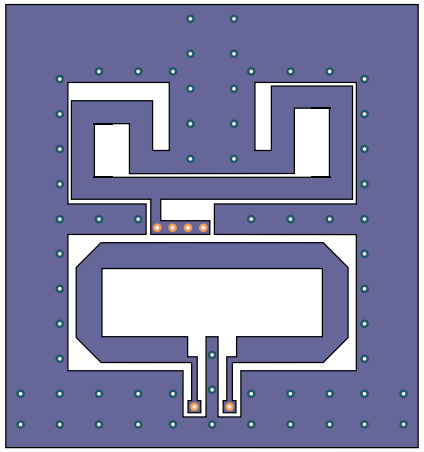
Reflectionless circuit

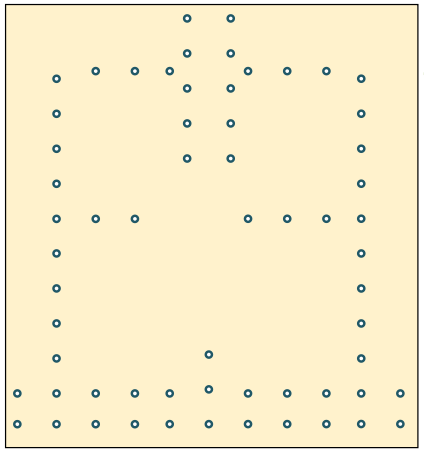


Balun circuit









NR operating band	Uplink (UL) operating band BS receive / UE transmit $F_{UL,low}$ - $F_{UL,high}$	Downlink (DL) operating band BS transmit / UE receive $F_{DL,low}$ - $F_{DL,high}$
n7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz
n38	2570 MHz – 2620 MHz	2570 MHz – 2620 MHz
n41	2496 MHz – 2690 MHz	2496 MHz – 2690 MHz
N48	3550 MHz – 3700 MHz	3550 MHz – 3700 MHz
n78	3300 MHz – 3800 MHz	3300 MHz – 3800 MHz

Comparison With State-of-the-Arts

- **Comparison table**

Ref.	MWCL	EuMC2019	TMTT	**This Work**
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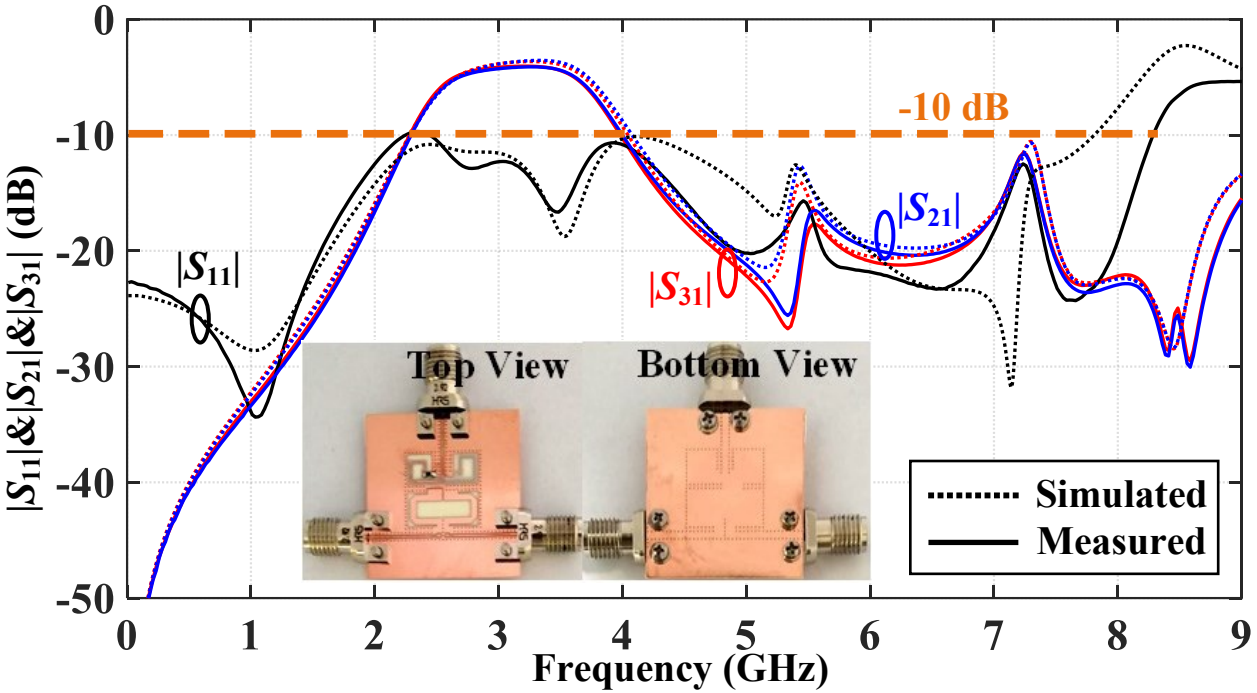
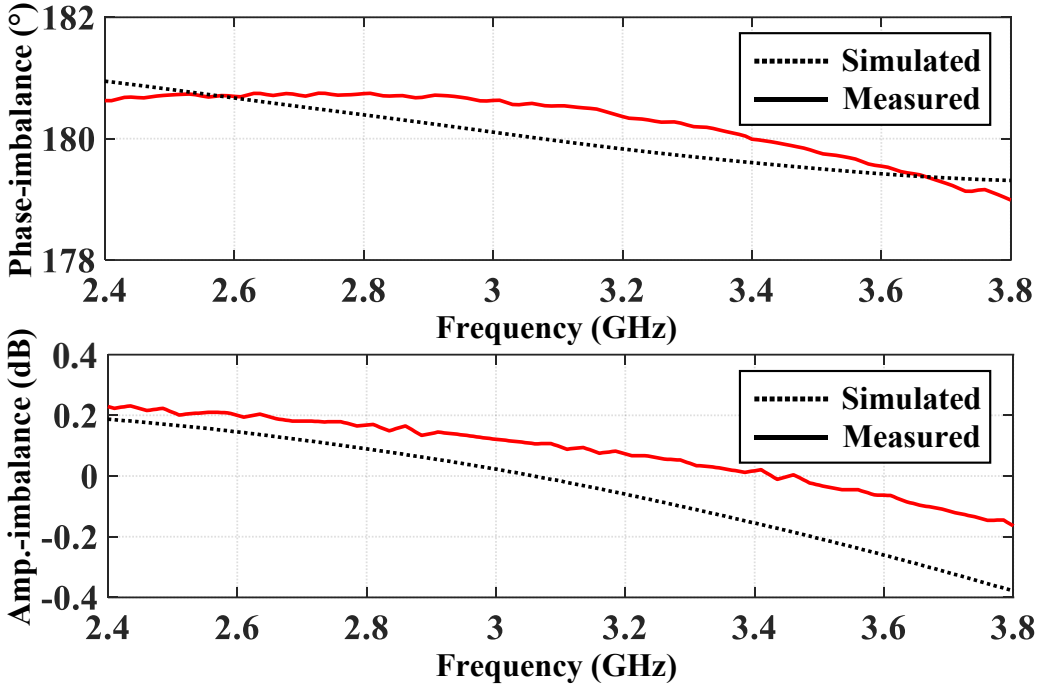
*: Insertion loss. **: Amplitude-Imbalance/Phase-Imbalance.

Measurements

- ***S*-parameters**
- ✓ Operation band: 2.4-3.8 GHz
- ✓ Reflectionless level: −10 dB (DC-8.2 GHz)



- **Phase/amplitude imbalance**
- ✓ Phase imbalance ≤ 1°
- ✓ Amplitude imbalance ≤ 0.22 dB



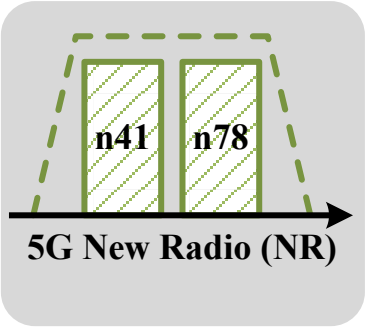
Conclusion

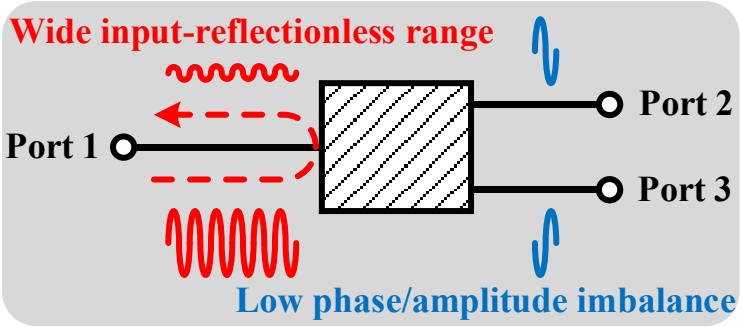
- **Feature**

✓ Wide passband

✓ Wide input-reflectionless range

✓ Low phase/amplitude imbalance





- **Next step**

Expand reflectionless range and achieve three-port reflectionless balun