A Thru-Reflect-Series-Resistance (TRS) Calibration for Cryogenic Device Characterization in 40-nm CMOS Technology

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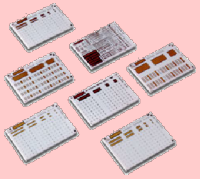
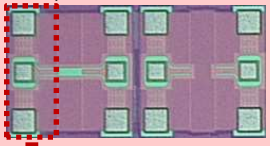
Motivation

Conventional VNA Calibration for Device Characterization

1. Probe Tip Calibration with ISS



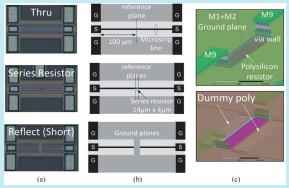
2. On-chip De-embedding



Lumped model approximation

- ✓ Standard operation procedure for on-chip device characterization requires multiple steps of calibration. The accuracy depends on the model of calibration structures and probing precision
- ✓ Our goal is to develop a technique that can simplify the calibration procedure for on-chip device characterization at improved accuracy

Thru-Reflect-Rs (TRS) Calibration



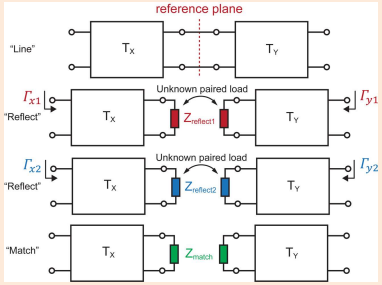
Components needed for Thru-Reflect-Series-Resistance Calibration

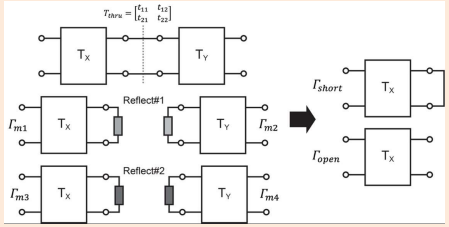
Lakeshore CRX-4K cryogenic probe station

- ✓ Summary of Thru-Reflect-Series-Resistance Calibration
  - ➢ Implemented in TSMC 40-nm CMOS technology
  - ➢ Requiring only three calibration structures
  - ➢ Can be applied at cryogenic temperatures (4K)

Calibration Flow

Review of LRRM Calibration

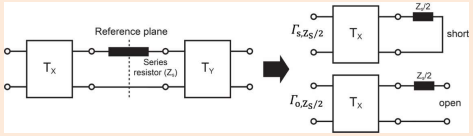




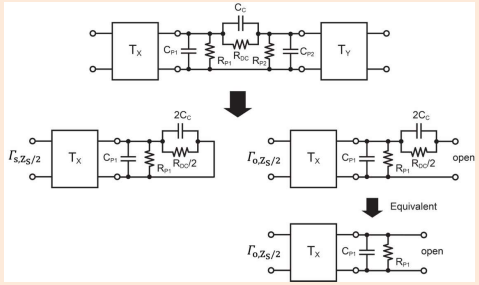
The implication from the LRRM calibration

- ✓ Line-Reflect-Reflect-Match Calibration Technique
  - ➢ Using four standards to accomplish the two-port cal.
  - ➢ Specifically, identical but unknown "reflect" loads are utilized as the calibration standards. This mitigates the need for accurate standard models.
  - ➢ Importantly, it only needs to know the model for the "match" load (generally close to 50ohm).
  - ➢ The "error box" is mainly dependent by the "Line" standard. It can be a "zero-length thru" or any "reciprocal elements".

Proposed TRS Calibration



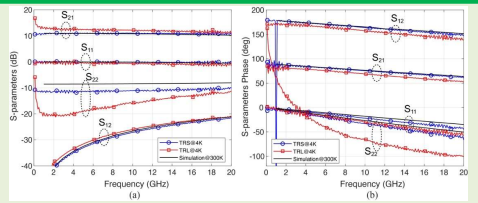
Employing "series-resistor" at the new "thru" leads to two new "load" measurements



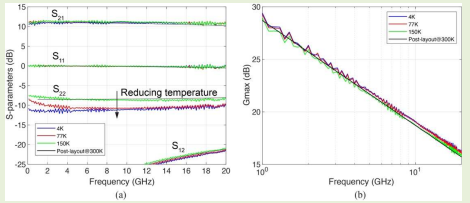
The equivalent lumped models of series-resistor structure and its circuit implication to complete the calibrations

- ✓ Thru-Reflect-Series-Resistance Calibration Technique
  - ➢ Using single-sided probing to create the two "Rs" and to reduce the # of calibration structures to three.
  - ➢ Algorithm is similar to LRRM calibration but we use series polyresistor in the "Line" of LRRM.
  - ➢ DC resistance of polyresistor is used as a frequency-independent "load" model.
  - ➢ The high-frequency effect from terminal parastics are removed by "correlated" double sampling technique.

Experimental Results



The measured 40-nm NMOS DUT S-parameters using different calibrations. (a) Magnitude. (b) Phase



(a) The measured NMOS DUT S-parameters and (b) GMAX at different temperatures

PROPOSED CONCEPT GOALS

Thru-Reflect-Series-Resistance Calibration featuring:

- ✓ Simpler and more accurate calibration scheme
- ✓ No impedance conversion and bandwidth limitation suffered from TRL calibration
- ✓ Requiring only three calibration structures to reduce unwanted probing error
- ✓ Measured at cryogenic temperatures (4K) to create DC/RF models for cryo-CMOS applications.