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A Low-Loss High-Speed SIW Cavity SPDT Switch Architecture

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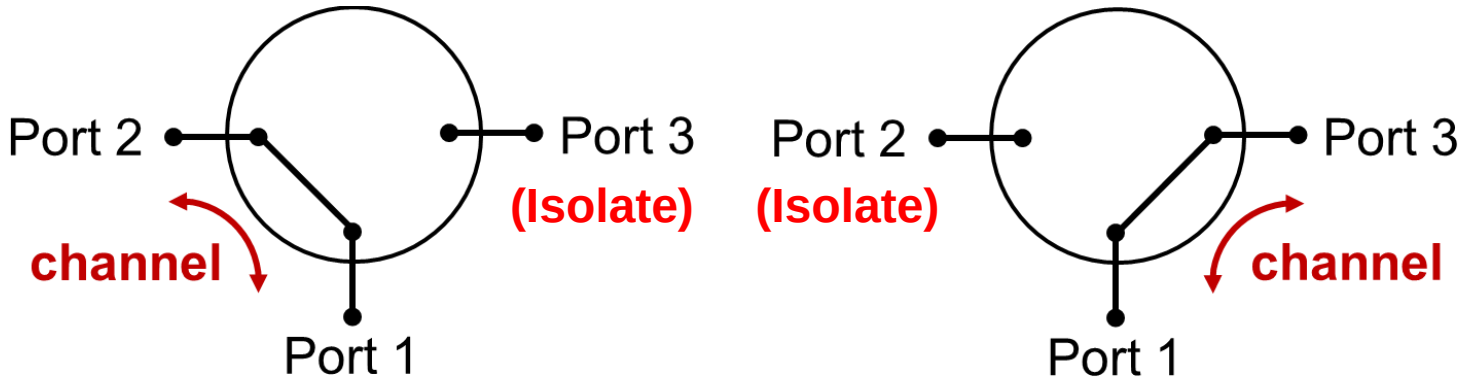
SPDT Switch Concept

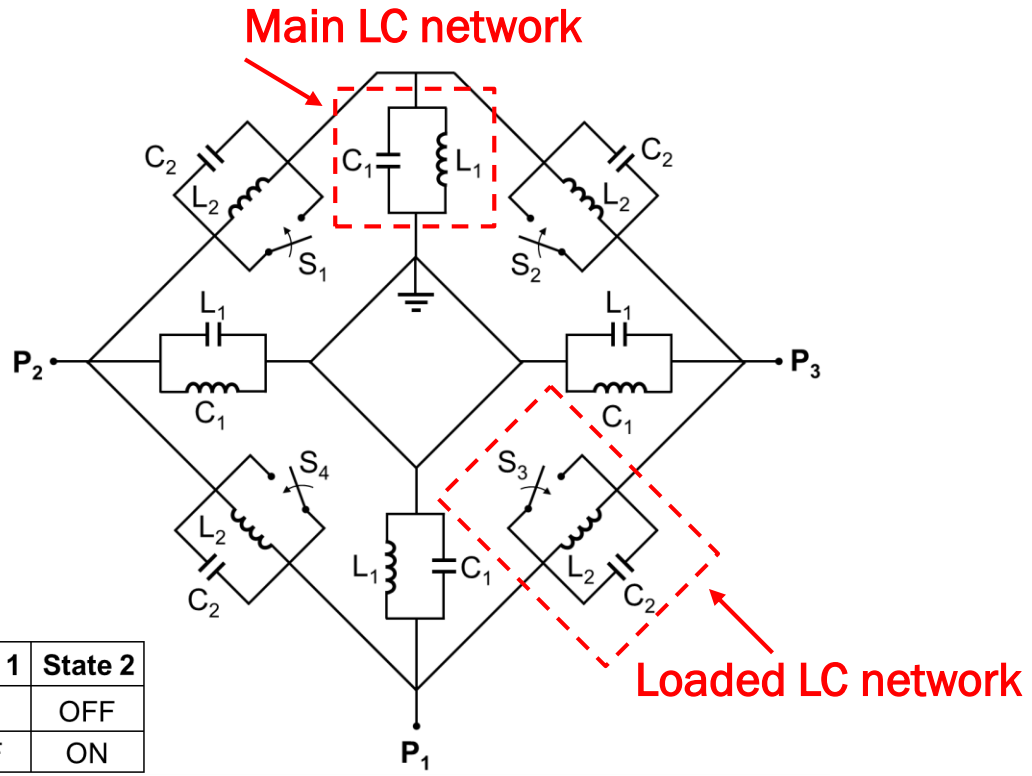
- Considering port 1 as the input port, the power flow can be switched between the output ports (port 2 and 3).



The architecture of a traditional SPDT switch.
(a) State 1. (b) State 2.

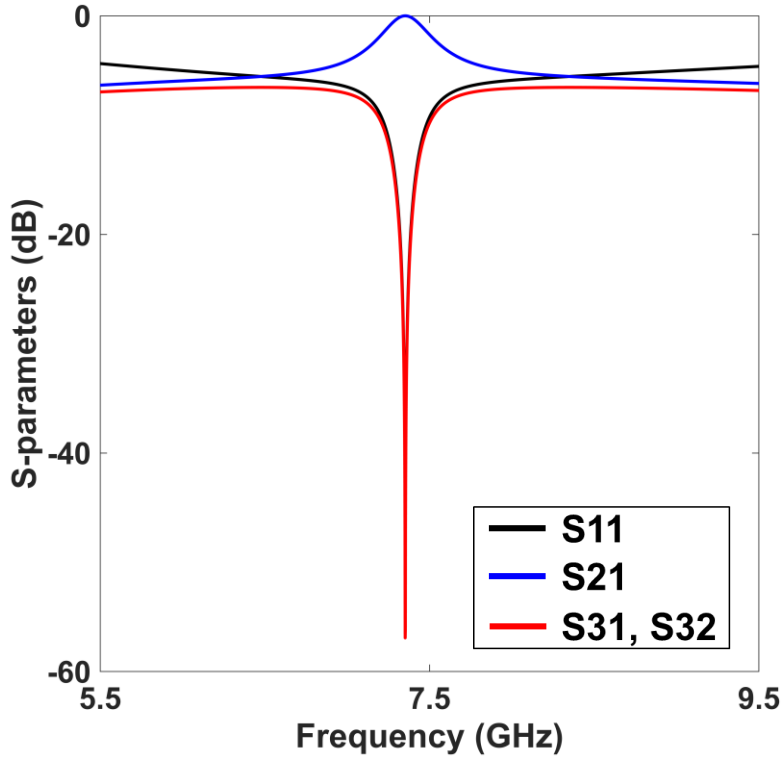
Proposed Circuit Model

- By controlling the states of the switches (ON and OFF), the states of the SPDT switching structure are defined.



	State 1	State 2
$S_{2,4}$	ON	OFF
$S_{1,3}$	OFF	ON

The equivalent circuit of the proposed SPDT switch.



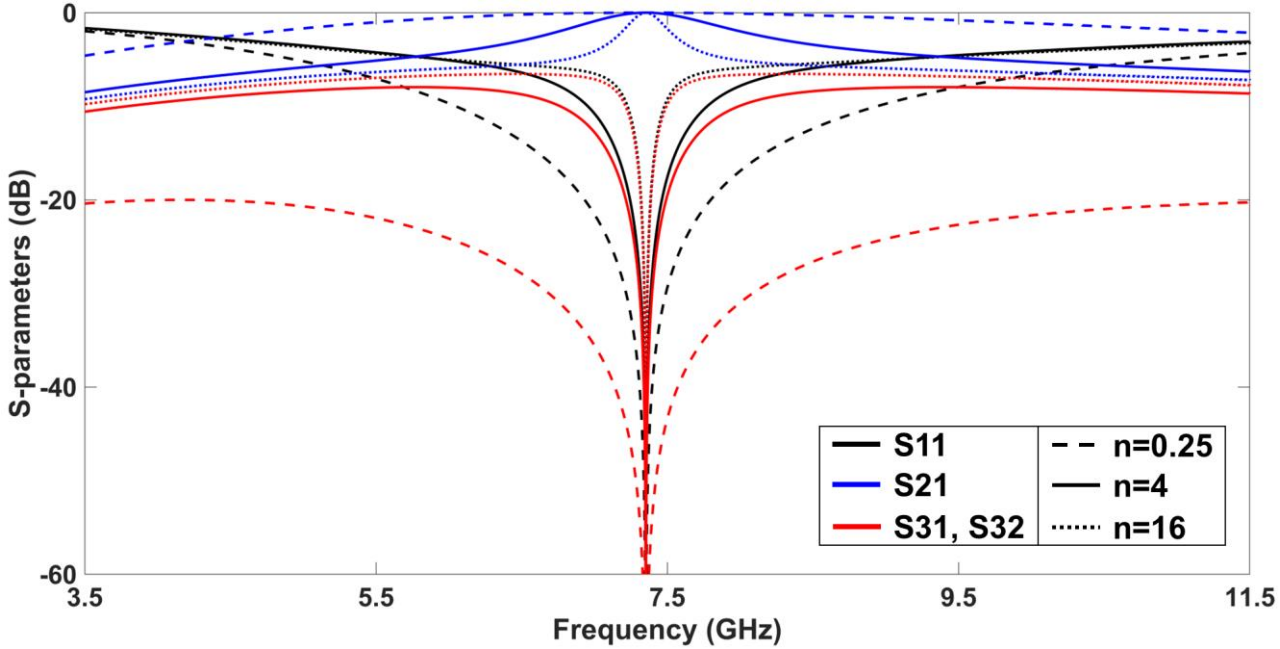
Circuit simulation of state 1 of the proposed SPDT switch.

Proposed Circuit Model

- The resonant frequency of the SDPT is determent by the main LC network (L_1 & C_1)
- The isolation happens by choosing the values of the lumped elements of the loaded parallel LC network to be a multiple factor of the main LC network as follows:

$$C_2 = nC_1 \qquad \& \qquad L_2 = L_1/n$$

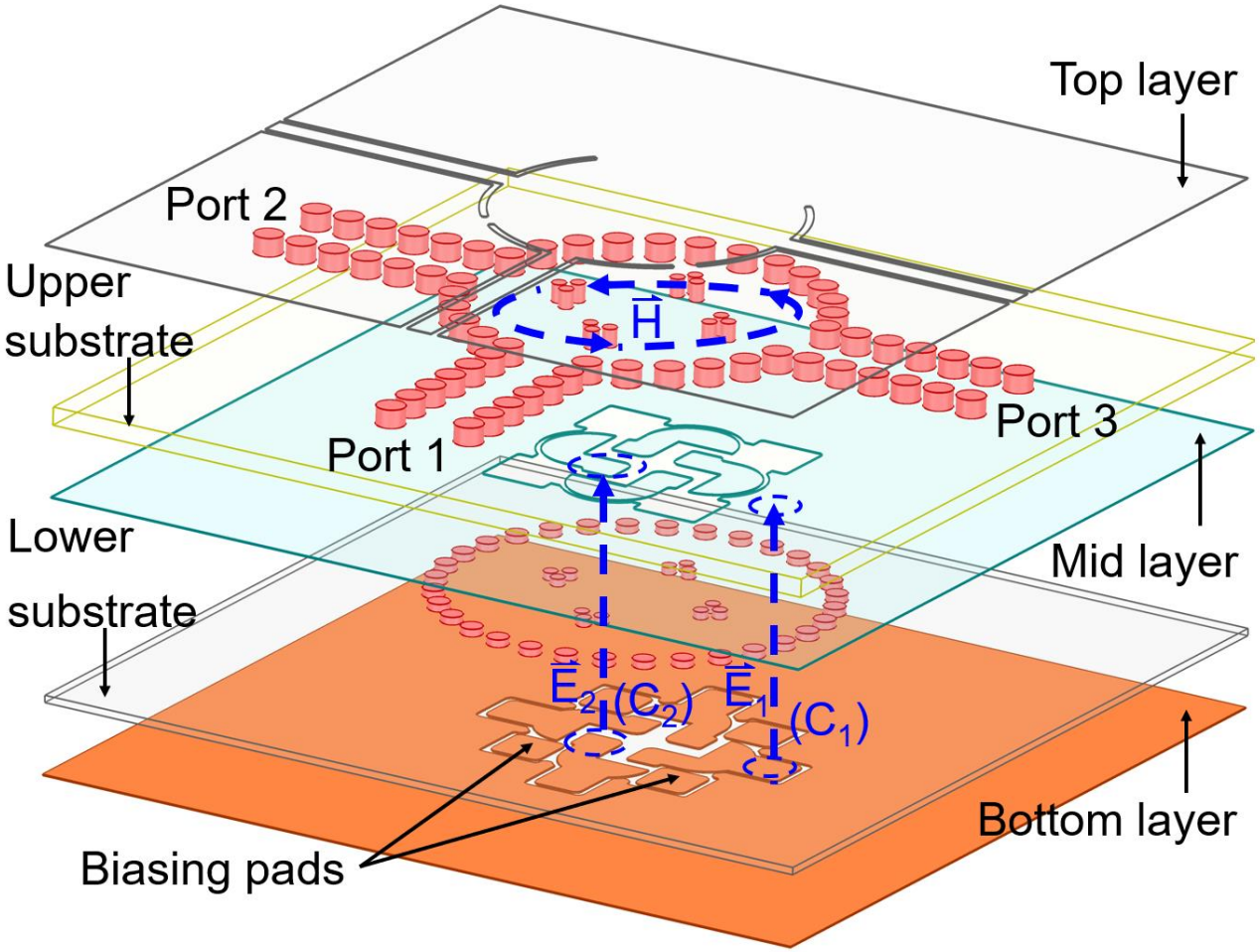
- Controlling the value of the factor (n), the isolation bandwidth of the SPDT switch is tuned.



The impact of the factor (n) on the S-parameters of the proposed SPDT switching circuit (state 1).

SPDT Switch EM Design

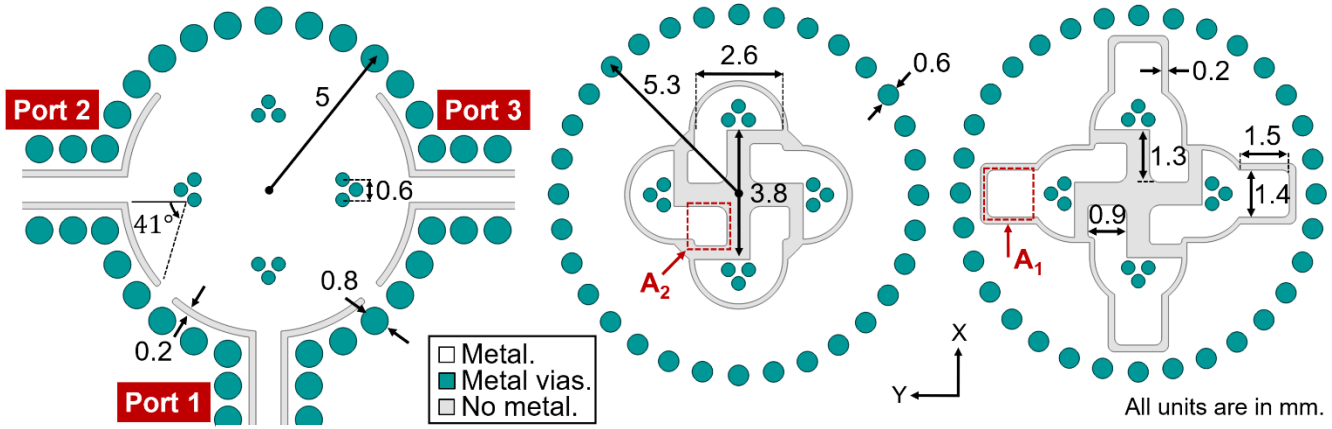
- The proposed SIW-SPDT switch consists of two vertically-aligned substrates with three layers of copper.
- The upper substrate hosts the main evanescent-mode circular SIW cavity resonator in which the magnetic field is confined.
- Four capacitive posts are centered in the cavity with three metal vias drilled in each post.



A 3D structure of the proposed SIW-SPDT switch showing two substrates and three layers of copper.

SPDT Switch EM Design

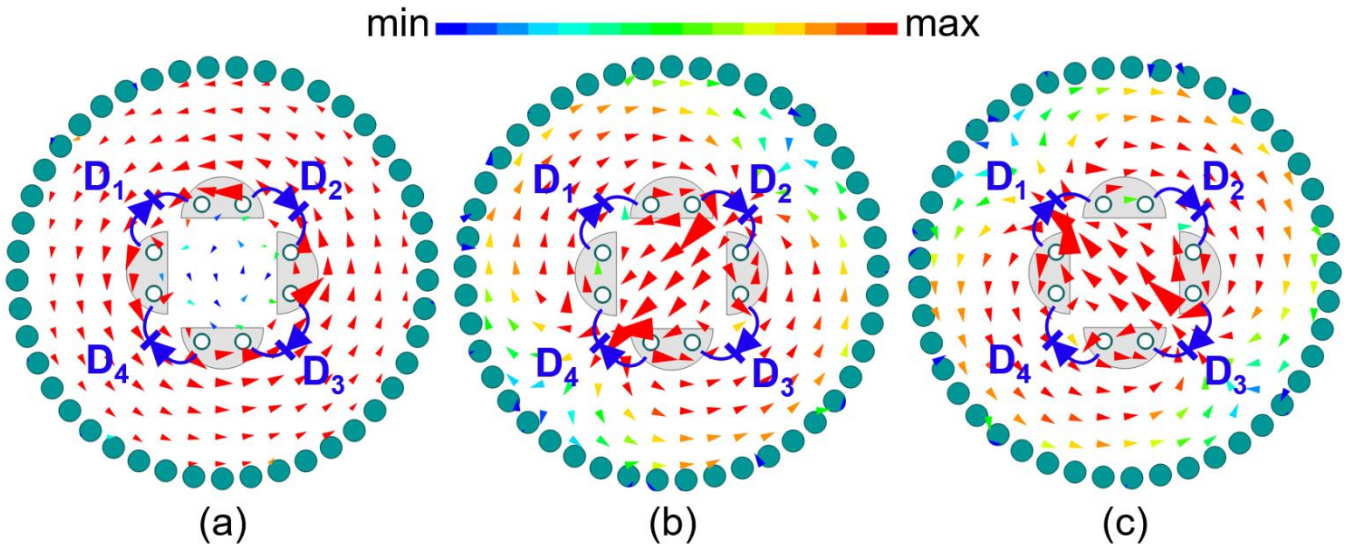
- Using a four-post evanescent mode cavity resonator allows the generation of three modes.
- Loading capacitances are created in the lower substrate in which the electric field exists.
- Each post is designed with two metalized areas (A_1) and (A_2).
- (A_1) creates a capacitance (C_1) between each post and the ground that affects the resonant frequencies of all modes.
- The area (A_2) creates a capacitance (C_2) between adjacent posts. This capacitance dictates only the resonant frequency of modes II and III.



The structure of the proposed SIW-SPDT switch with detailed dimensions. (a) Top layer. (b) Middle layer. (c) Bottom layer.

SPDT Switch EM Design

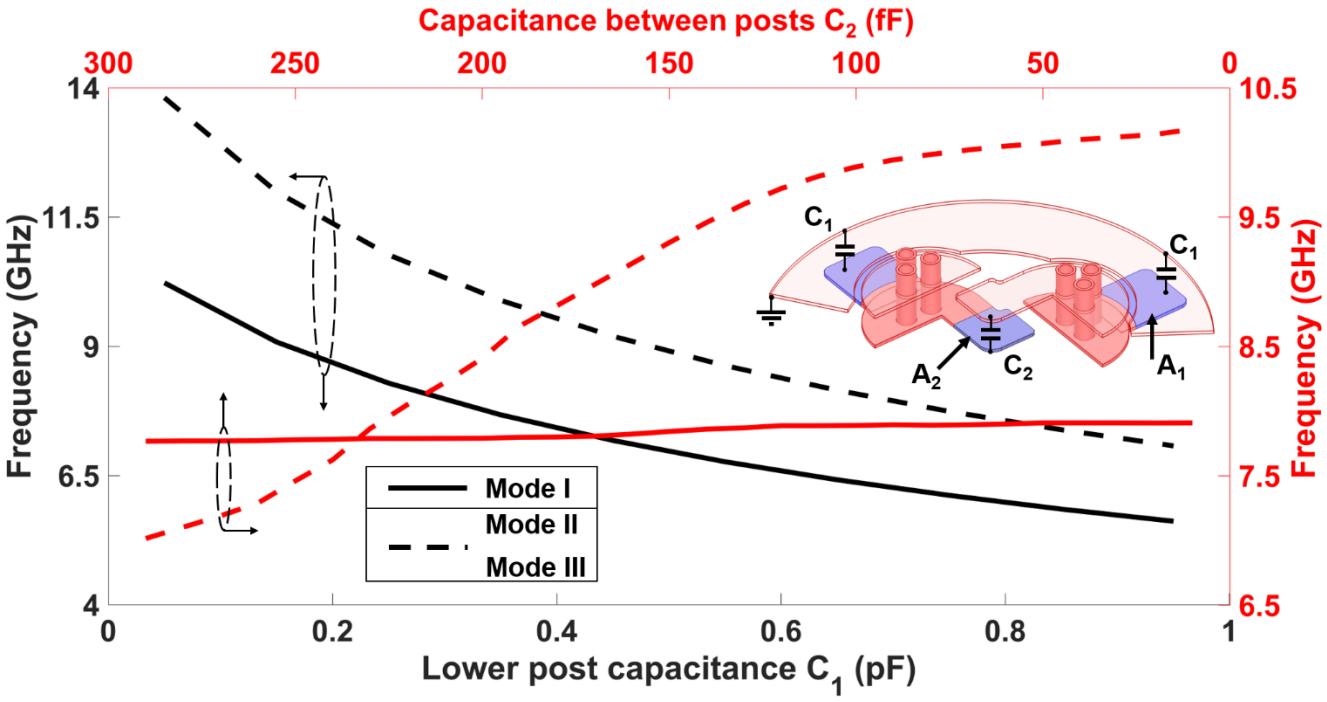
- Mode I is the main mode while modes II and III are higher-order modes having the same resonant frequency.
- Four pairs of PIN-diodes are used. Each pair is connected in a back-to-back configuration, named as (D_n) where (n = 1, 2, 3, 4) and located between each two adjacent posts.
- Mode I only exists in the area outside the posts and circulates in one direction.
- Modes II and III are differential modes that rotate around the connected posts.



In the upper substrate, (a) The magnetic field behavior of Mode I. (b) The magnetic field behavior of Mode II (D1 and D3 are ON while D2 and D4 are OFF). (c) Magnetic field behavior of Mode III (D2 and D4 are ON while D1 and D3 are OFF).

SPDT Switch EM Design

- The areas (A_1) and (A_2) represent the loading capacitance for resonance modes.
- The capacitance (C_1) affects all modes, while (C_2) only changes Modes II and III.
- The resonant frequencies of the modes are aligned by controlling the value of (C_1) by adjusting area (A_1).
- The capacitance (C_2) is used to align the operating frequency of modes II and III on mode I.



The variation of the resonant frequency of mode I, II and mode III with imposed capacitances (C1) and (C2).

SPDT Switch EM Design

- The insertion loss of the switch is better than 2 dB even at a diode resistance of 11 Ohms.

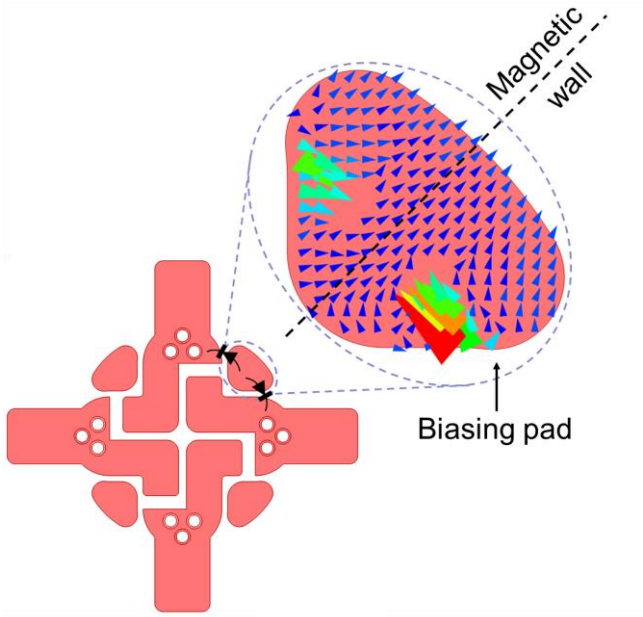
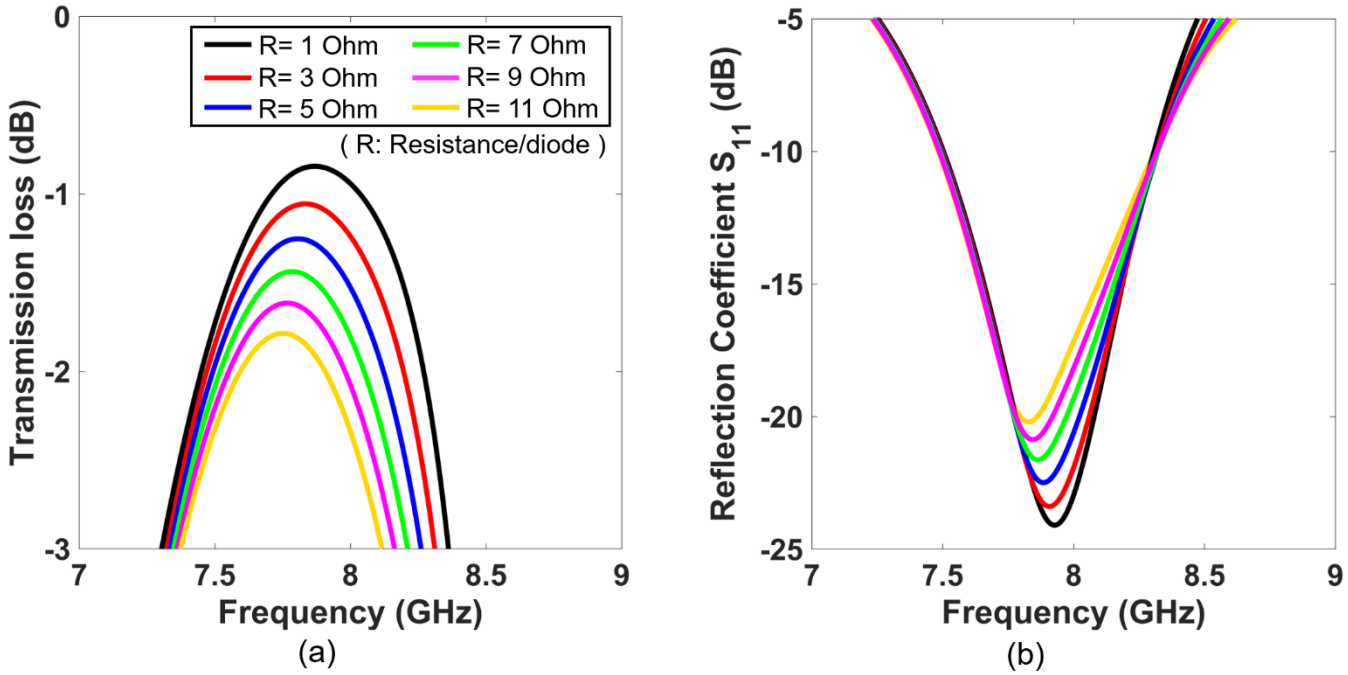


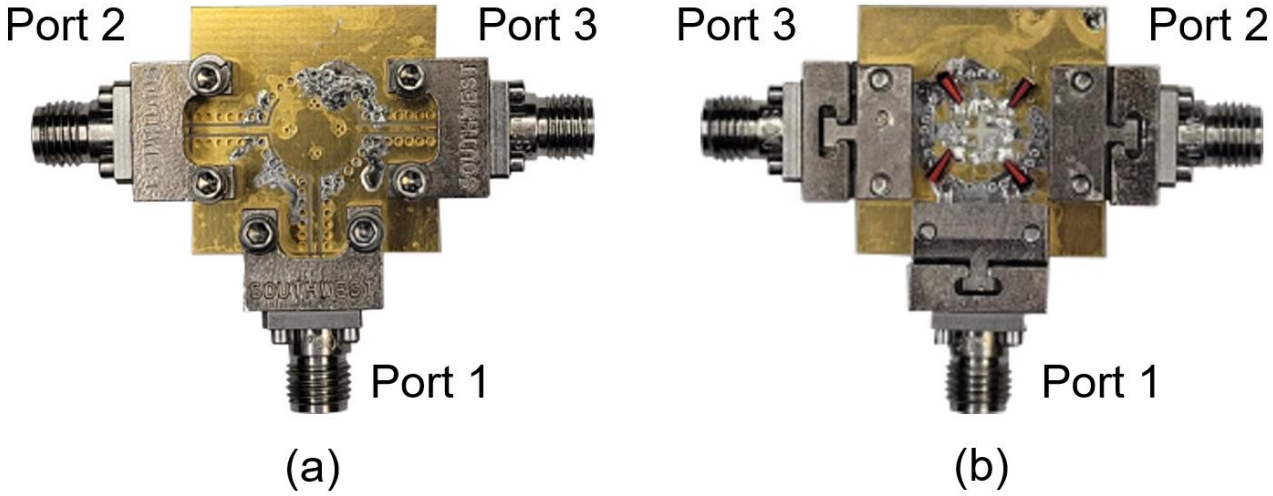
Fig. 9. A magnified view of the biasing pad showing a magnetic wall (o.c.) boundary condition.



Simulated S parameters of one state of the proposed SIW-SPDT switch with different values of PIN diodes equivalent resistances, (a) transmission coefficient (b) reflection coefficient.

SPDT Switch Implementation

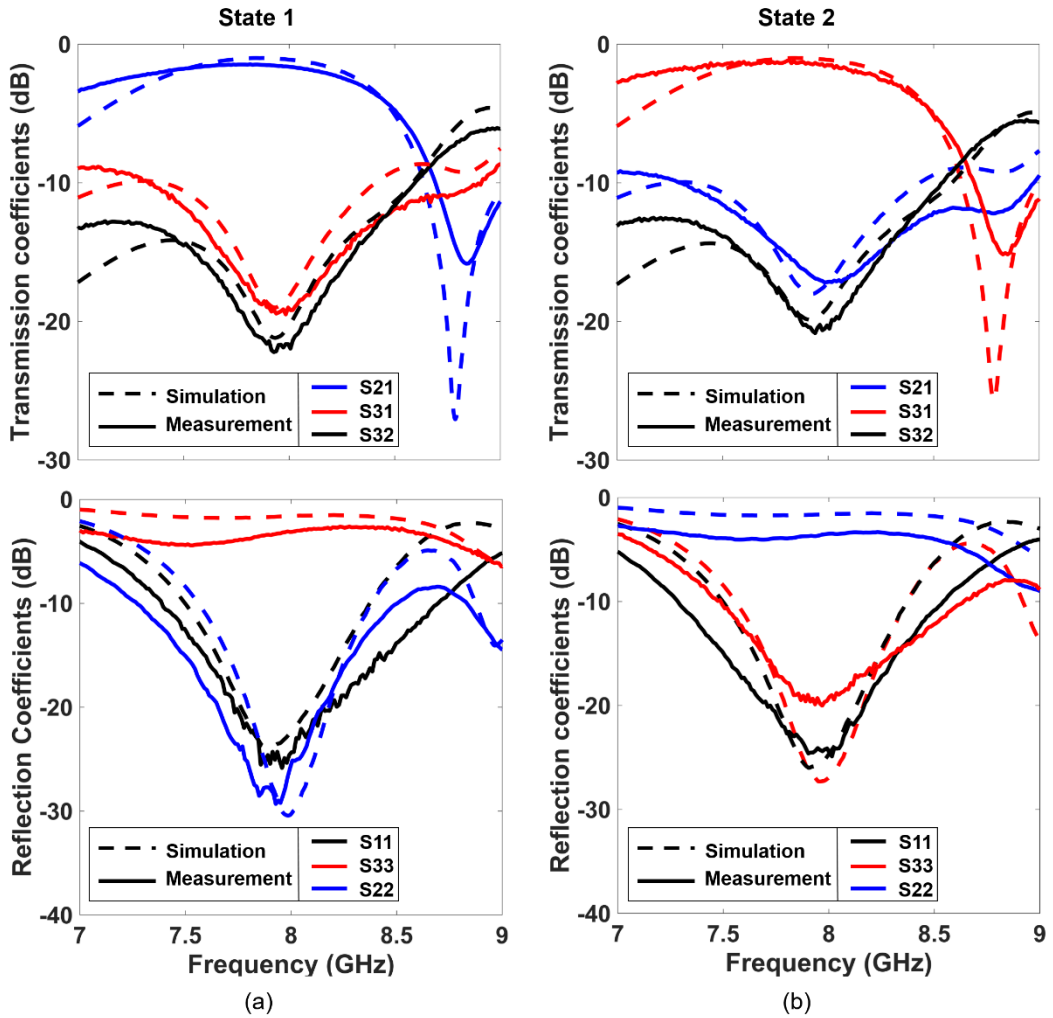
- The proposed SIW-SPDT switch is fabricated with RO4003C substrates with 20 and 8 mils thicknesses for the upper and lower substrates.
- The proposed SIW-SPDT cavity has a size of (11 mm × 11 mm) excluding the feeding lines.
- Four pairs of high switching speed PIN-diodes (DSM8100-000 Skyworks Mesa Beam-Lead) are used.



Photograph of the fabricated SIW-SPDT switch. (a) Top view. (b) Bottom view. (Bias details are removed for clarity).

SPDT Switch Results

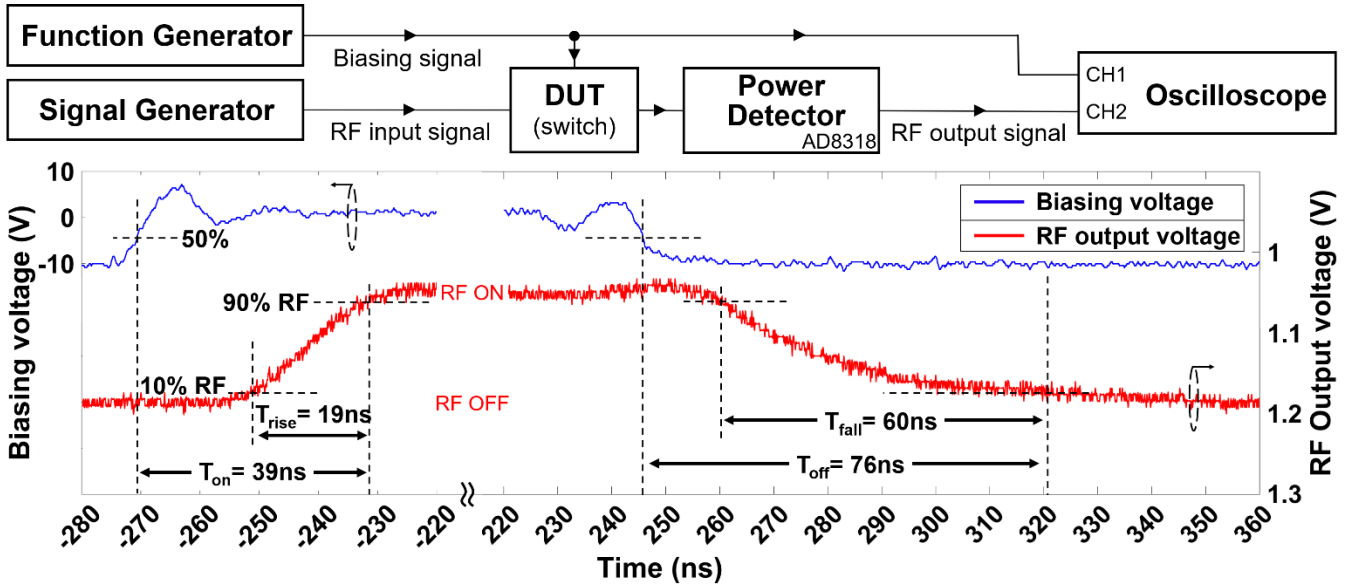
- For both states, the switch is well-matched with reflection coefficients better than 24.5 dB and 25.5 dB at the input and the output ports, respectively.
- The isolated port remains unmatched with a reflection coefficient of approximately 3 dB.
- The operating channel has a measured insertion loss better than 1.6 dB for both states.
- The measured isolation between the isolated port and the input port is 18 dB and between output ports is 22 dB.
- the switch has a measured 15 dB isolation bandwidth of 579 MHz.



Simulated and measured S-parameters of the proposed SPDT switch. (a) State 1. (b) State 2.

SPDT Switch Results

- The results show a high-speed switching performance.
- T_{on} and T_{off} are 39 ns and 76 ns respectively while T_{rise} and T_{fall} are 19 ns and 60 ns respectively.



Switching speed measurement results. (T_{on} → 50% control to 90% RF, T_{rise} → 10% to 90% RF, T_{off} → 50% control to 10% RF, T_{fall} → 90% to 10% RF).

Conclusion

- A novel low-loss SIW-SPDT switch with a resonant frequency of 8 GHz is presented.
- The switching concept relies on the constructive and destructive interference between the modes, selected by the PIN diodes.
- A low measured insertion loss of 1.6 dB is achieved, while the measured isolation is better than 18 dB.
- The switch shows a high switching speed that remains below 80 ns.