Th2G-2

A Multi-stage 19.2-dBm, 30.4%-PAE D-band Power Amplifier in a 250-nm InP HBT Process

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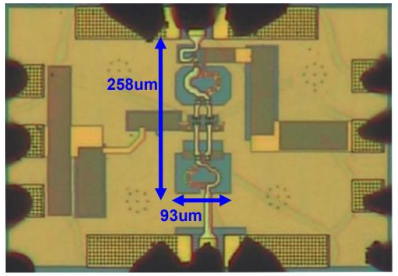
Overview

- Introduction
- Device cell design
- Circuit design
- Measurements and simulations
- Conclusion

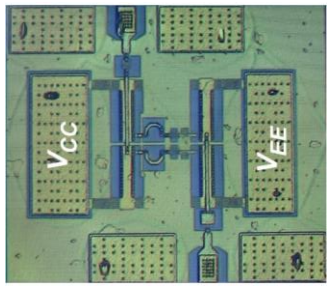
Motivation

- Several InP PAs demonstrate record efficiencies at D-band
- Highest efficiency PAs currently demonstrate single stage Pas
- This work demonstrates a multi-stage high-efficiency PA with 19.2 dBm Psat at 135 GHz



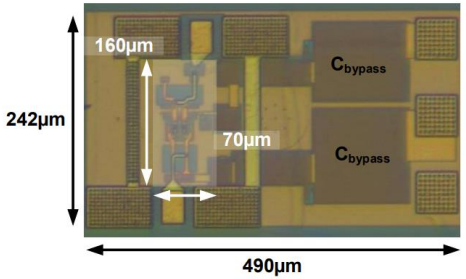
[J.Chien, IMS2022]

Freq	PAE
115 GHz	32.7%



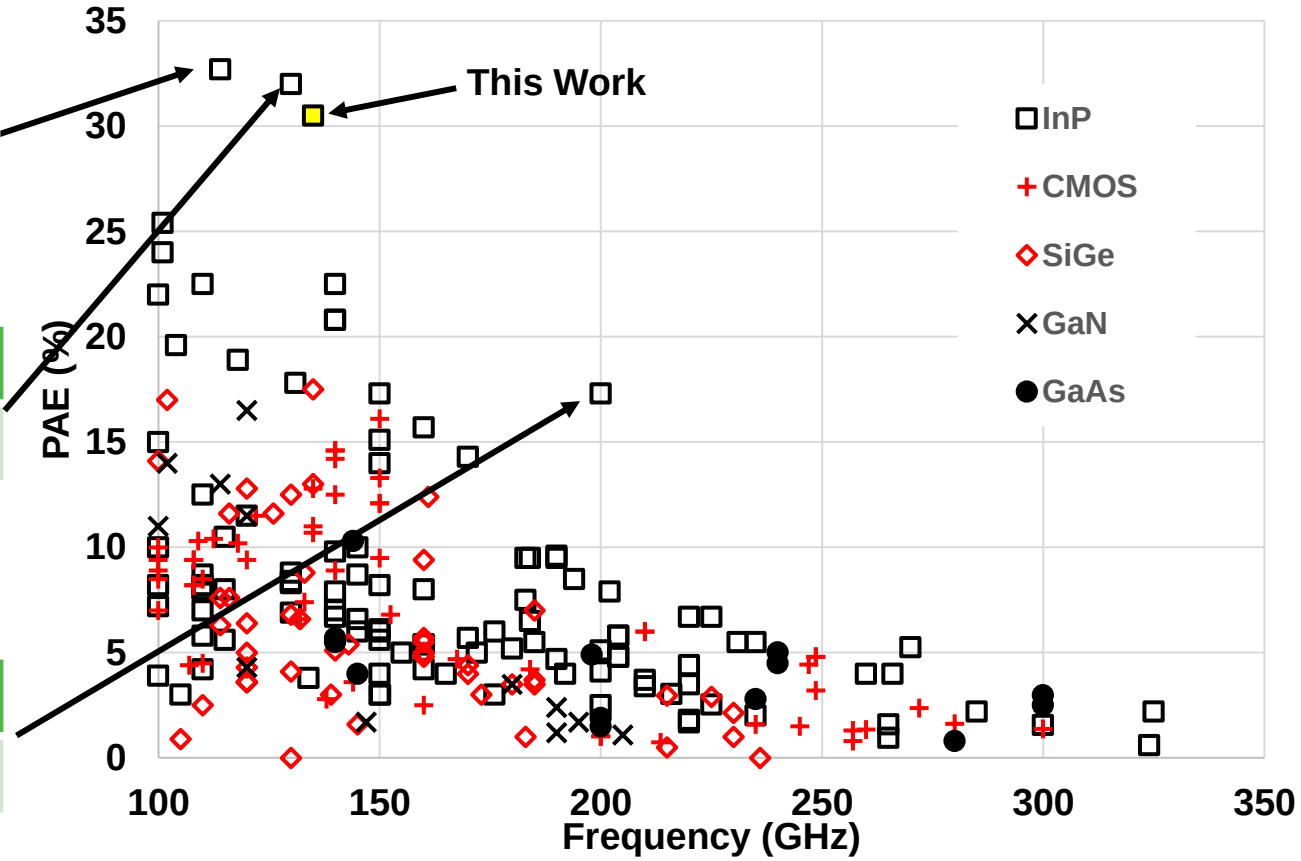
[K.Ning, RFIC2020]

Freq	PAE
130 GHz	32%



[J.Chien, BCICTS2023]

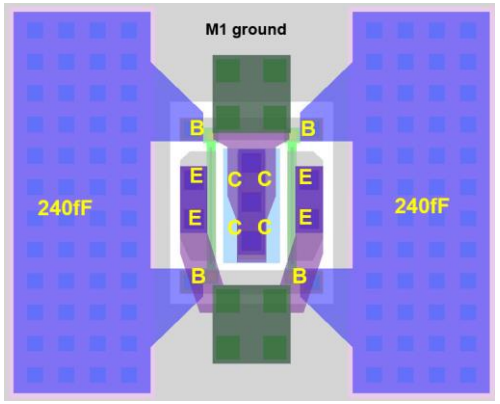
Freq	PAE
200 GHz	17.3%



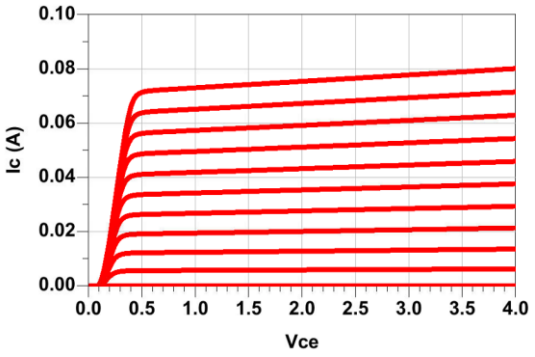
Teledyne 250-nm InP Technology

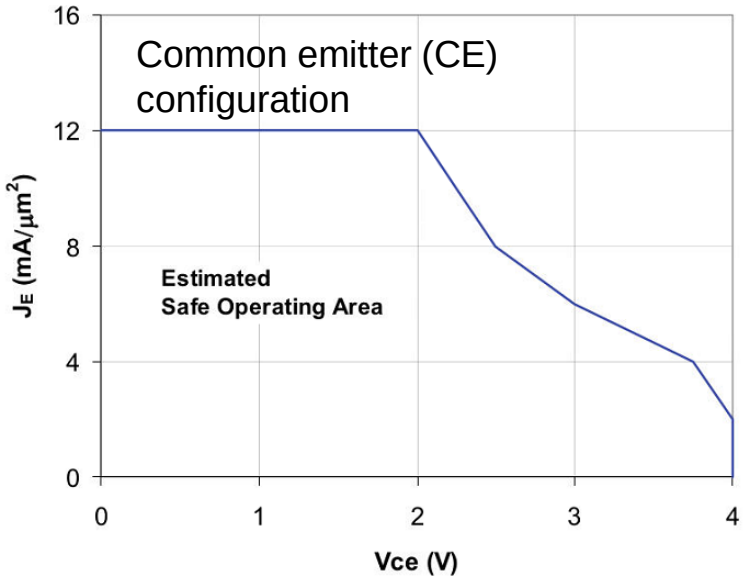
- Nominal fT/fmax of 370/650 GHz for 4 um emitter length, VCE=1.8 V, Je =2 mA/um

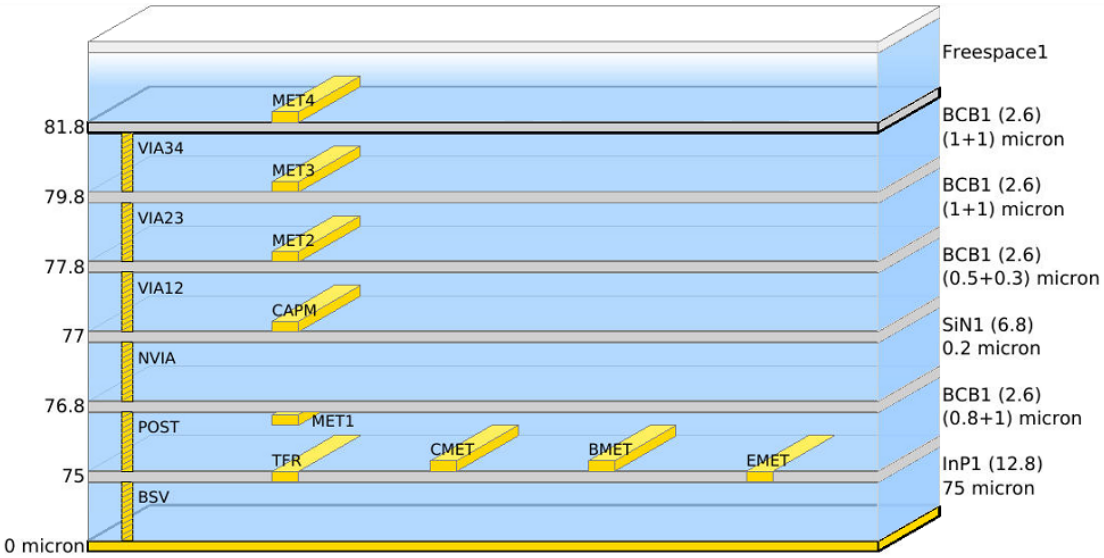
4x6 um common base (CB) Layout



f_{max}	Je,max	Typical Vce	Vknee	# metal (Au) layers
~600 GHz	3 mA/um	2.5 V	0.7 V	4

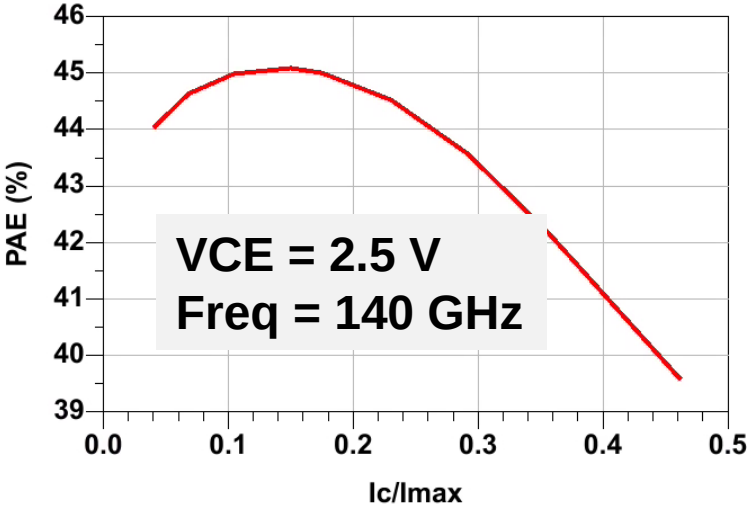


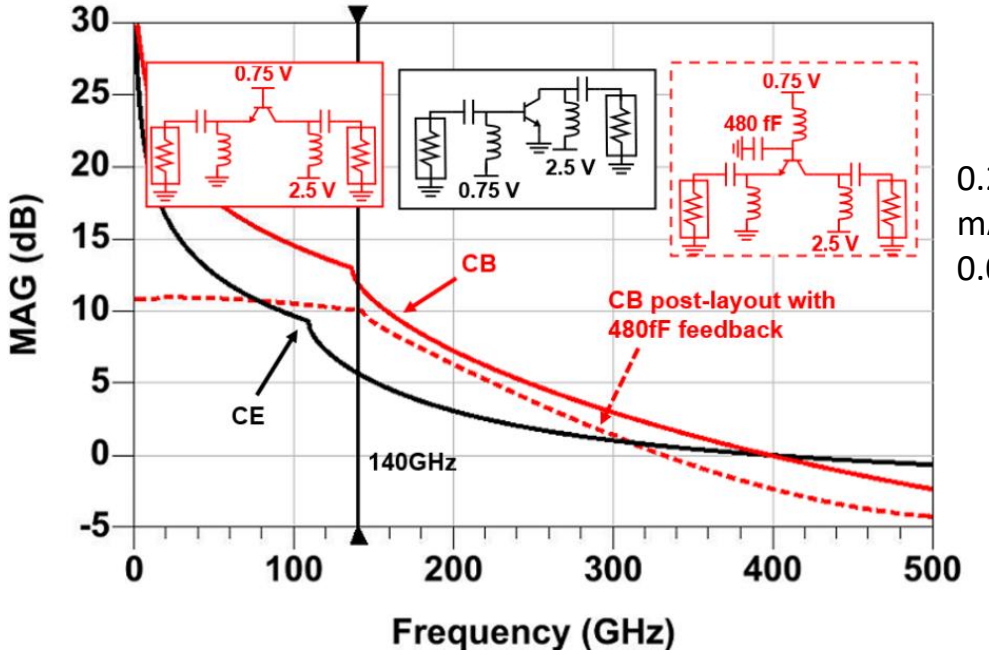




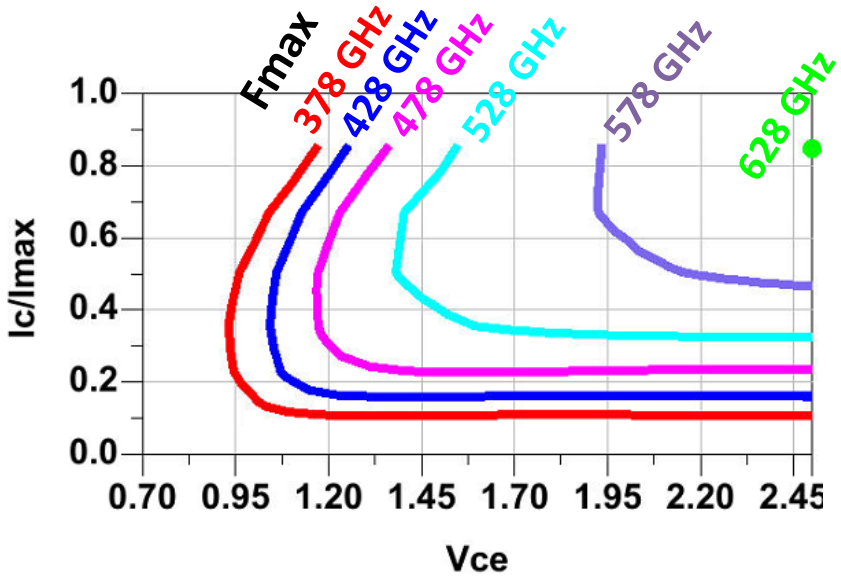
4x6um InP HBT Operating Bias

- Gain in a device can be controlled through operating bias, but there is a tradeoff with PAE
- Optimum PAE at 140 GHz is around 10% of Imax at 2.5 V which reduces our Fmax to about 350-400 GHz



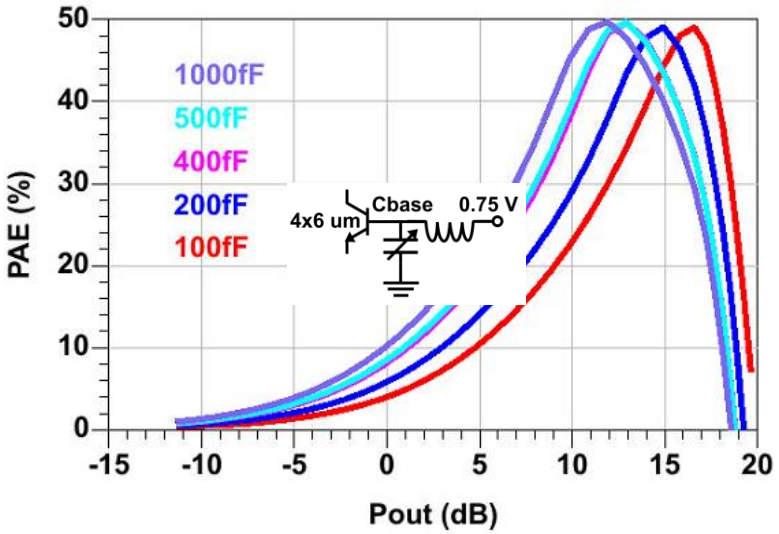


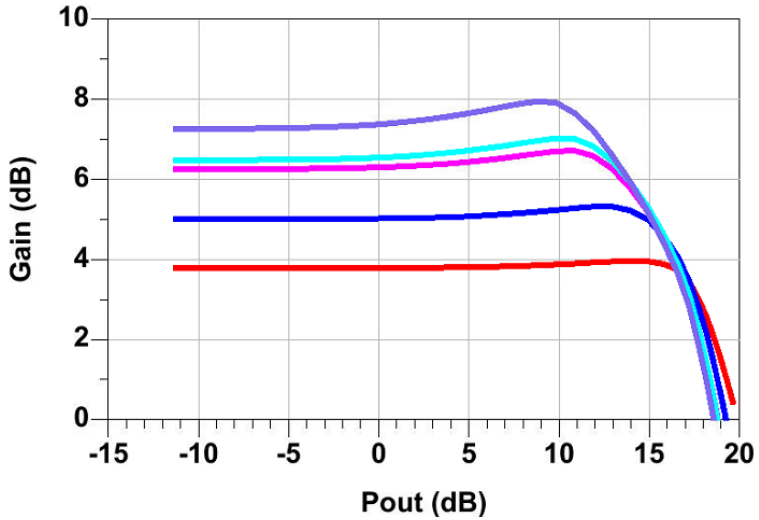
0.21 mA/um, 0.07*Imax

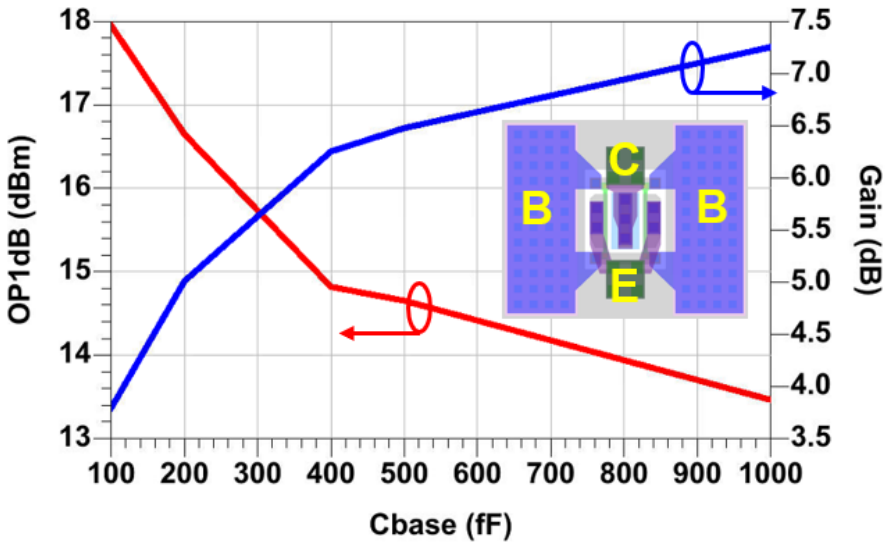


4x6um InP HBT Degeneration

- Gain can also be controlled through base degeneration, but we tradeoff with OP1dB
  - Higher shunt Cbase gives higher gain, but lower OP1dB
  - Similarly, lower shunt Cbase results in lower gain, but higher OP1dB
- Below we show plots for varying shunt base capacitance values
- PAE is invariant with assumption of lossless embedding and no harmonic tuning



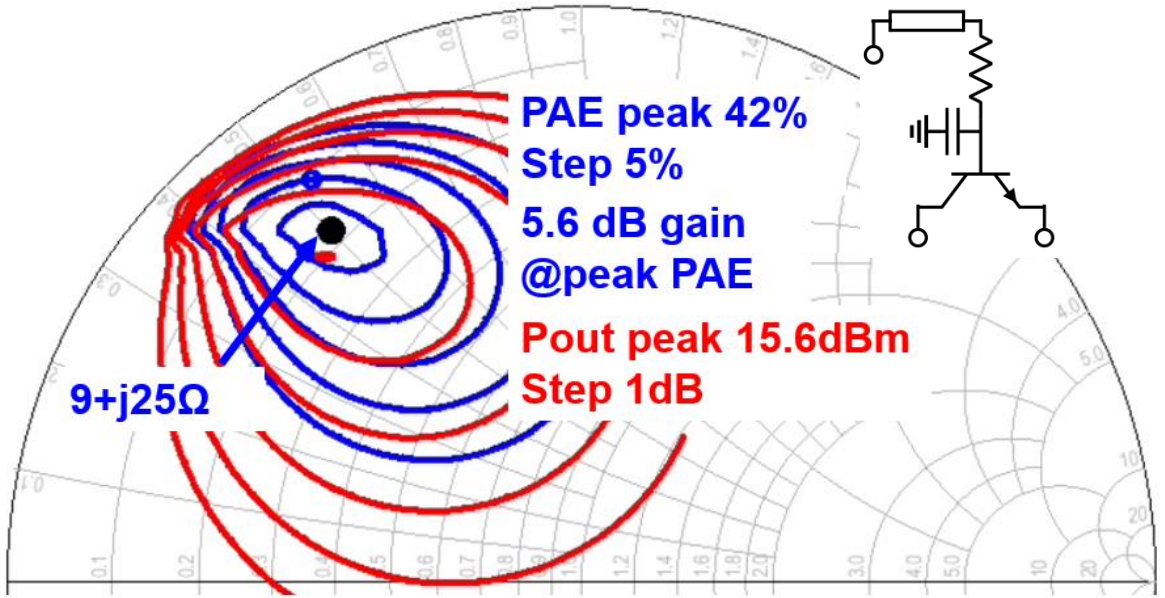




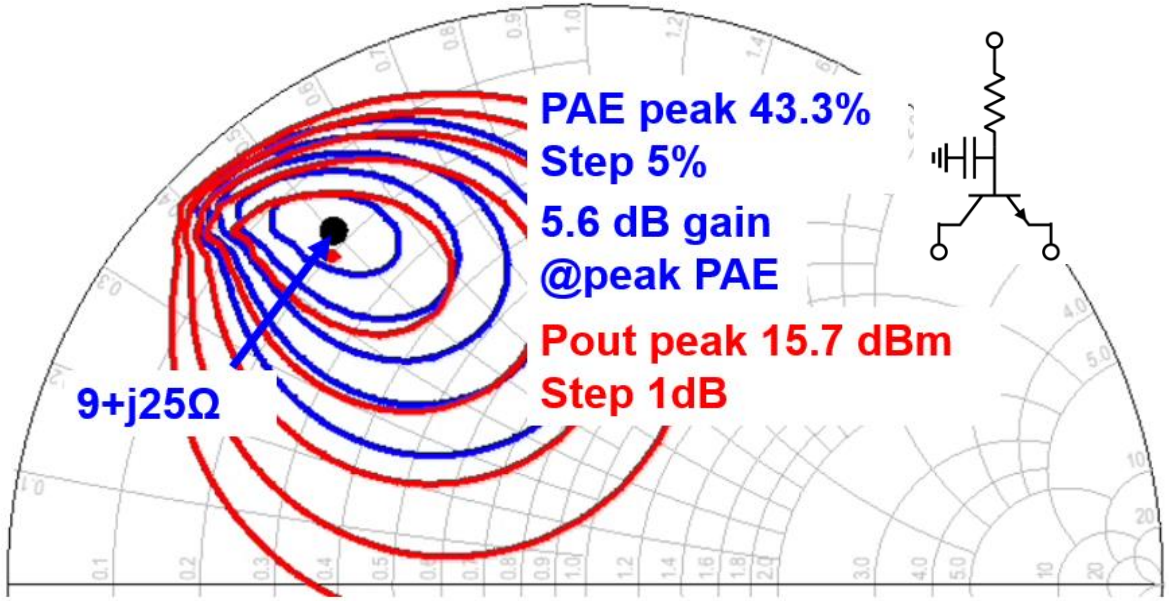
Device Loadpull

- Addition of a base resistor helps to
  - Reduce thermal runaway effects
  - Bias stabilization
  - Out of band RF stability
- Reduction in PAE due to real impedance presented at 140 GHz
  - Add a quarterwave line at the base

w/o base quarterwave line

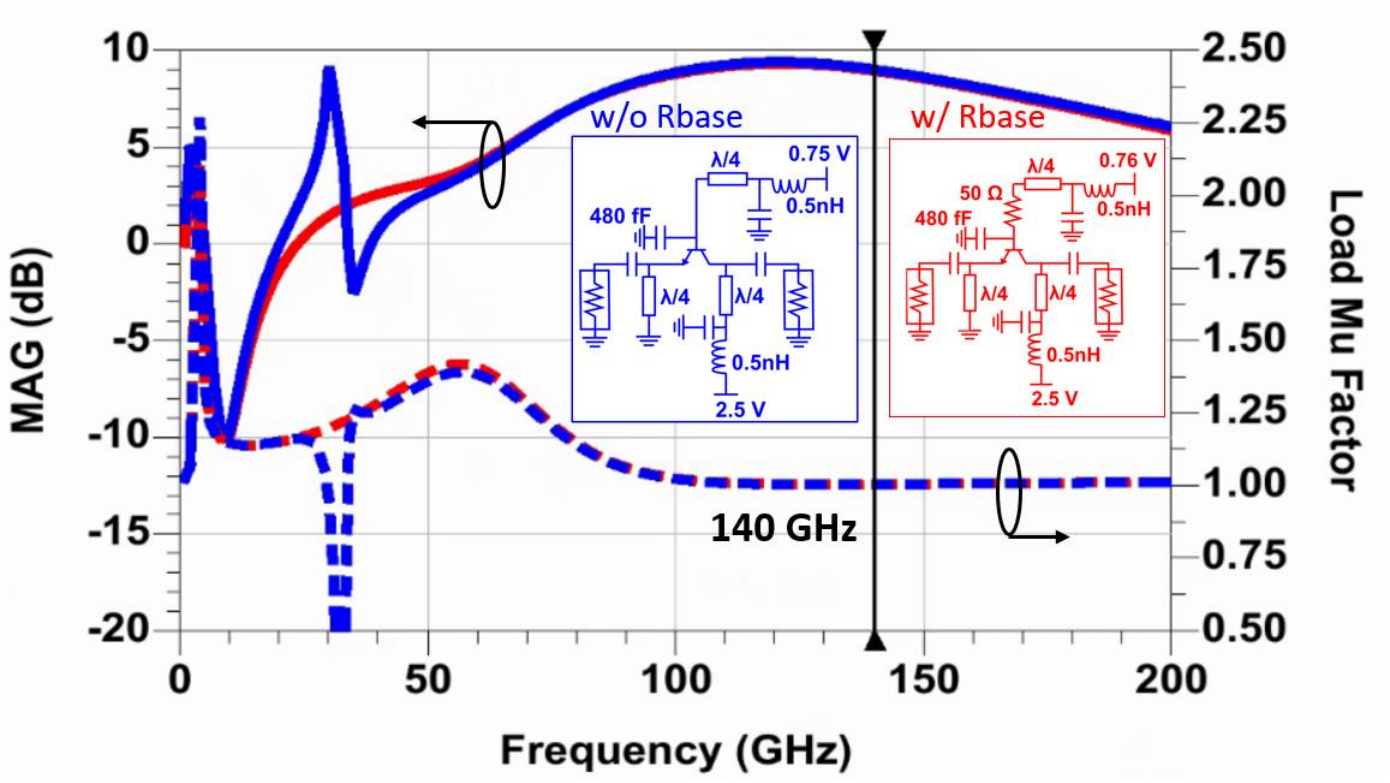


w/ base quarterwave line



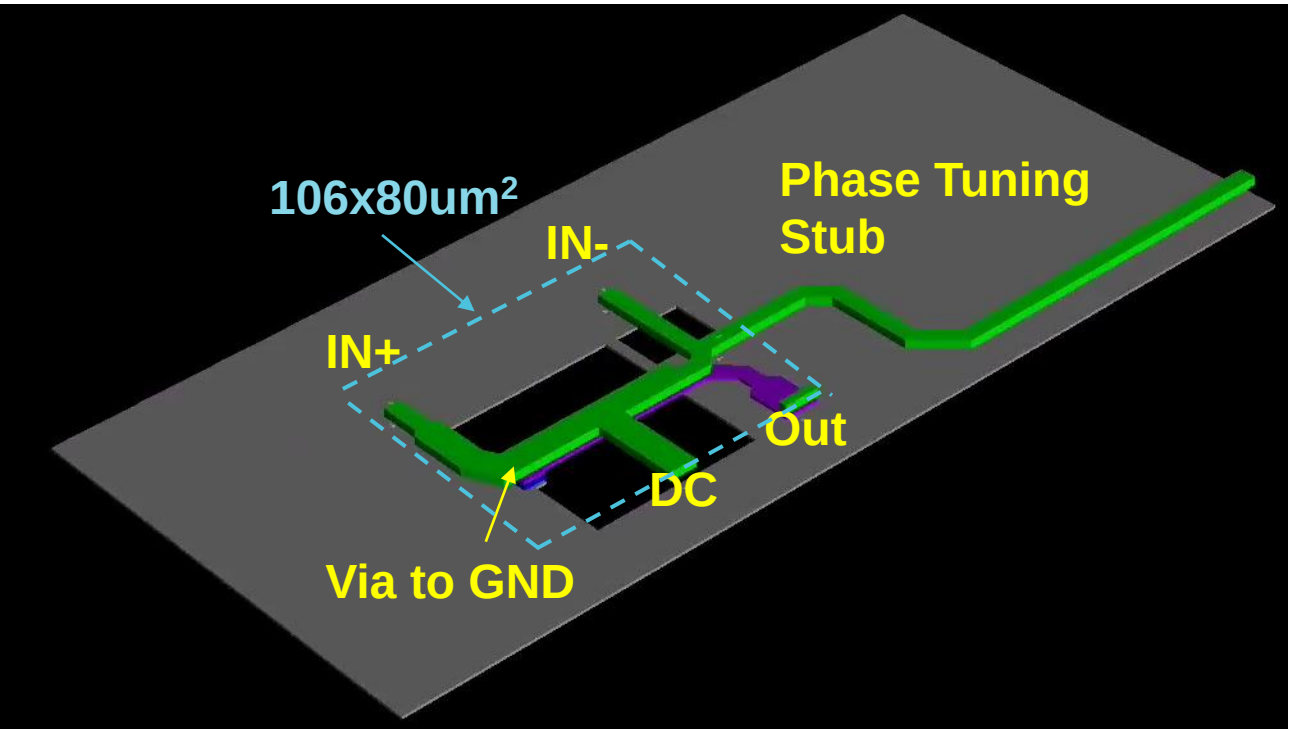
RF Device Stability

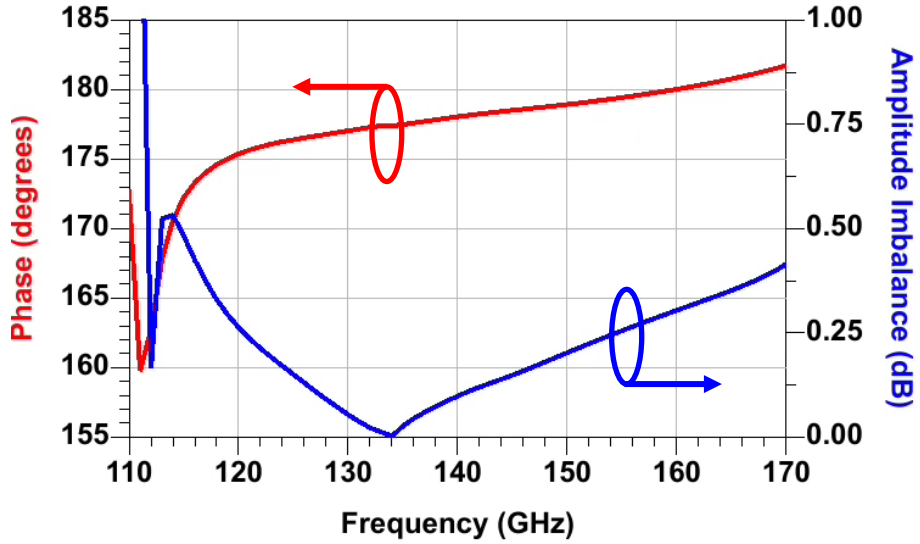
- Stability issues at ~30 GHz without addition of base resistance
- Assuming about 0.5 nH inductance from DC probes

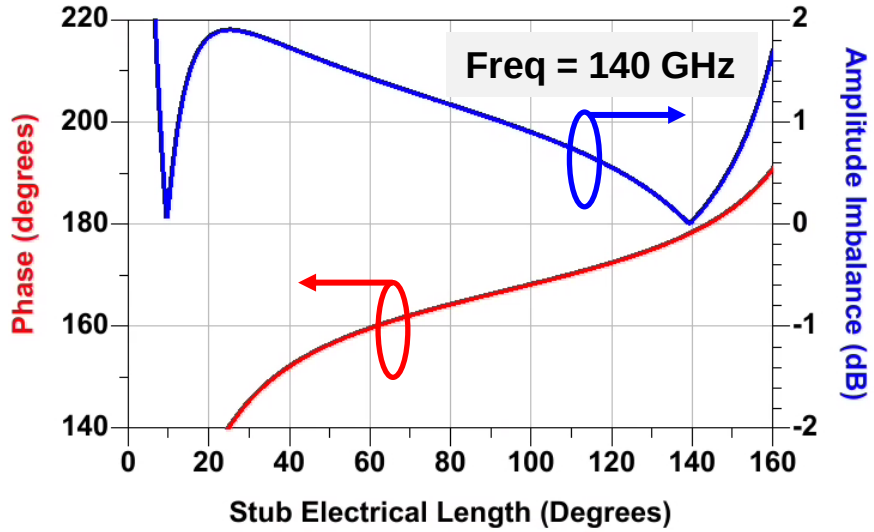


Coupled Line Balun

- Balun uses a compact short section coupled line for differential power combining
- DC feed through center tap
- Open stub added to tune phase balance
- Insertion loss of about 0.75 dB at 140 GHz

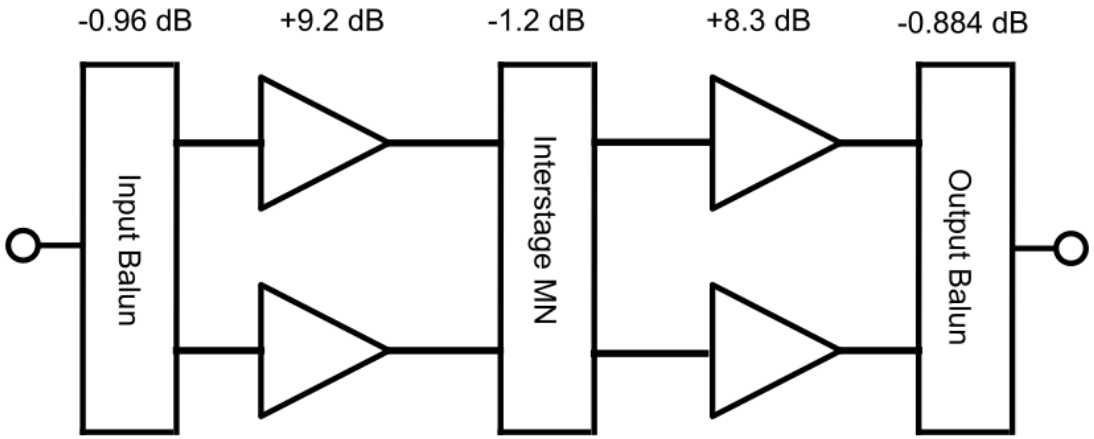


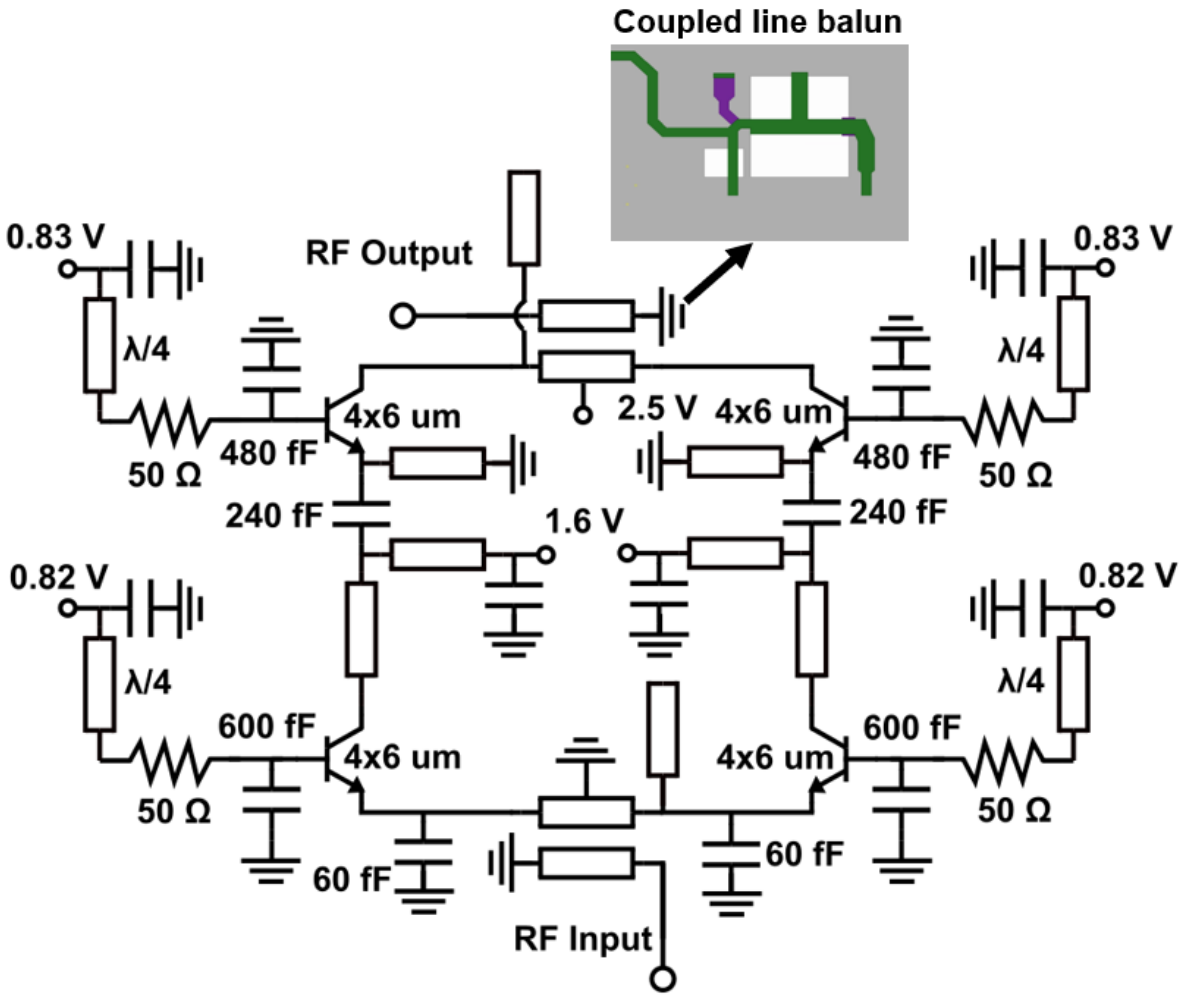




2-Stage PA Circuit

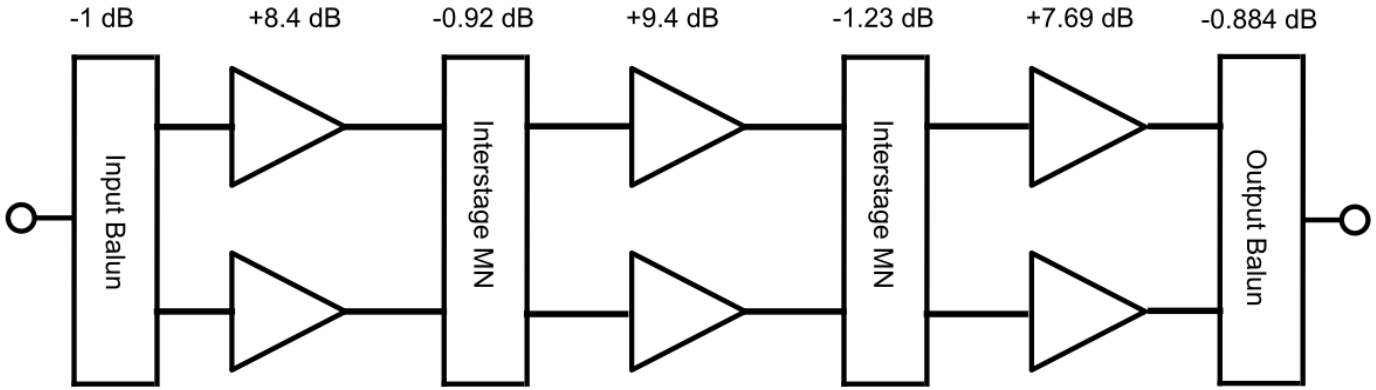
- 2-way combined pseudo-differential topology
- Output coupled line balun loss about 0.884 dB including pad loss of 0.13 dB
- Base capacitance tuned for higher OP1dB in output stage, but lowered gain

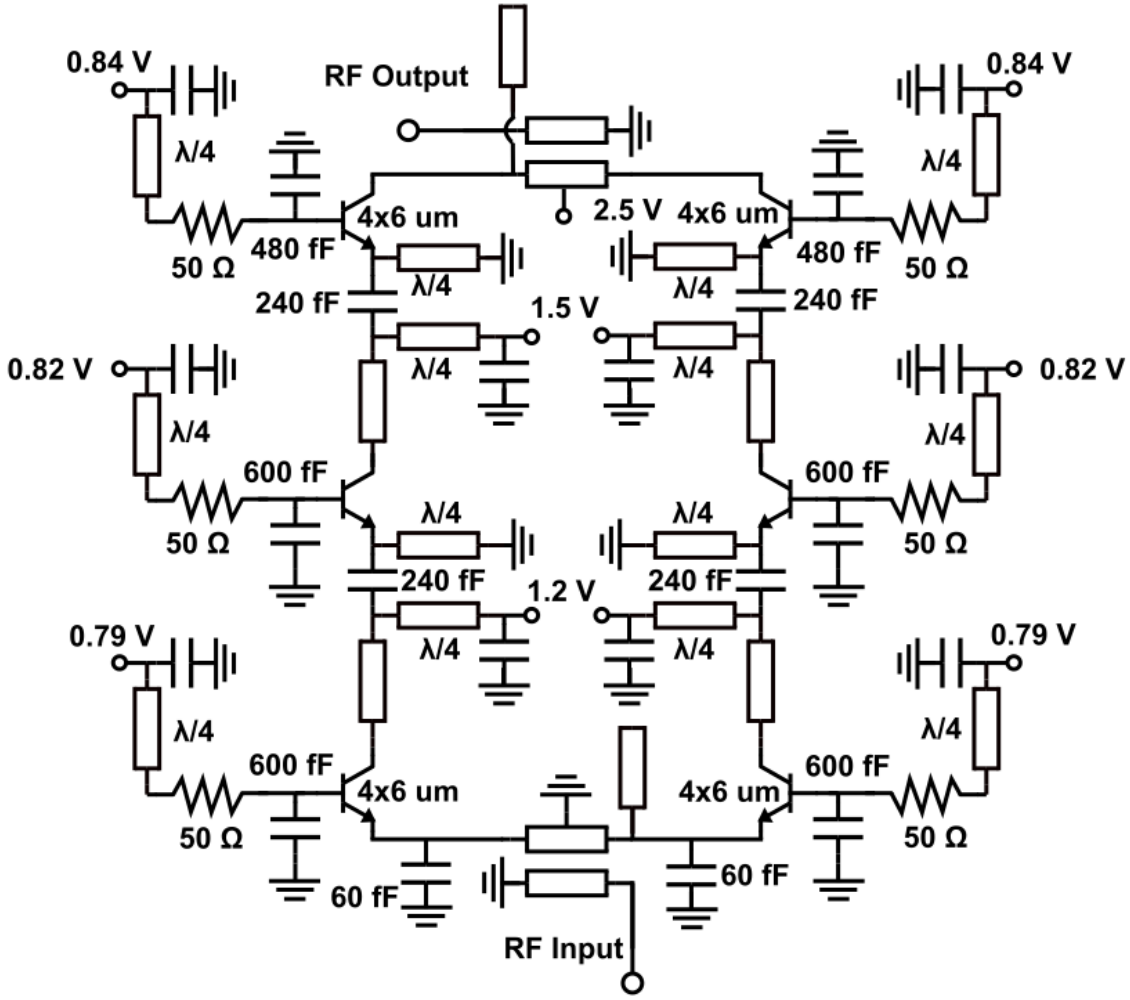




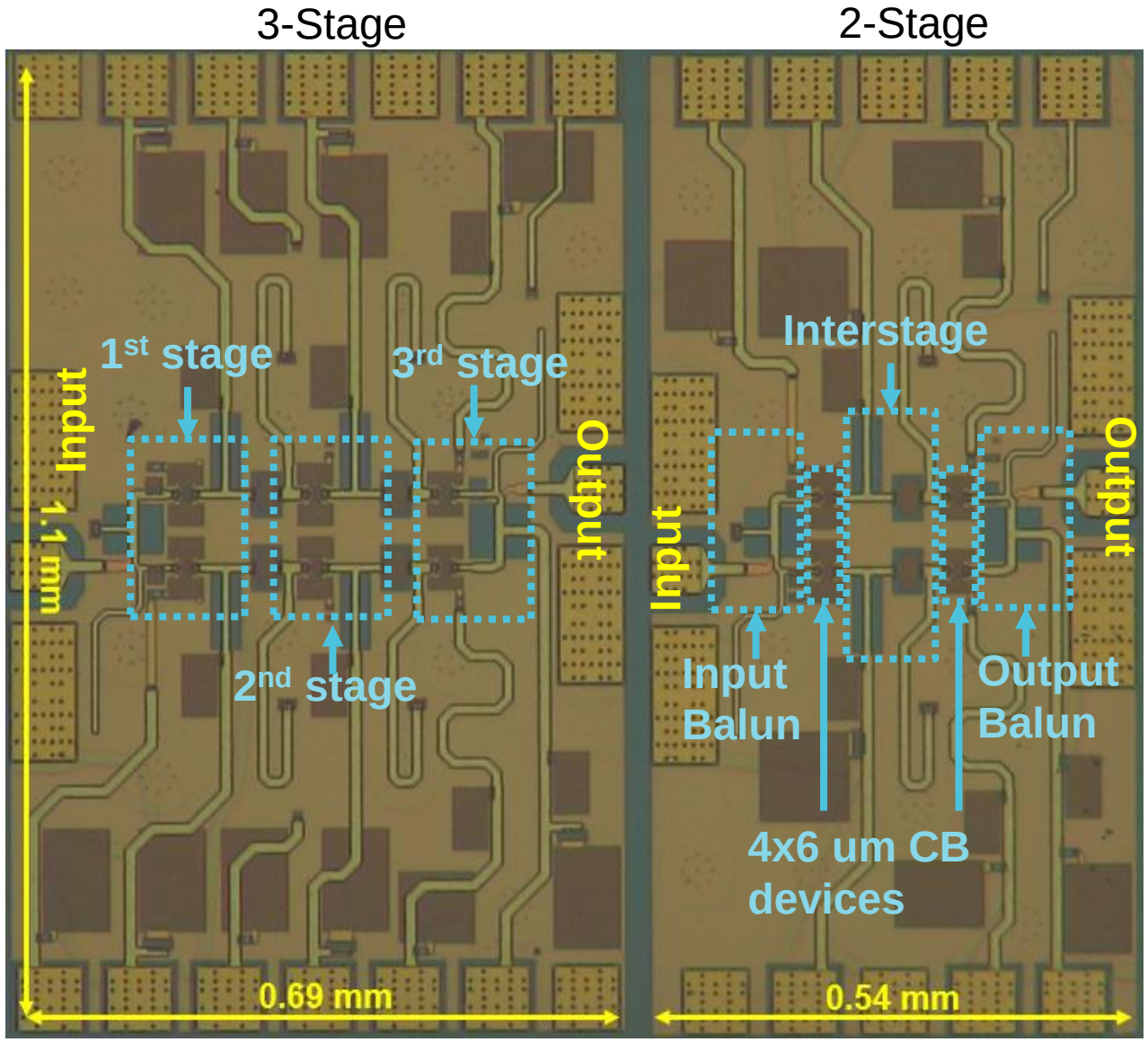
3-Stage PA Circuit

- Design is identical to 2-stage with an added stage biased slightly lower current
  - 1.2 VCE and 0.79 V Vbe for added first stage





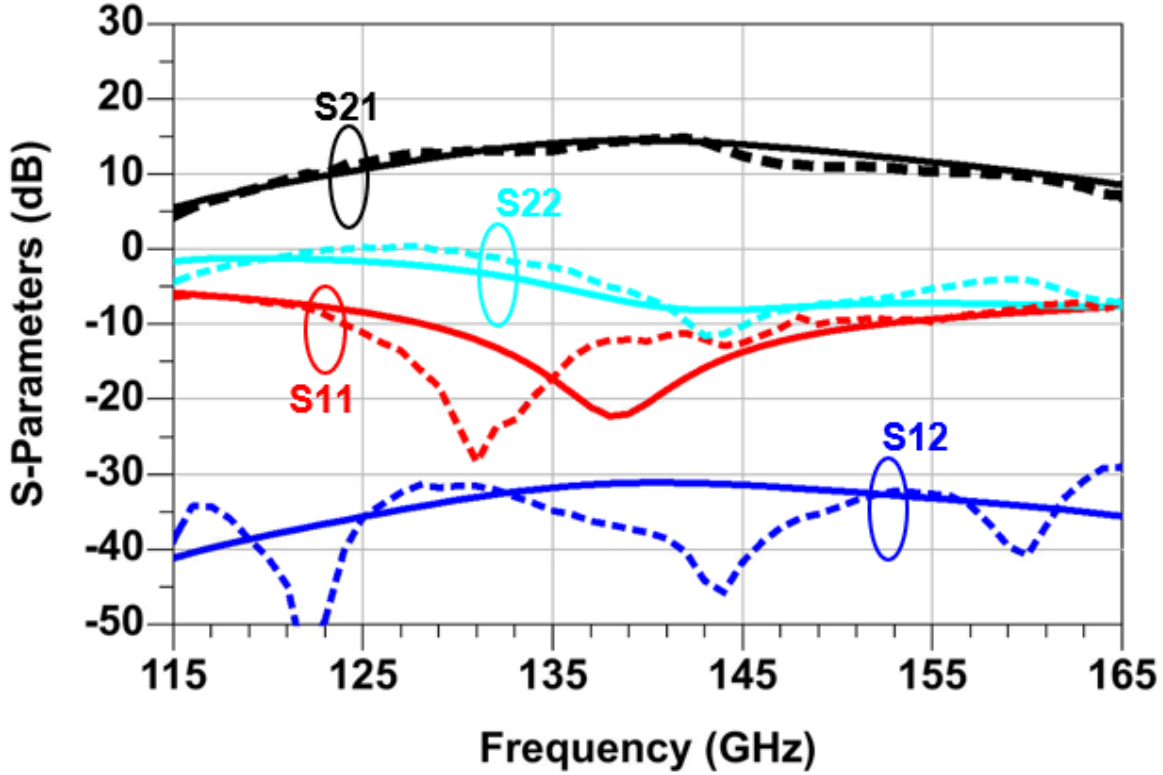
Chip Photograph



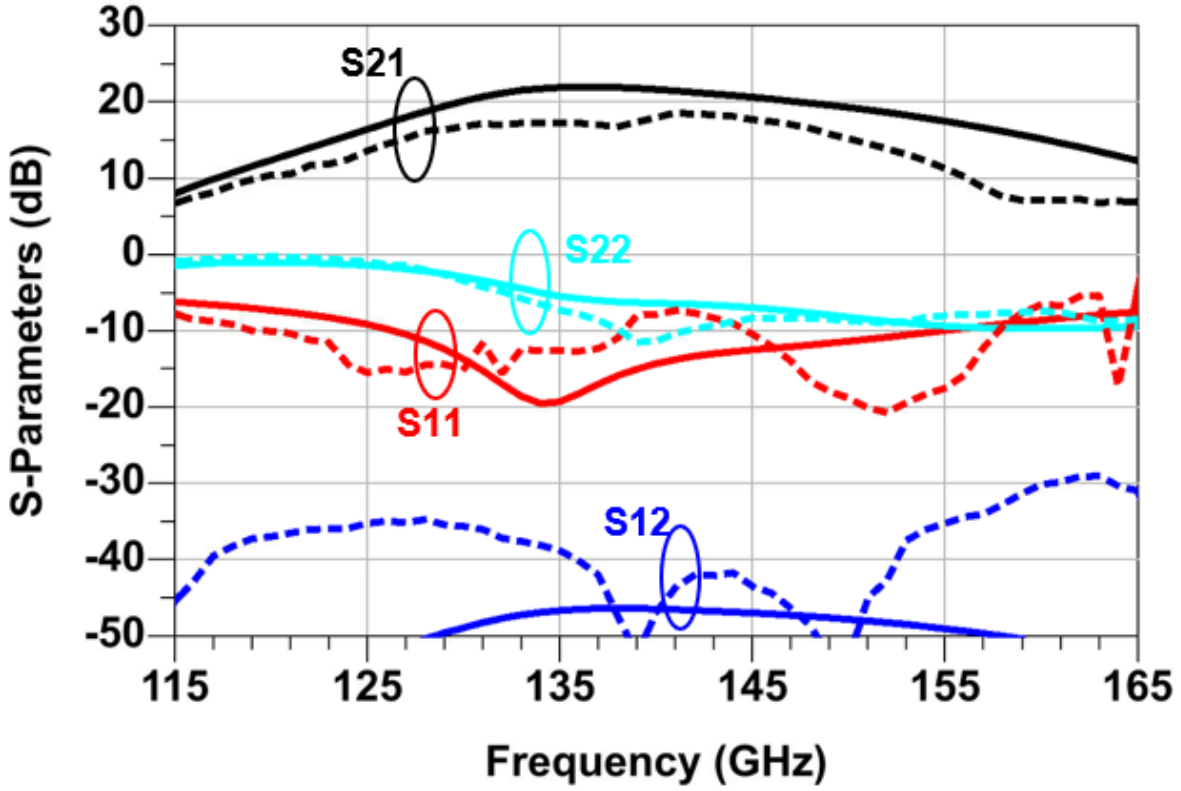
S-Parameter Measurements

Measurements (dotted lines) vs simulations (solid lines)

2-Stage Design



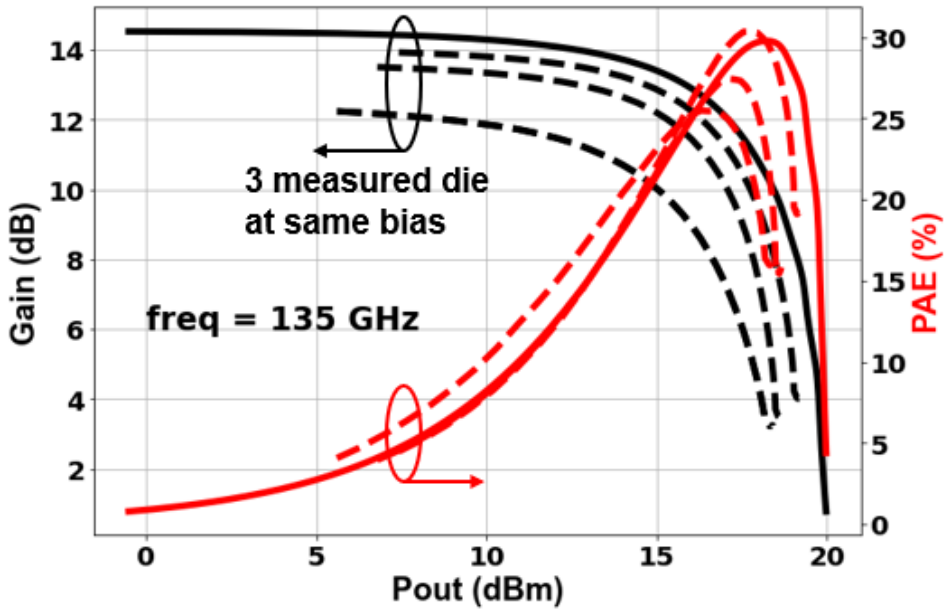
3-Stage Design

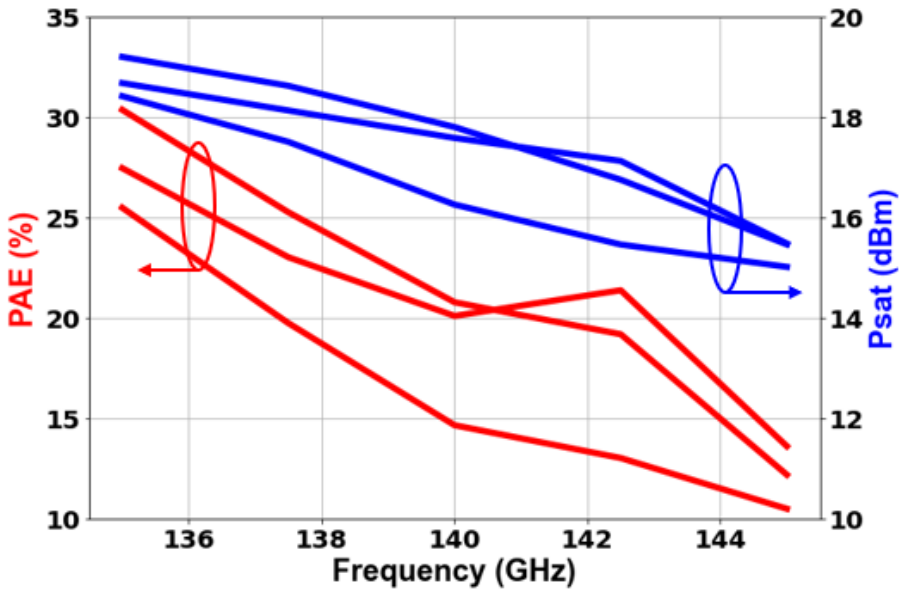


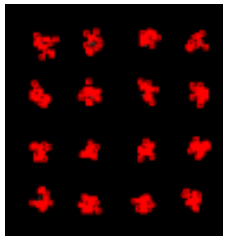
2-stage Measurement Results

- At 135 GHz, 30.4% peak PAE, 19.2% dBm Psat and 14 dB of gain
- Measurements cut off at 135 GHz due to spurs at lower D-band frequencies on VDI extenders
- 3 different die measurements show large gain variations
- EVM relatively unchanged compared to THRU measurement

Measurements (dotted lines) vs simulations (solid lines)



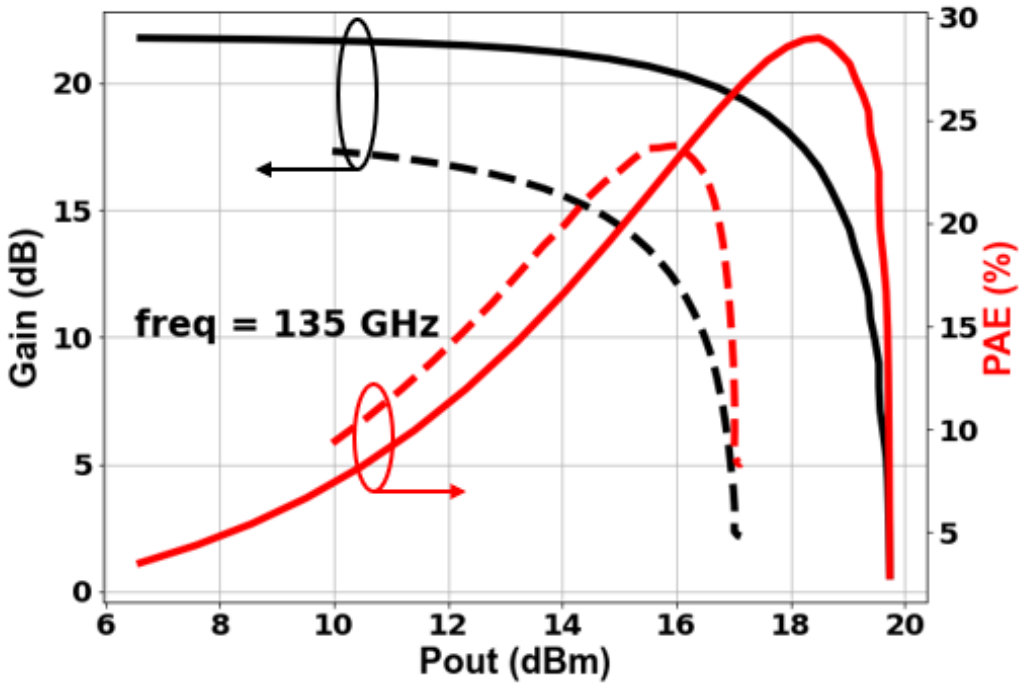


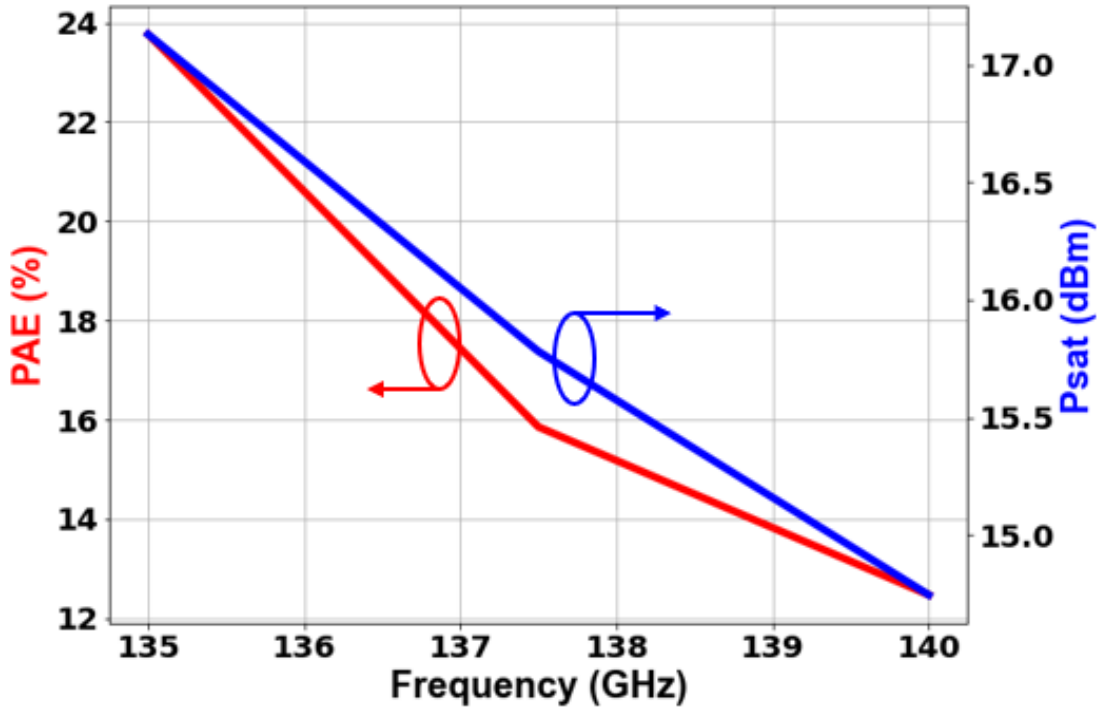


6.4% EVM
@-7dBm Pin
Freq = 130GHz

3-stage Measurement Results

- Measurement (dotted), simulations (solid)
- At 135 GHz, 23.8% peak PAE, 17.1 dBm Psat, 17.3 dB gain
- Identical RF design with added stage
- Subtle differences in the bias design and placement of TSVs





Comparison

- Highest PAE for this power level at D-band
- 2-stage with 30.4% peak PAE and 19.2 dBm Psat with 14 dB gain
- 3-stage with 23.8% peak PAE and 17.1 dBm Psat with 17.3 dB gain

Table 1. Comparison between State-of-the-Art D-band PAs

Reference	Technology	Frequency (GHz)	Gain (dB)	Psat (dBm)	PAE (%)	Chip Area (mm^2)
This Work	250nm InP HBT	135	14	19.2	30.4	0.59
			17.3	17.1	23.8	0.76
[6]	250nm InP HBT	118-148	7	15.3	32	0.2
[7]	250nm InP HBT	150-175	31.7	23.1-24	13.1-15.7	1.26
[4]	250nm InP HBT	125-150	12.3-15.9	18.9-20.5	14.3-20.8	0.69
[5]	250nm InP HBT	140	8.4	17.3	22.5	0.44 / 0.1*
[8]	250nm InP HBT	110-128	8.5	17.6	32.7	0.024
[9]	45nm CMOS SOI	140	24	17.5	13.4	0.43*
[10]	55nm SiGe	135	24	17.6	17.5	0.18
			22.4	19.3	13	0.76
[2]	130nm SiGe	161	30.7	18.1	12.4	0.42

*core area

Thank You!

Acknowledgements

- Thanks to Semiconductor research corporation (SRC) for funding this project through ComSenTer