Th3A-5

A Reconfigurable Reflective/Absorptive SPDT Plasma Switch

A. Fisher[1], T. R. Jones[1], and D. Peroulis[1]

[1]Purdue University, West Lafayette, IN, USA

Presentation Overview

Motivation

Technology Overview

Design

Testing

Results

Comparison

Conclusion

Presentation Overview

Motivation

Technology Overview

Design

Testing

Results

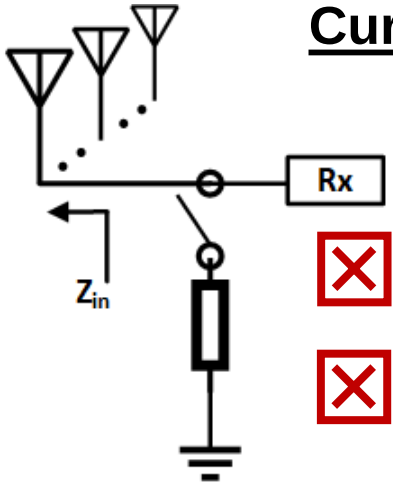
Comparison

Conclusion

Motivation

- Protect sensitive RFFEs (Rx)
- Static impedance (switched)
  - SMT resistor
  - Limited effectiveness as antenna impedance changes
    - Beamforming
- Low power absorption
  - Power limit to ~33 dBm (max) usually
- SSP a great candidate

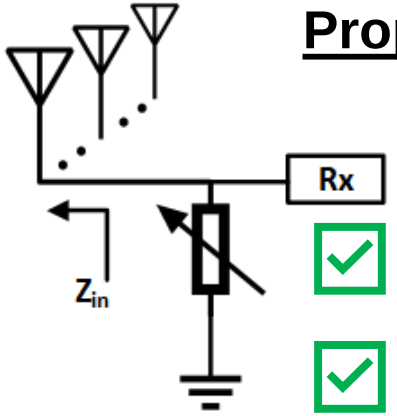
Current Topology



☒ Static Impedance

☒ Low power absorption

Proposed Topology



☑ Dynamic Impedance

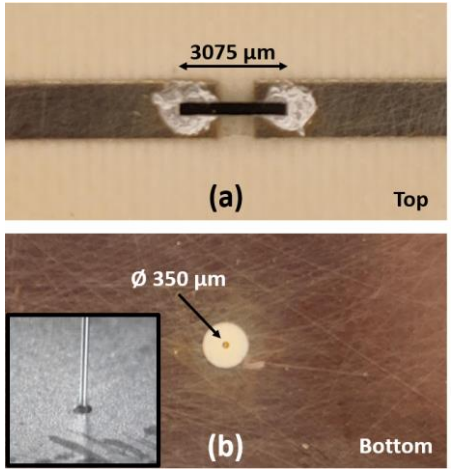
☑ High power absorption

Dynamic matching needed.

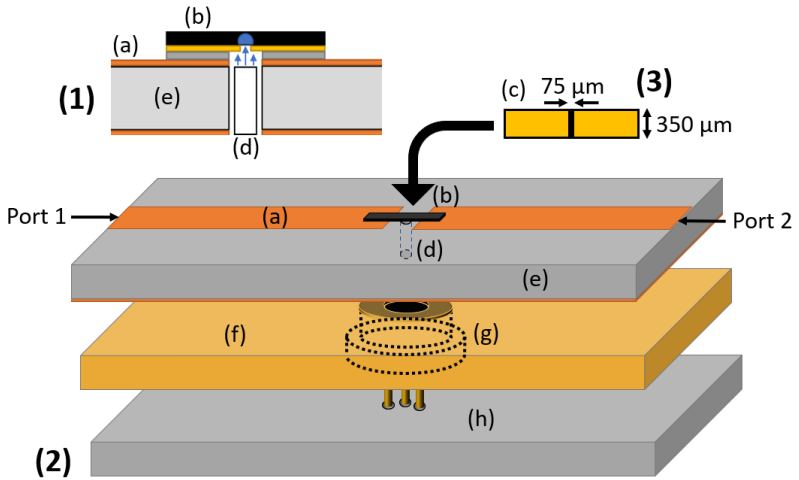
Solid-State Plasma Solution

- Solid-state plasma as a series switch
  - Variable control of equivalent resistance
  - Optical bias (electrically decoupled)
    - Wide bandwidth (including dc)
    - Low loss
  - High power handling
    - 100+ W CW, 30 W hot switching
    - Able to absorb without failure
  - Low loss (<0.2 dB)
  - High linearity (68.8 dBm IP3)
  - Single-digit µs switching

Series Switch



Integrated Optics



SSP a promising candidate.

Presentation Overview

Motivation

Technology Overview

Design

Testing

Results

Comparison

Conclusion

Principle of Operation

- Conductive channel
  - Optical excitation ($E_{ph} \geq E_{BG}$)
  - $\sigma \propto I_0$ (tunable response)

Recombination

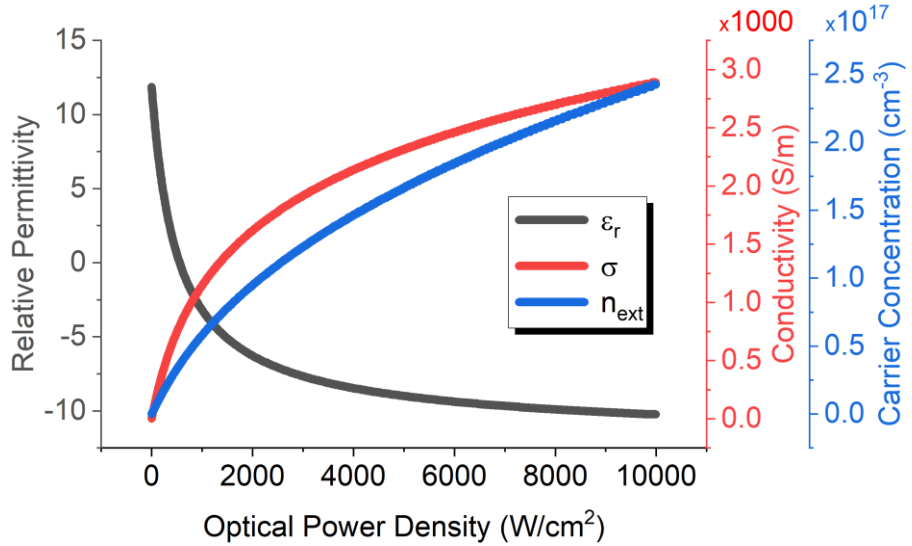
Diffusion

Generation

Steady-state

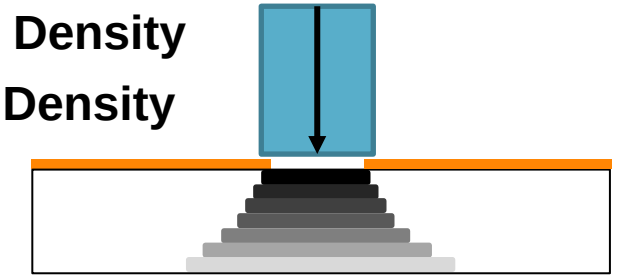
$$0 = D_n \nabla^2 n - \frac{n}{\tau} + G$$

$$\sigma(z) \approx q(\mu_e + \mu_h) \frac{\tau_a q_e I_0}{h\nu(L_a + \tau_a S)} e^{-z/L_a}$$



Higher Carrier Density

Lower Carrier Density

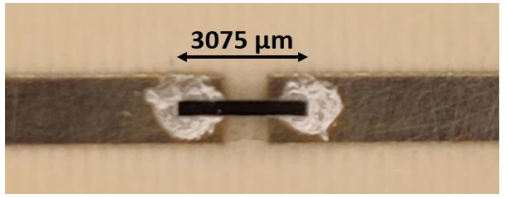


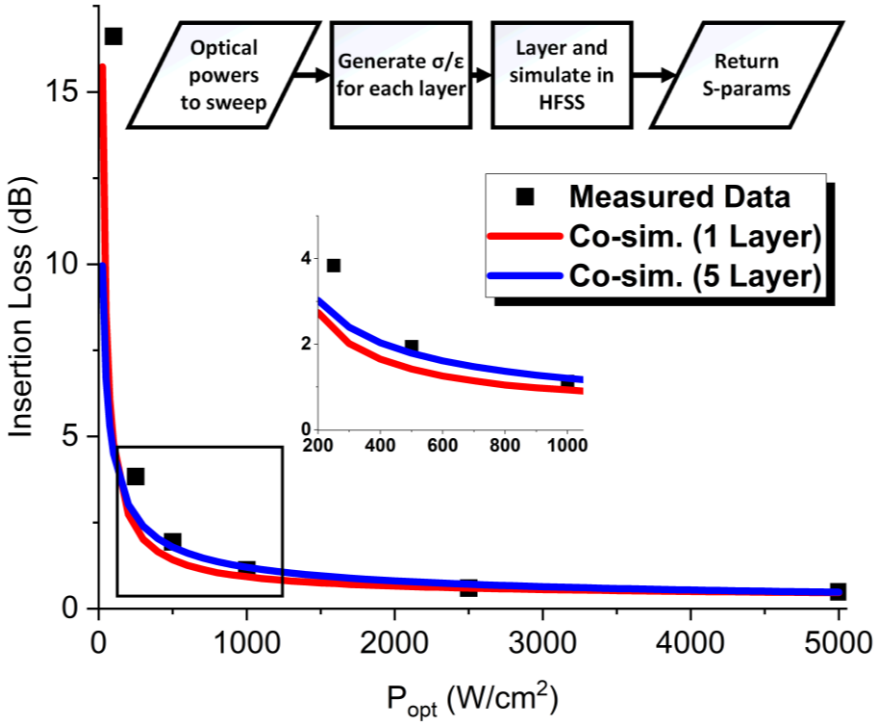
Tunable conductivity

Technology Overview

- Reliable co-simulations
  - Custom script + HFSS
  - Material + optical power density -> [S]
- Analog control over conductivity
  - Match any real impedance
  - Reconfigure reflective/absorptive
- Power consumption
  - Low loss = high dc power consumption

Example Switch





Accurate modelling for switch response

True reconfigurable reflective/absorptive switch behavior

Presentation Overview

Motivation

Technology Overview

Design

Testing

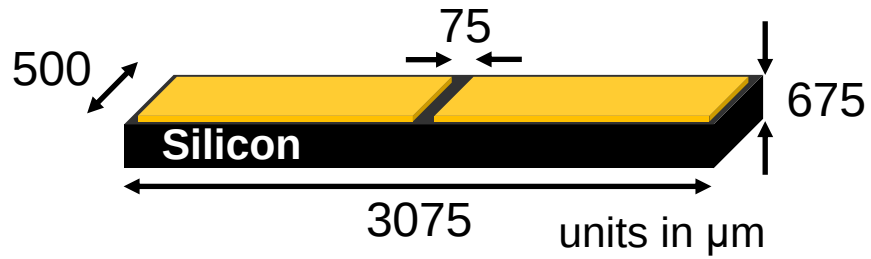
Results

Comparison

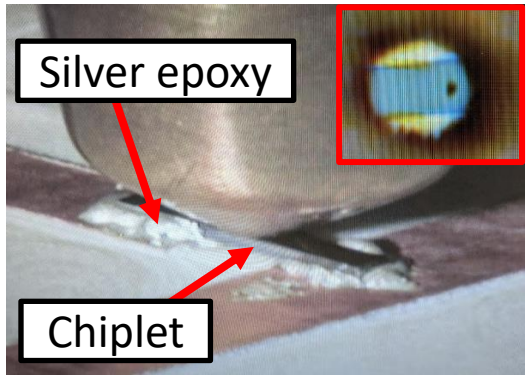
Conclusion

Design: Chiplet

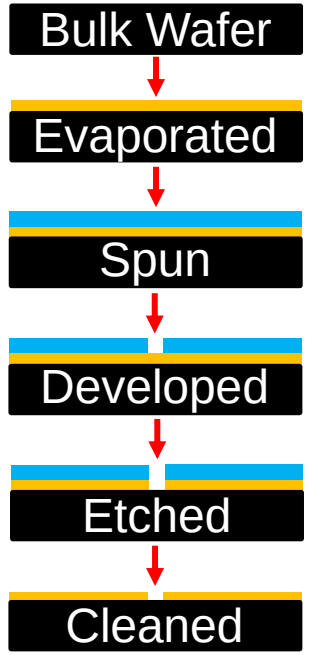
- Chiplet from [10]
  - HRS with patterned metal
  - Gap aperture accepts optical bias
- Microstrip gap
  - Gap placed over via w/ conductive epoxy
- Equivalent circuit
  - Parallel R-C



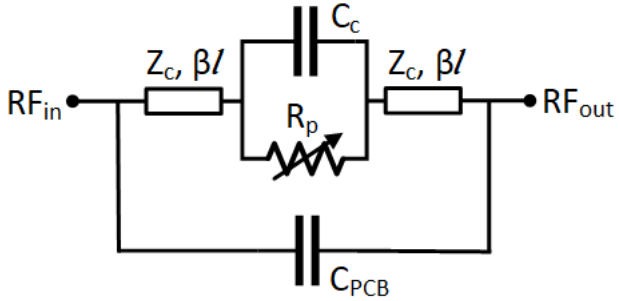
Placement/Alignment



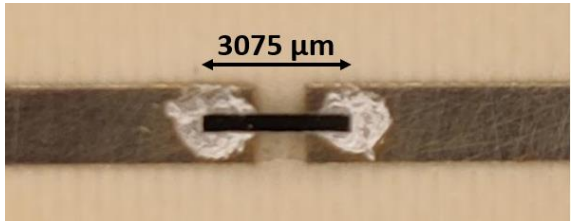
Fabrication



Equivalent Circuit

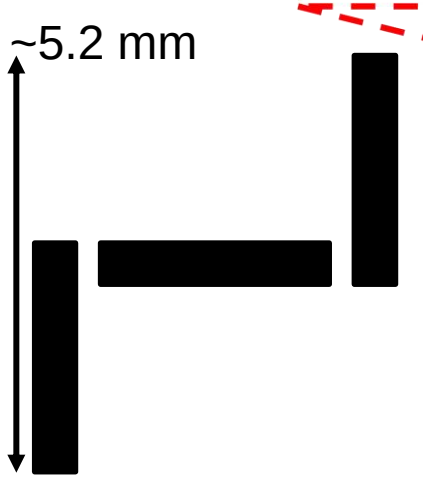


Equivalent Circuit

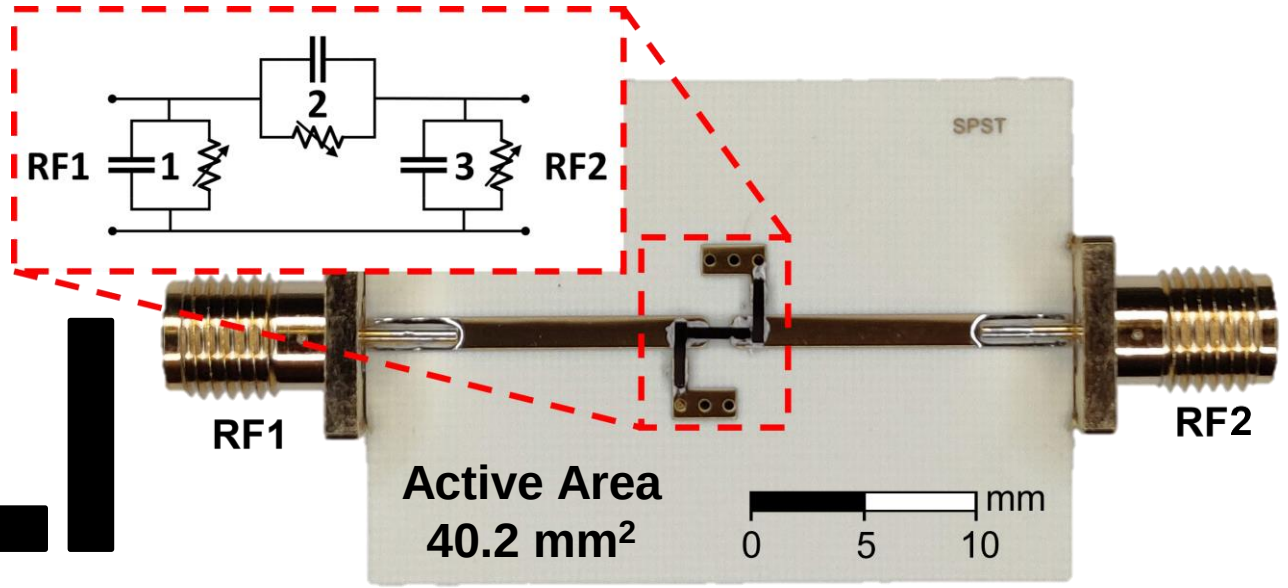


Design: SPST

- Series-shunt topology
  - Compact
  - Wide bandwidth
- Ground plane
  - Inductive stub
    - Via 200 µm
- RO4350B 30-mil
  - $\varepsilon_r = 3.38$
  - 1.6 mm for 50 ohms



2*0.5 – shunt width
2*0.15 – buffer
3.075 – series length
~4.4 mm



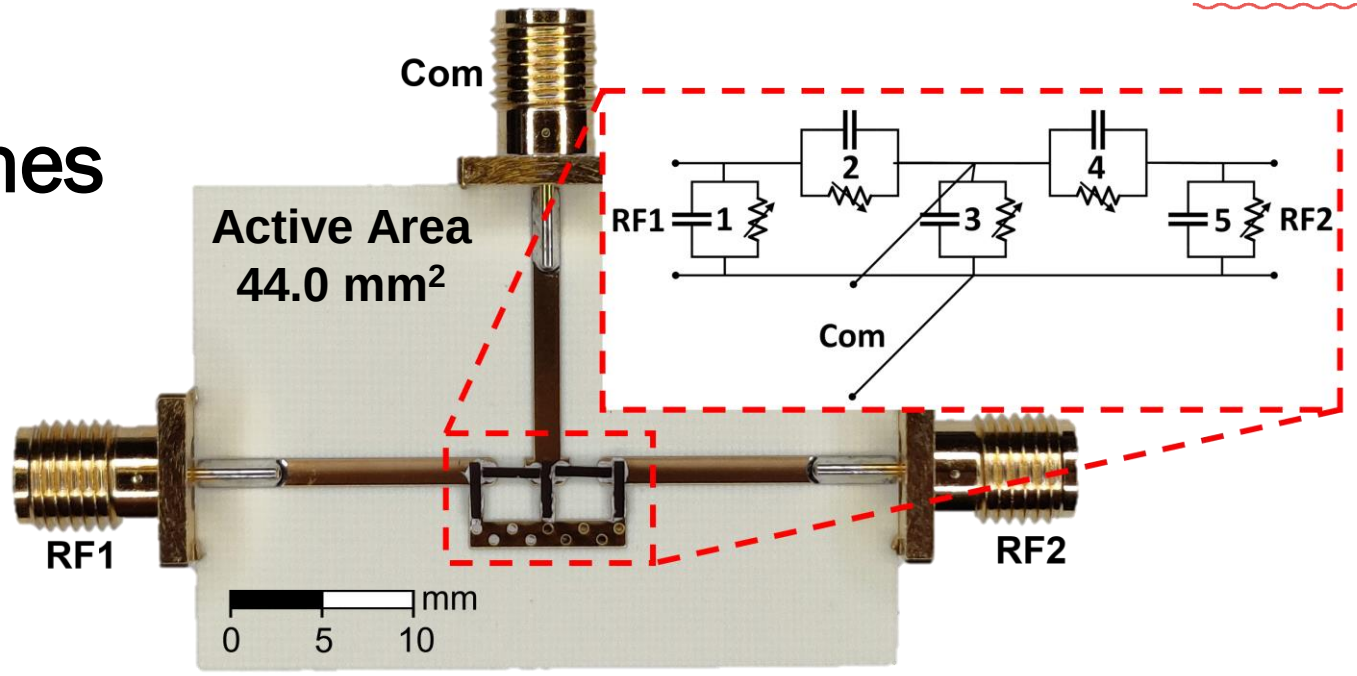
Assembled SPST

*Excludes added length/width from ground plane

Designed for wide bandwidth, compactness

Design: SPDT

- Two cascaded SPST switches
- All ports have ability to be matched
- Eval board size similar to SPST
  - Reduce number of cal standards
- Fast switching speeds
  - Down to single-digit µs



3*0.5 – shunt width
4*0.15 – buffer
2*3.075 – series length
~8.3 mm

*Excludes added length/width from ground plane

Designed for wide bandwidth, compactness

Presentation Overview

Motivation

Technology Overview

Design

Testing

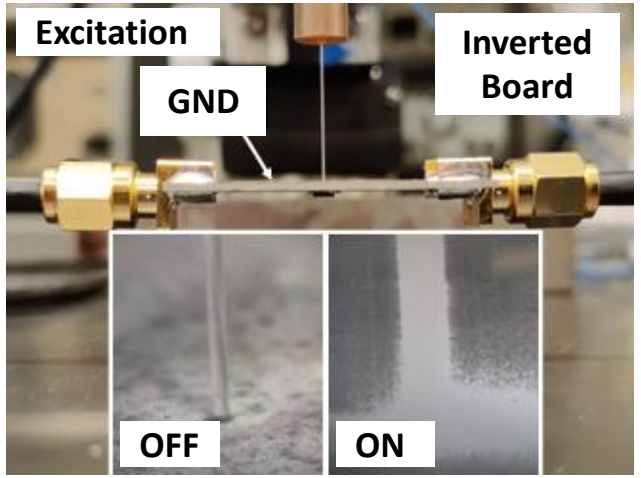
Results

Comparison

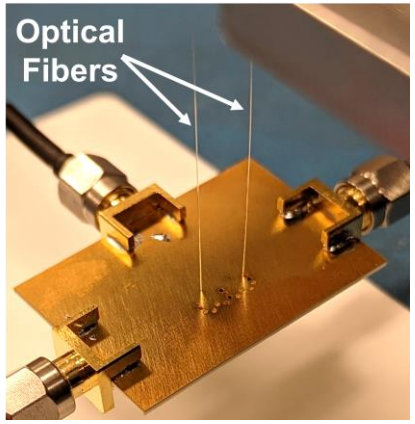
Conclusion

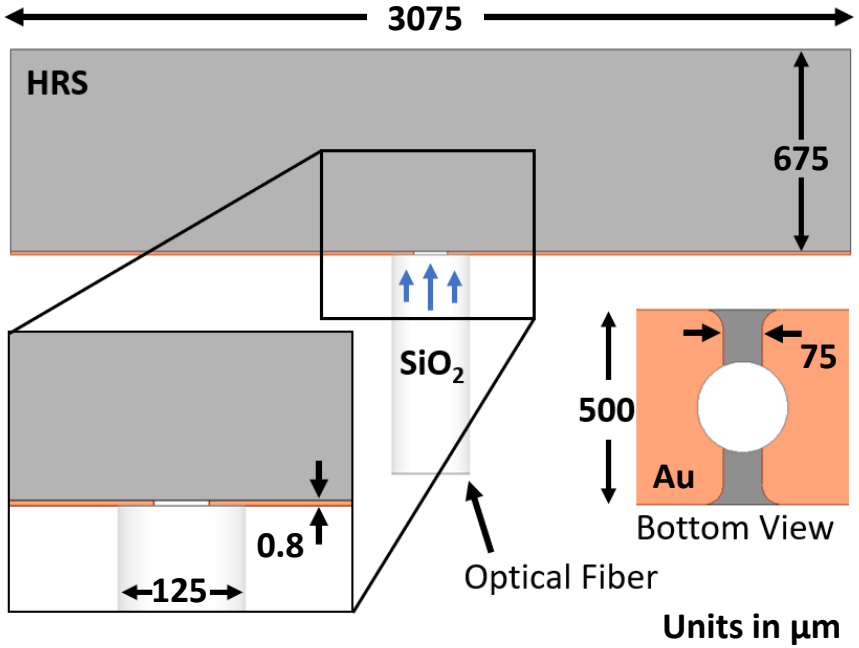
Test Setup

- Common excitation
  - Via in PCB allows for fiber insertion
    - Board inverted for access
  - Optical bias in chiplet aperture
- Series switch
  - Light OFF = Switch OFF
  - Light ON = Switch ON



SPDT Testing





Optical excitation (bias) setup.

Presentation Overview

Motivation

Technology Overview

Design

Testing

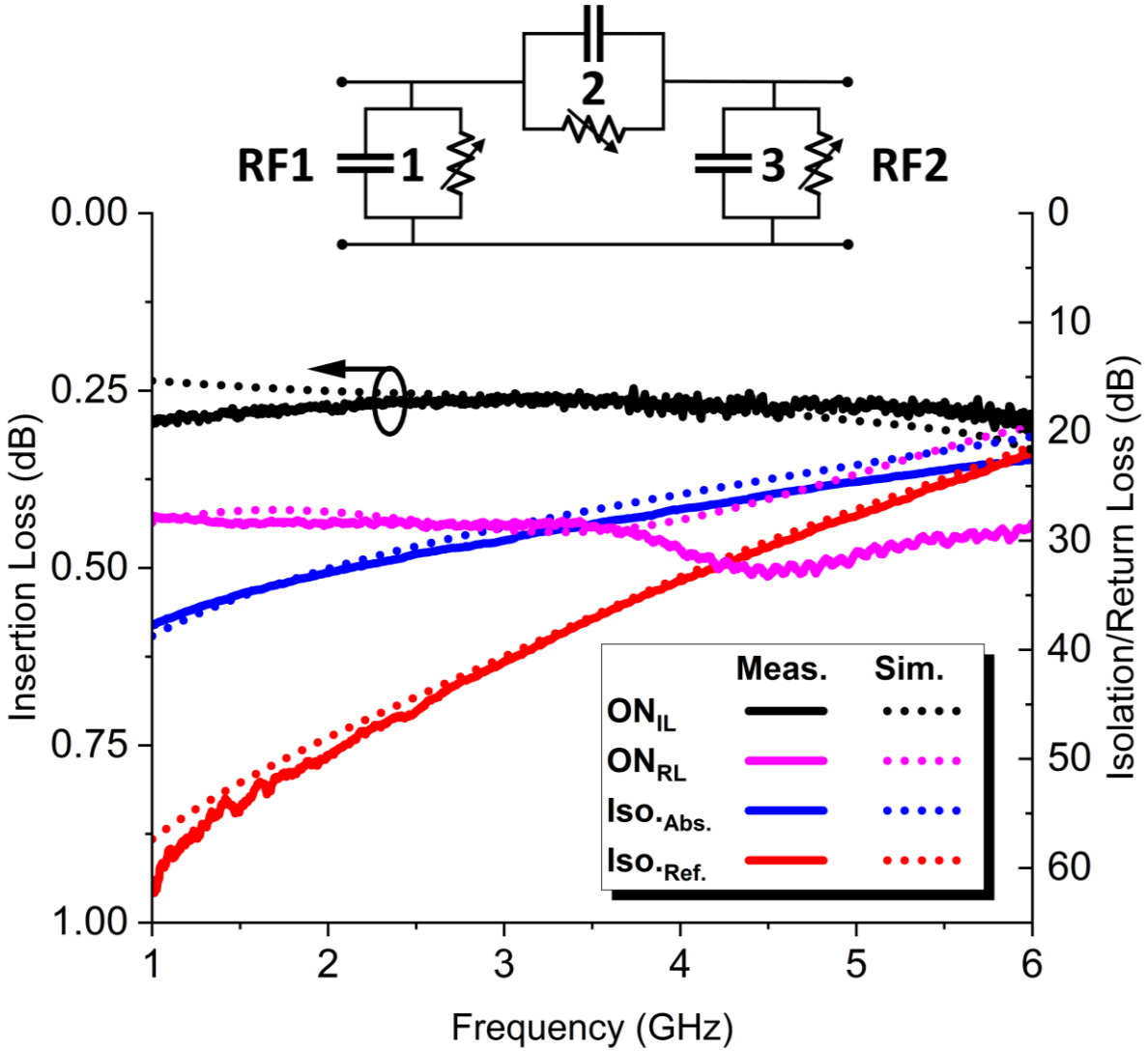
Results

Comparison

Conclusion

Results: SPST

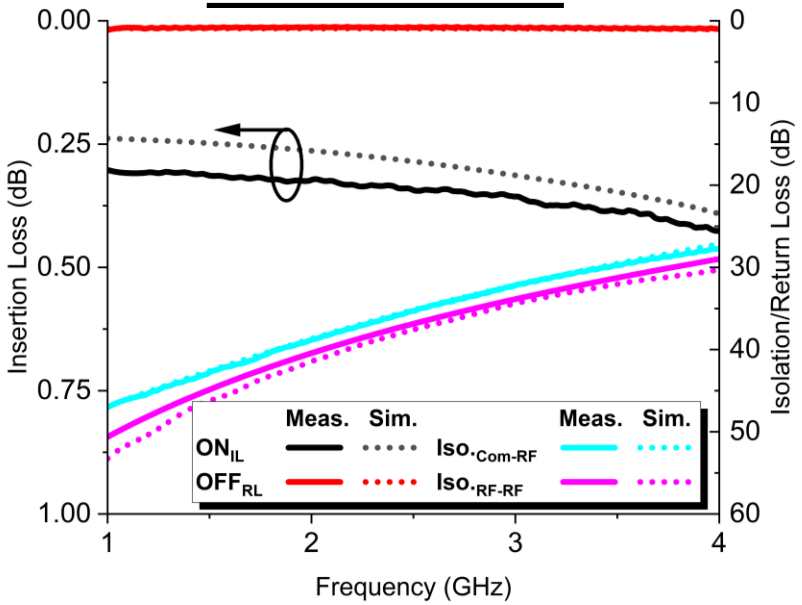
- dc-6 GHz
- ON state
  - SW 2 ON
  - IL: 0.27 dB (flat response)
  - RL: >28 dB
- OFF state Isolation
  - SW 1 & 3 ON (var. powers)
  - Ref: 62->22.5 dB
  - Abs: 35->22.5 dB



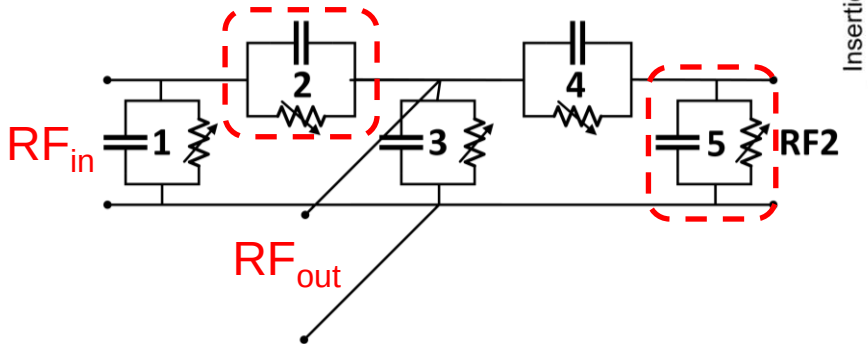
Dual mode absorptive/reflective switch behavior.

Results: SPDT

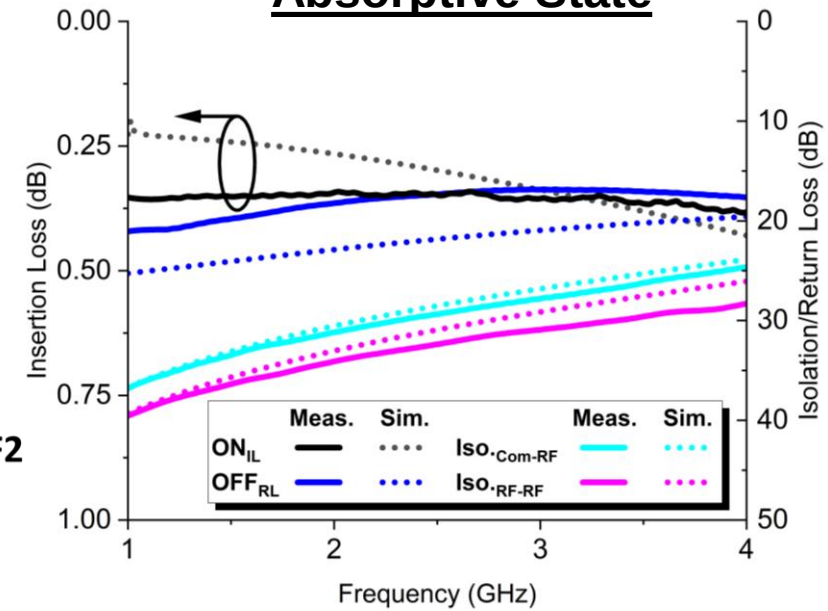
Reflective State



- Dc-4 GHz
- IL: <0.43 dB

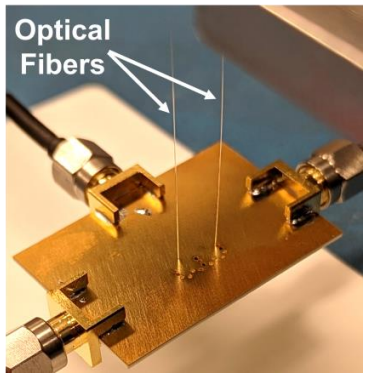


Absorptive State



- 2 & 5 fully ON
- Isolation
  - RF_{in}-RF_2: 53-30 dB
  - Com-RF_2: 46-28 dB

2-Fiber Testing

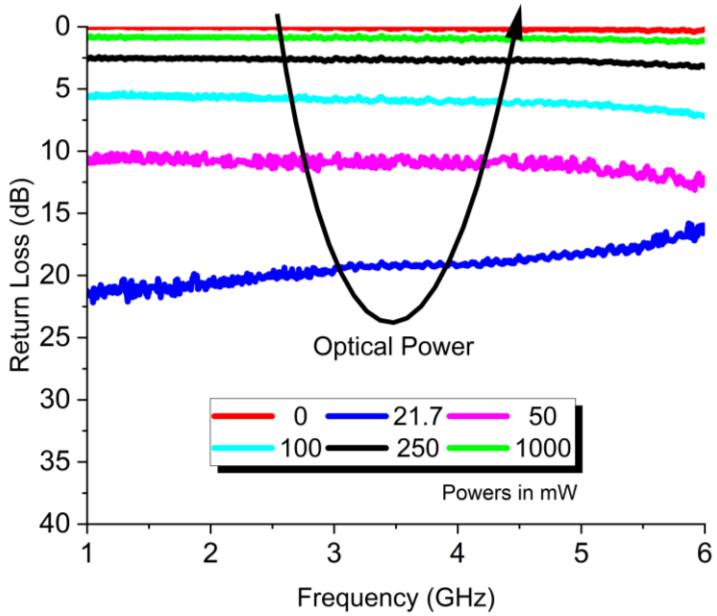


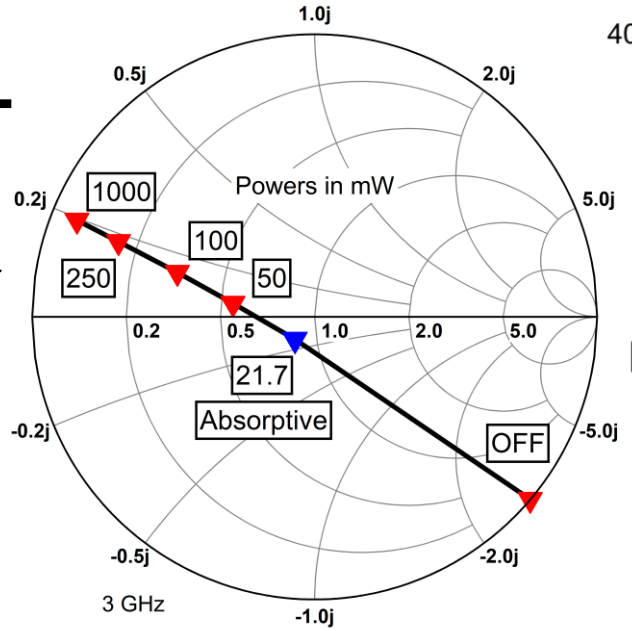
- 2 fully ON, 5 abs. state
- RL: ~20 dB (@ RF_2)
- Isolation
  - RF_{in}-RF_2: 40-28 dB
  - Com-RF_2: 36-25 dB

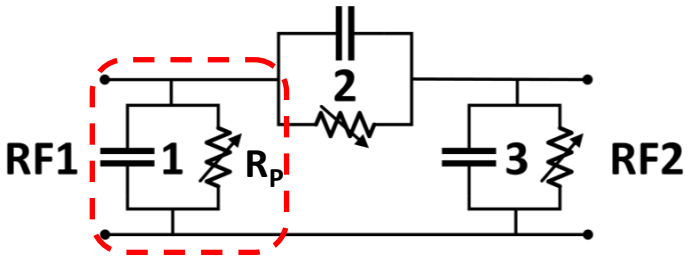
Great performance and reconfigurable

Results: Varying Z_0

- Shunt-configured chiplet in SPST
  - SW 1 ON (varying optical powers)
  - OFF state RL varied
  - $R_P \propto {}^{1}/_{I_0}$
- Optical power swept until RL maximized
  - $\boldsymbol{Re|Z_{in}| = 50\ \Omega\ @\ 21.7\ mW}$



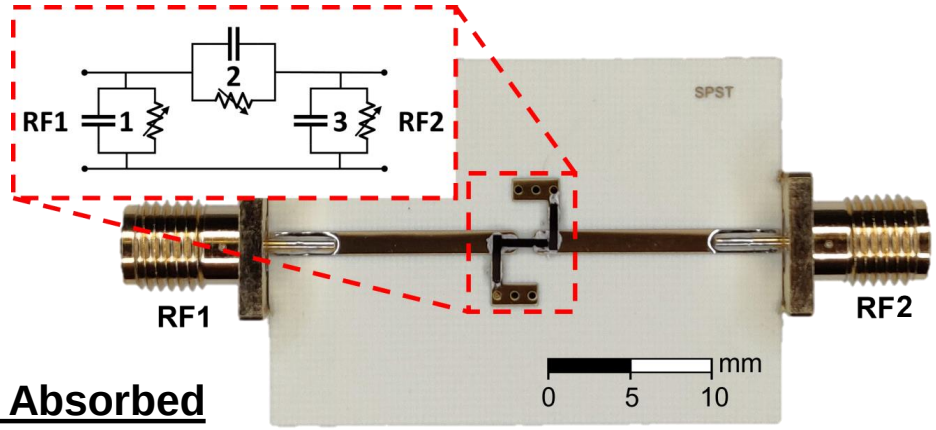




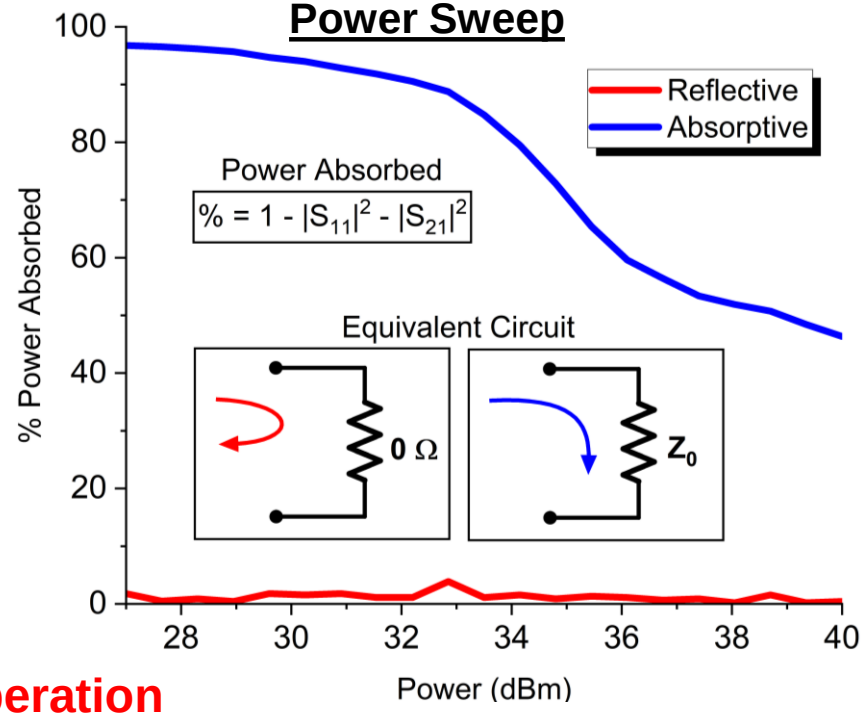
Control over $Re|Z_{in}|$

Results: High-Power Absorption

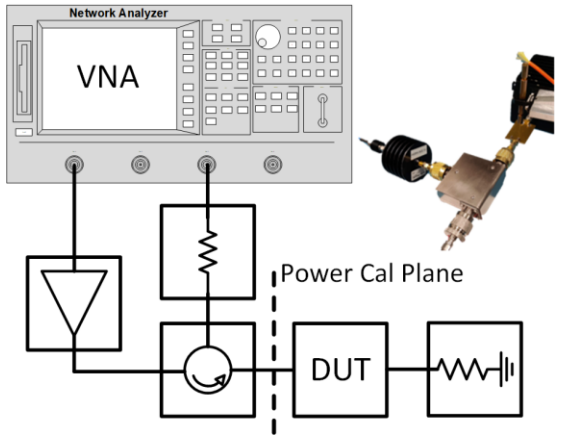
- Single shunt element (SW 1)
  - Fully ON state – ~0 Ω
    - ~1000 mW
    - Reflective
  - Zo state – 50 Ω
    - ~21.7 mW
    - Absorptive
- >10 W survivability
- >10 dB @ 33 dBm



Reflective and Absorbed Power Sweep



High-Power Setup



DC power reduction by 46x
High absorbed power and dual mode operation

Presentation Overview

Motivation

Technology Overview

Design

Testing

Results

Comparison

Conclusion

Discussion

- Reflective SPST: lower loss, higher power handling
- Absorptive SPST: DC operation, lower loss, higher absorbed power
- Reflective SPDT: Higher power handling
- Absorptive SPDT: DC operation, lower loss, higher absorbed power

Table 1. Comparison of State-of-the-Art SPST and SPDT Switches.

Ref.	Technology	[a]Configuration	Freq. (GHz)	IL (dB)	[b]Iso. (dB)	[c]Iso. (dB)	[d]RL (dB)	[e]Power (W)
This Work	SSP-Si	$SPST_R$	0-6	0.27	62-22	-	-	35
HMC550A	GaAs	$SPST_R$	0-6	0.7	22-10	-	-	<2.5
This Work	SSP-Si	$SPST_A$	0-6	0.27	38-22.5	-	>17.5	35/10+
QPC6014	SOI	$SPST_A$	0.005-6	0.5-1.3	62-35	-	35-15	5/0.8
This Work	SSP-Si	$SPDT_R$	0-4	<0.43	54-30	47.5-28	-	35
MM5140	MEMS	$SP4T_R$	0-6	0.4	>27	>27	-	25
This Work	SSP-Si	$SPDT_A$	0-4	<0.38	39.5-28	37-25	25-16.8	35/10+
HMC8038W	Si	$SPDT_A$	0.1-6	0.6-0.9	60-40	73-51	21-17	3.2/1

[a]Subscript denotes reflective (R) or absorptive (A) operation. [b]RF-RF. [c]Com-RF. [d]Isolated port. [e]ON state/Absorbed power handling.

Discussion

- Reflective SPST: lower loss, higher power handling
- **Absorptive SPST: DC operation, lower loss, higher absorbed power**
- Reflective SPDT: Higher power handling
- Absorptive SPDT: DC operation, lower loss, higher absorbed power

Table 1. Comparison of State-of-the-Art SPST and SPDT Switches.

Ref.	Technology	[a]Configuration	Freq. (GHz)	IL (dB)	[b]Iso. (dB)	[c]Iso. (dB)	[d]RL (dB)	[e]Power (W)
This Work	SSP-Si	$SPST_R$	0-6	0.27	62-22	-	-	35
HMC550A	GaAs	$SPST_R$	0-6	0.7	22-10	-	-	<2.5
This Work	SSP-Si	$SPST_A$	0-6	0.27	38-22.5	-	>17.5	35/10+
QPC6014	SOI	$SPST_A$	0.005-6	0.5-1.3	62-35	-	35-15	5/0.8
This Work	SSP-Si	$SPDT_R$	0-4	<0.43	54-30	47.5-28	-	35
MM5140	MEMS	$SP4T_R$	0-6	0.4	>27	>27	-	25
This Work	SSP-Si	$SPDT_A$	0-4	<0.38	39.5-28	37-25	25-16.8	35/10+
HMC8038W	Si	$SPDT_A$	0.1-6	0.6-0.9	60-40	73-51	21-17	3.2/1

[a]Subscript denotes reflective (R) or absorptive (A) operation. [b]RF-RF. [c]Com-RF. [d]Isolated port. [e]ON state/Absorbed power handling.

Highest absorbed power

Discussion

- Reflective SPST: lower loss, higher power handling
- Absorptive SPST: DC operation, lower loss, higher absorbed power
- **Reflective SPDT: Higher power handling**
- Absorptive SPDT: DC operation, lower loss, higher absorbed power

Table 1. Comparison of State-of-the-Art SPST and SPDT Switches.

Ref.	Technology	[a]Configuration	Freq. (GHz)	IL (dB)	[b]Iso. (dB)	[c]Iso. (dB)	[d]RL (dB)	[e]Power (W)
This Work	SSP-Si	$SPST_R$	0-6	0.27	62-22	-	-	35
HMC550A	GaAs	$SPST_R$	0-6	0.7	22-10	-	-	<2.5
This Work	SSP-Si	$SPST_A$	0-6	0.27	38-22.5	-	>17.5	35/10+
QPC6014	SOI	$SPST_A$	0.005-6	0.5-1.3	62-35	-	35-15	5/0.8
This Work	SSP-Si	$SPDT_R$	0-4	<0.43	54-30	47.5-28	-	35
MM5140	MEMS	$SP4T_R$	0-6	0.4	>27	>27	-	25
This Work	SSP-Si	$SPDT_A$	0-4	<0.38	39.5-28	37-25	25-16.8	35/10+
HMC8038W	Si	$SPDT_A$	0.1-6	0.6-0.9	60-40	73-51	21-17	3.2/1

[a]Subscript denotes reflective (R) or absorptive (A) operation. [b]RF-RF. [c]Com-RF. [d]Isolated port. [e]ON state/Absorbed power handling.

Discussion

- Reflective SPST: lower loss, higher power handling
- Absorptive SPST: DC operation, lower loss, higher absorbed power
- Reflective SPDT: Higher power handling
- **Absorptive SPDT: DC operation, lower loss, higher absorbed power**

Table 1. Comparison of State-of-the-Art SPST and SPDT Switches.

Ref.	Technology	[a]Configuration	Freq. (GHz)	IL (dB)	[b]Iso. (dB)	[c]Iso. (dB)	[d]RL (dB)	[e]Power (W)
This Work	SSP-Si	$SPST_R$	0-6	0.27	62-22	-	-	35
HMC550A	GaAs	$SPST_R$	0-6	0.7	22-10	-	-	<2.5
This Work	SSP-Si	$SPST_A$	0-6	0.27	38-22.5	-	>17.5	35/10+
QPC6014	SOI	$SPST_A$	0.005-6	0.5-1.3	62-35	-	35-15	5/0.8
This Work	SSP-Si	$SPDT_R$	0-4	<0.43	54-30	47.5-28	-	35
MM5140	MEMS	$SP4T_R$	0-6	0.4	>27	>27	-	25
This Work	SSP-Si	$SPDT_A$	0-4	<0.38	39.5-28	37-25	25-16.8	35/10+
HMC8038W	Si	$SPDT_A$	0.1-6	0.6-0.9	60-40	73-51	21-17	3.2/1

[a]Subscript denotes reflective (R) or absorptive (A) operation. [b]RF-RF. [c]Com-RF. [d]Isolated port. [e]ON state/Absorbed power handling.

Highest absorbed power

Presentation Overview

Motivation

Technology Overview

Design

Testing

Results

Comparison

Conclusion

Conclusion

- DC power reduction
  - 46x reduction (1000 -> 21.7 mW)
- High power handling and absorption
- Reflective/absorptive change
- Dynamic impedance matching
- First time planar SSP as a SPDT switch
- First time absorbed power handling in SSP measured

Dynamic impedance matching to absorb high incident powers

- Funding from the Office of Naval Research
  - Award #: N00014-19-1-2549

- Questions?
  - fishe128@purdue.edu or dperouli@purdue.edu