

**Tu1D-3**

# A Flip-Chip W-band On-off Keying Receiver in 90-nm CMOS

**Hong-Shen Chen, Hong-Wei Wu, Yun-Ting Tseng, and Jenny Yi-Chun Liu**

**Department of Electrical Engineering,  
National Tsing Hua University, Taiwan**

# Outline

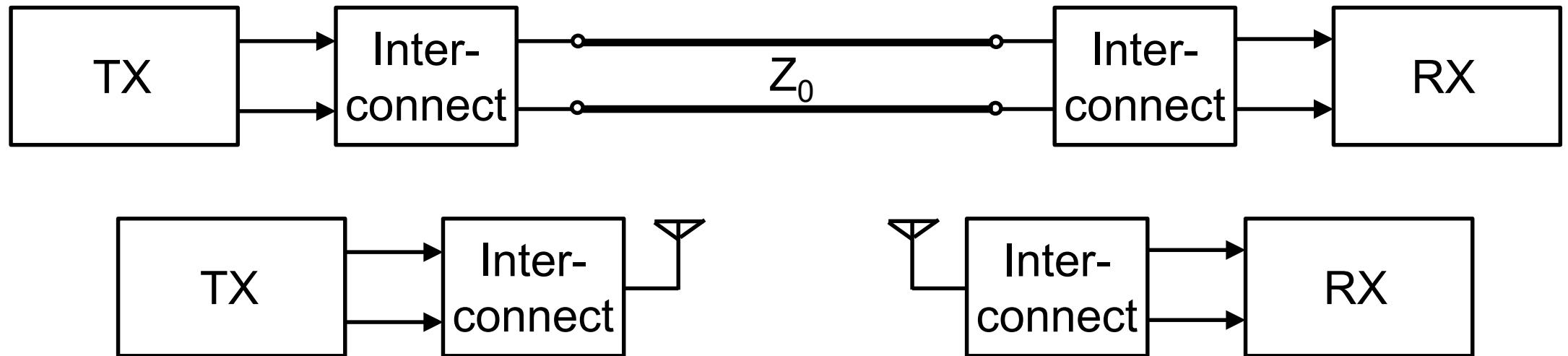
- Introduction
- Circuit design
- Chip implementation and measurement
- Conclusion

# Outline

- Introduction
- Circuit design
- Chip implementation and measurement
- Conclusion

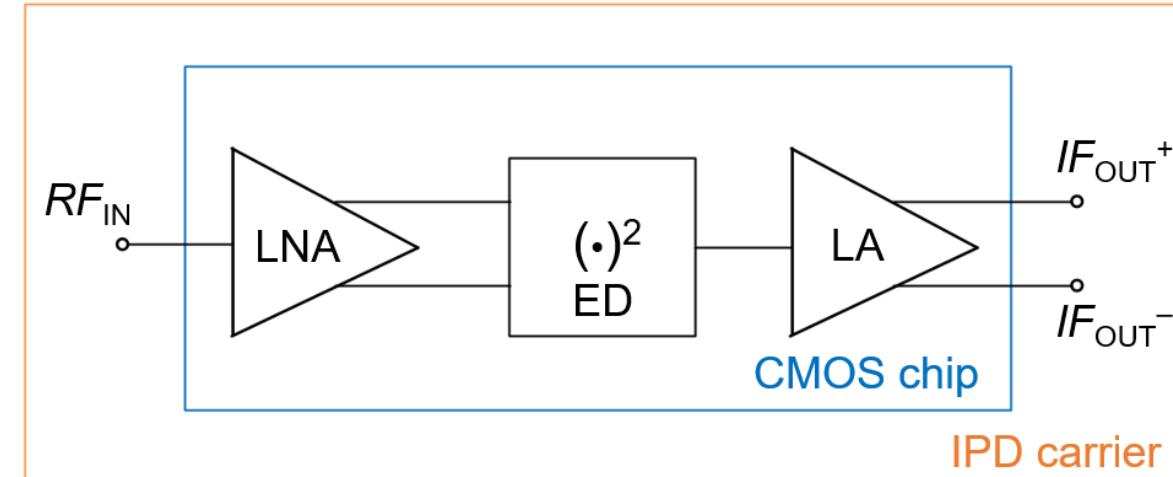
# Millimeter Wave Transceivers

- Millimeter-wave signal for intermediate-range wireline [1] and short-range wireless communication [2].



# Block Diagram and Challenges

- OOK RX: LNA, envelope detector (ED), limiting amplifier (LA).



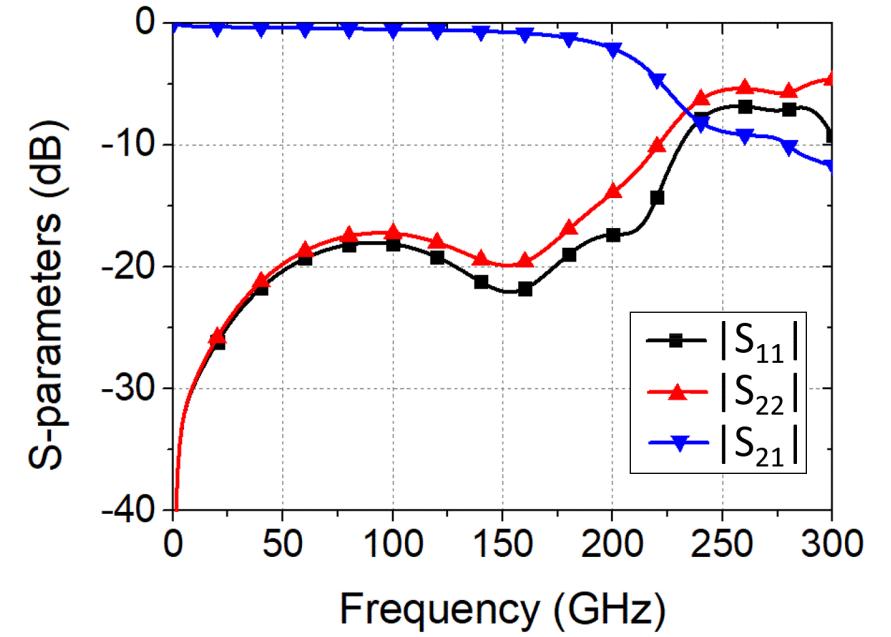
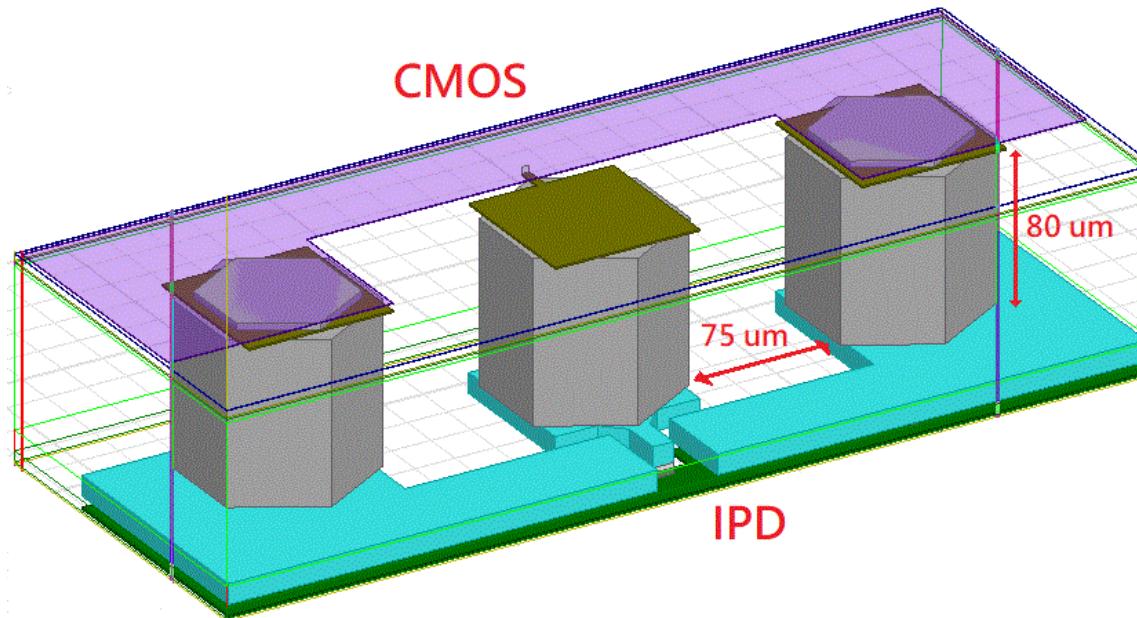
- Wideband LNA and high responsivity in ED are essential for OOK signal receiving.

# Outline

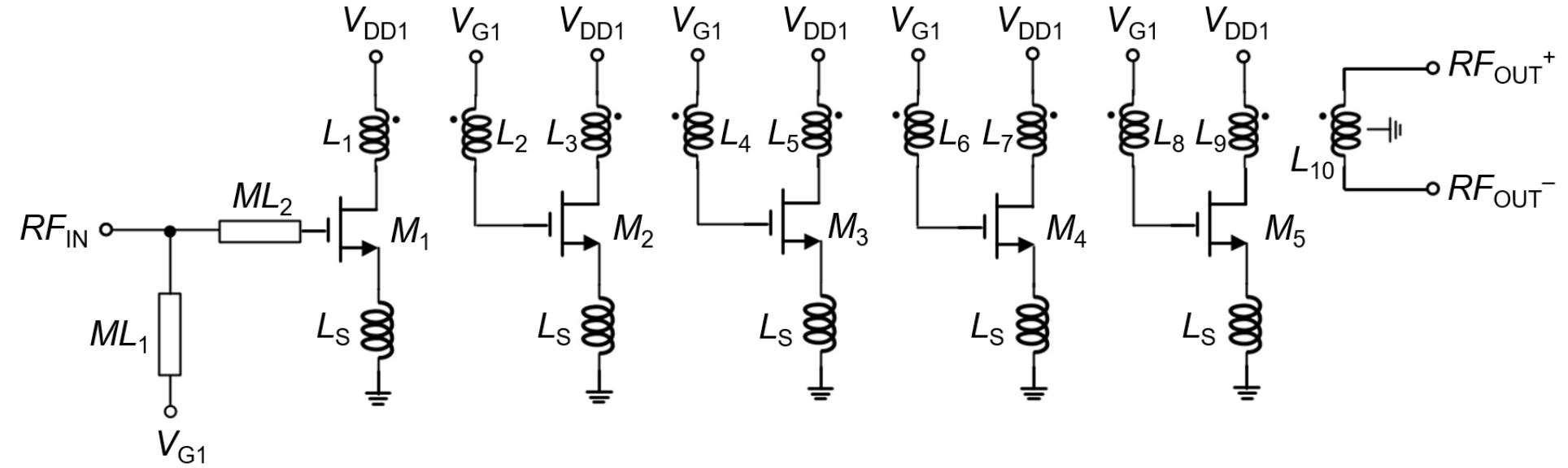
- Introduction
- Circuit design
- Chip implementation and measurement
- Conclusion

# IPD-CMOS Interconnects

- The optimization of inter-bump distance.
- Input/output return loss < -15 dB, insertion loss < 1 dB.



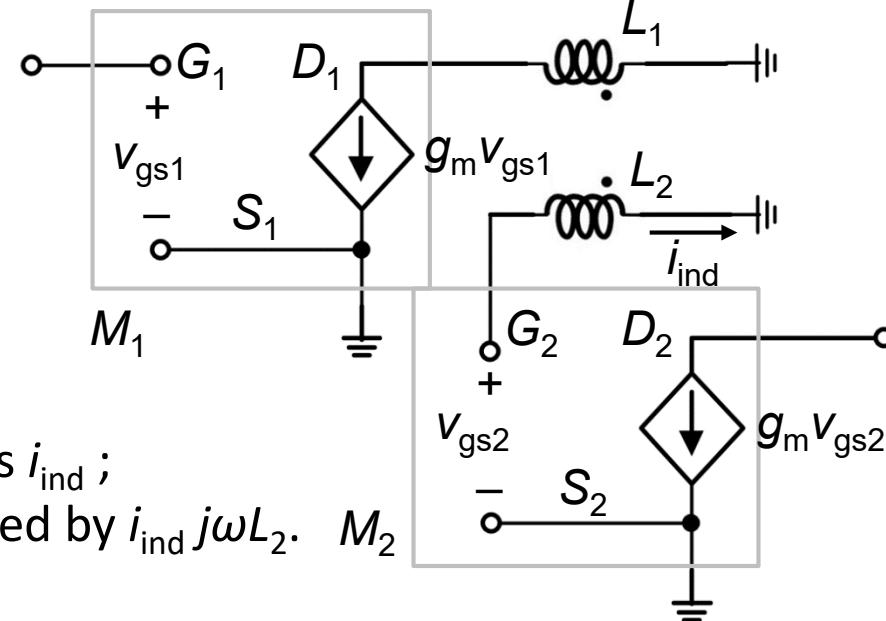
# LNA Design – Schematic



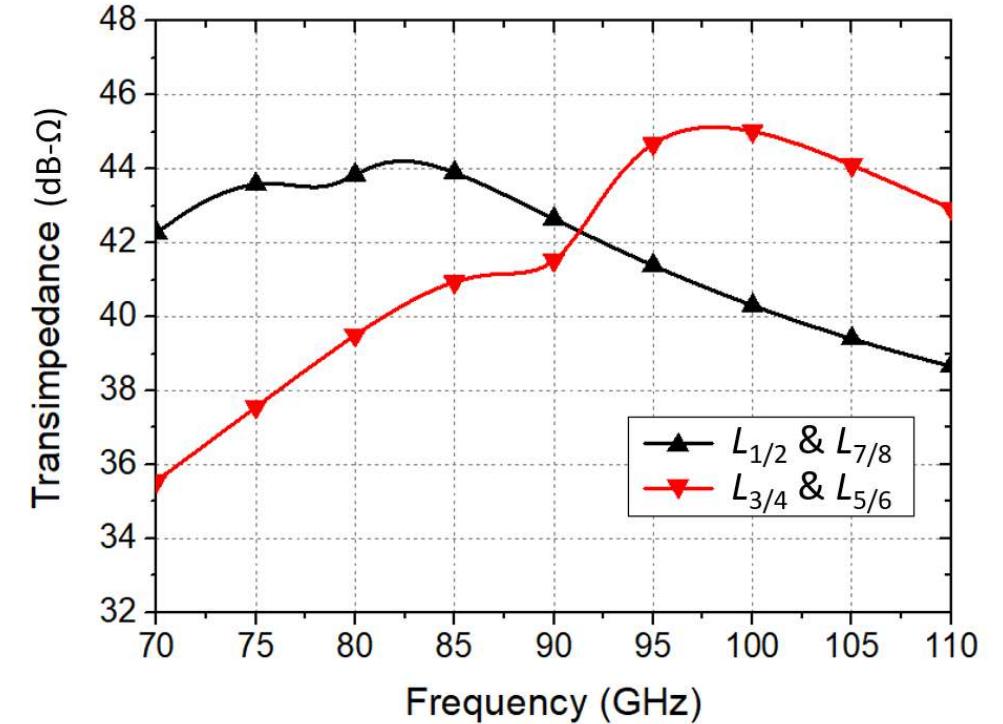
$M_{1-5}$	$2 \times 6 \mu\text{m} / 100 \text{ nm}$	$L_1/L_7 (\text{pH})$	128	$L_3/L_5 (\text{pH})$	112
$V_{G1} (\text{V})$	0.6	$L_2/L_8 (\text{pH})$	122	$L_4/L_6 (\text{pH})$	93
$V_{DD1} (\text{V})$	0.8	$k_{m,12}/k_{m,78}$	0.54	$k_{m,34}/k_{m,56}$	0.45

# LNA Design – Interstage Transformer

- Equivalent circuit model

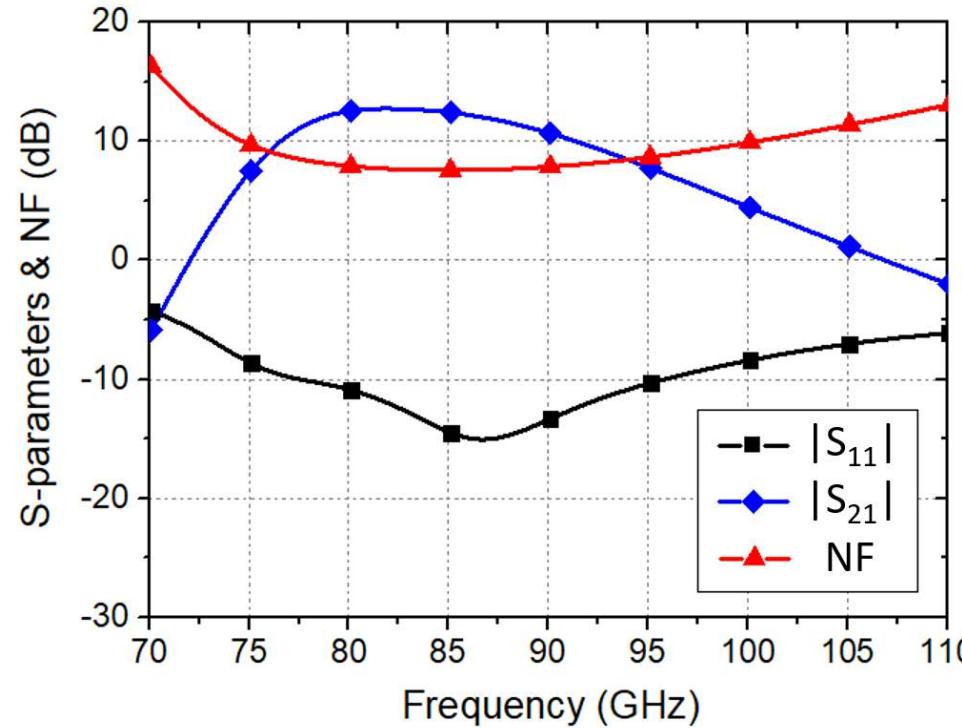


- Staggering operation frequency

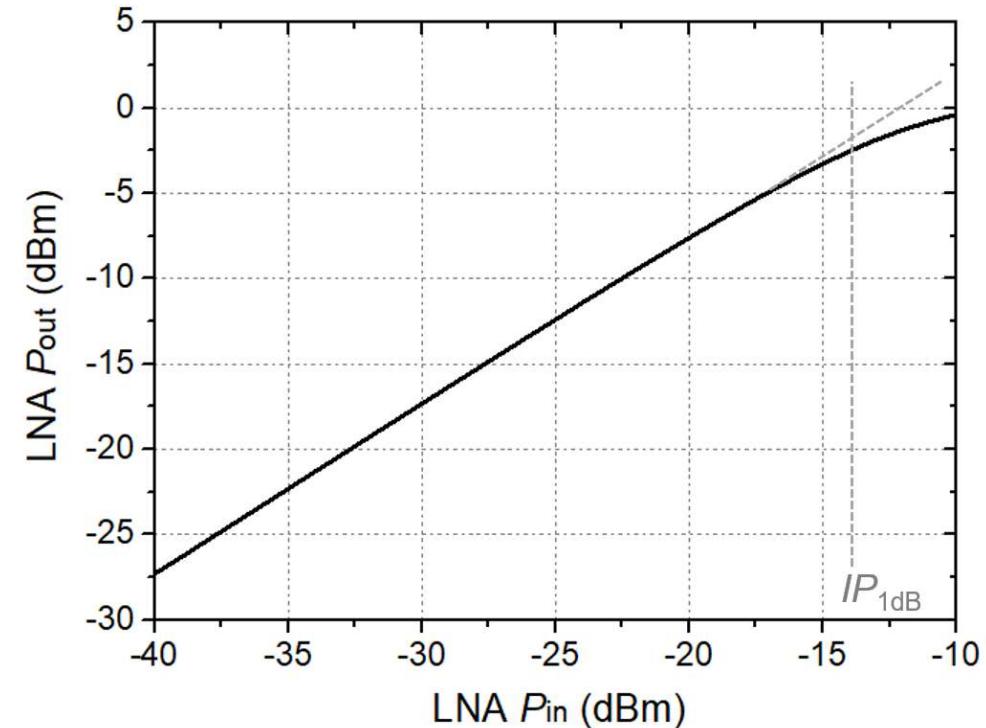


# LNA Design – Simulation Results

- S-parameters and NF



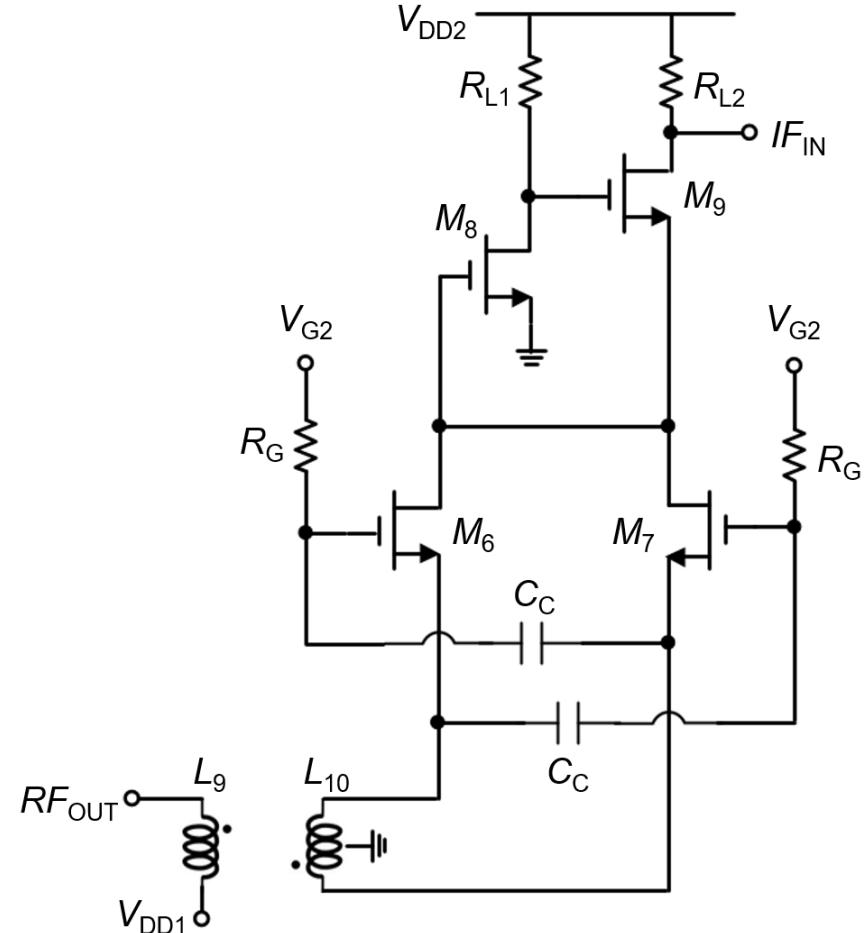
- $IP_{1dB}$



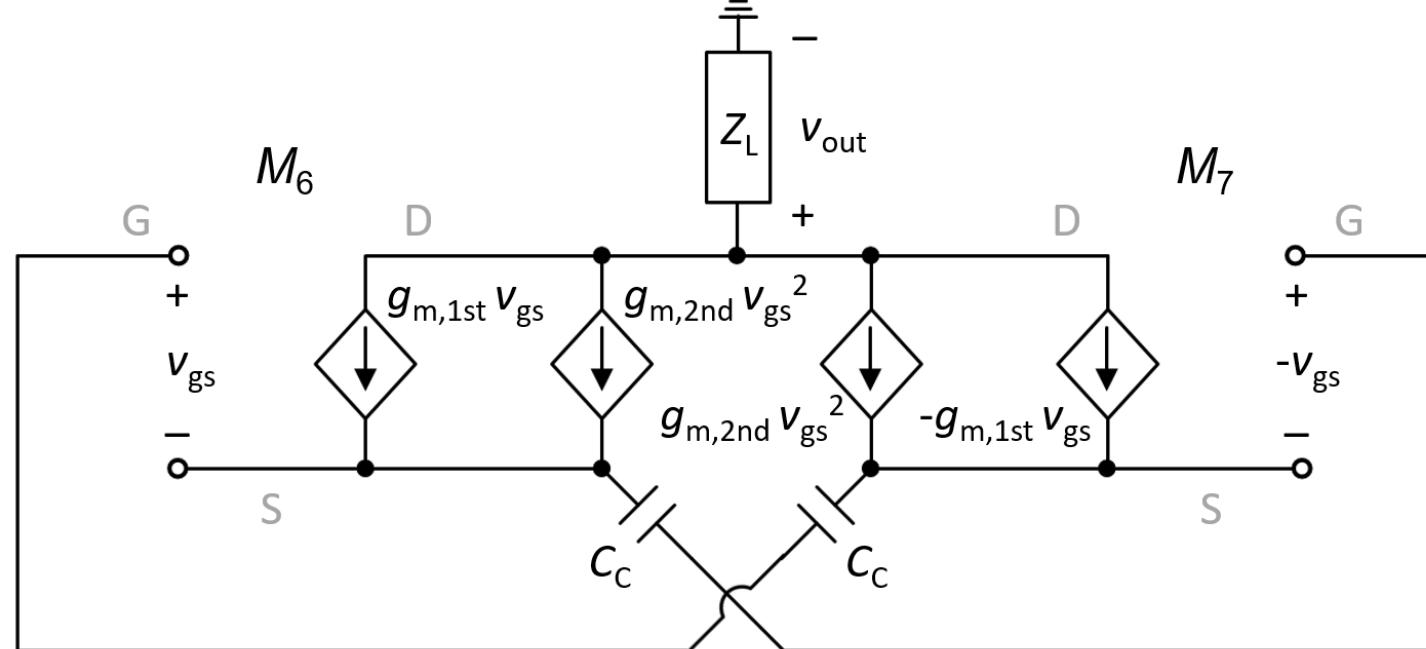
# Envelope Detector Design – Schematic

- Dual gain-boosted envelope detector

$M_{6-9}$	$2 \times 6 \mu\text{m} / 100 \text{ nm}$
$V_{G2} (\text{V})$	0.35
$V_{DD2} (\text{V})$	1.2
$C_C (\text{fF})$	45
$R_{L1} (\Omega)$	704
$R_{L2} (\Omega)$	847



# ED Design – Envelope Extraction



$$i_{D,\text{total}} = g_{m,2\text{nd}} V_{\text{RF}}^2 + g_{m,2\text{nd}} V_{\text{RF}}^2 \cos(2\omega_{\text{RF}} t)$$

$$v_{\text{out}} = -Z_L [g_{m,2\text{nd}} V_{\text{RF}}^2 + g_{m,2\text{nd}} V_{\text{RF}}^2 \cos(2\omega_{\text{RF}} t)]$$

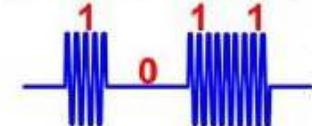
$$\text{Detected envelope offset} = Z_L (g_{m,2\text{nd}} V_{\text{RF}}^2)$$

RF input signal:

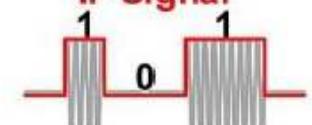
$$v_{\text{gs}} = V_{\text{RF}} \cos(\omega_{\text{RF}} t)$$

$$-v_{\text{gs}} = -V_{\text{RF}} \cos(\omega_{\text{RF}} t)$$

**Input  
(Received Signal)**



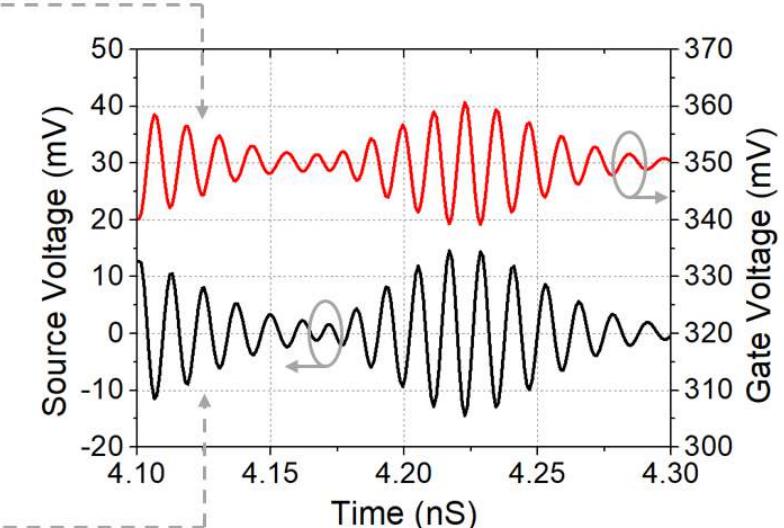
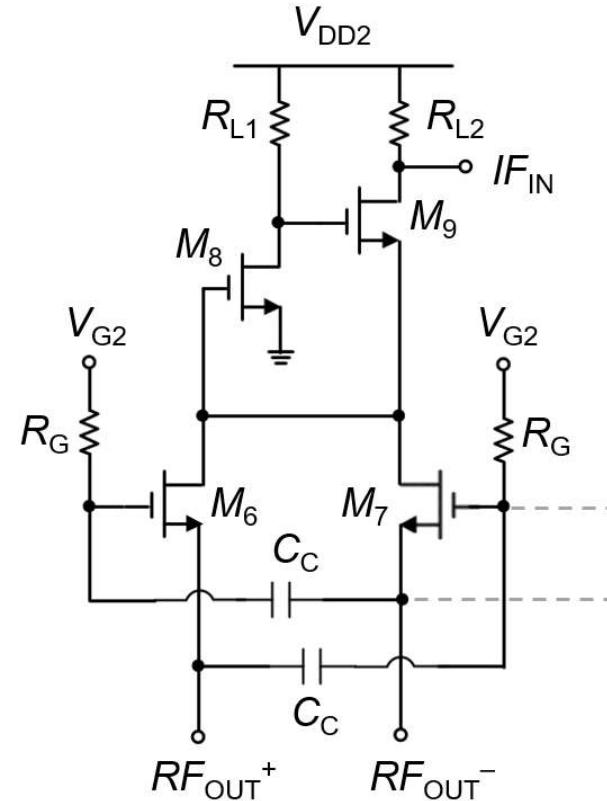
**Detected  
IF Signal**



The figure is from [9].

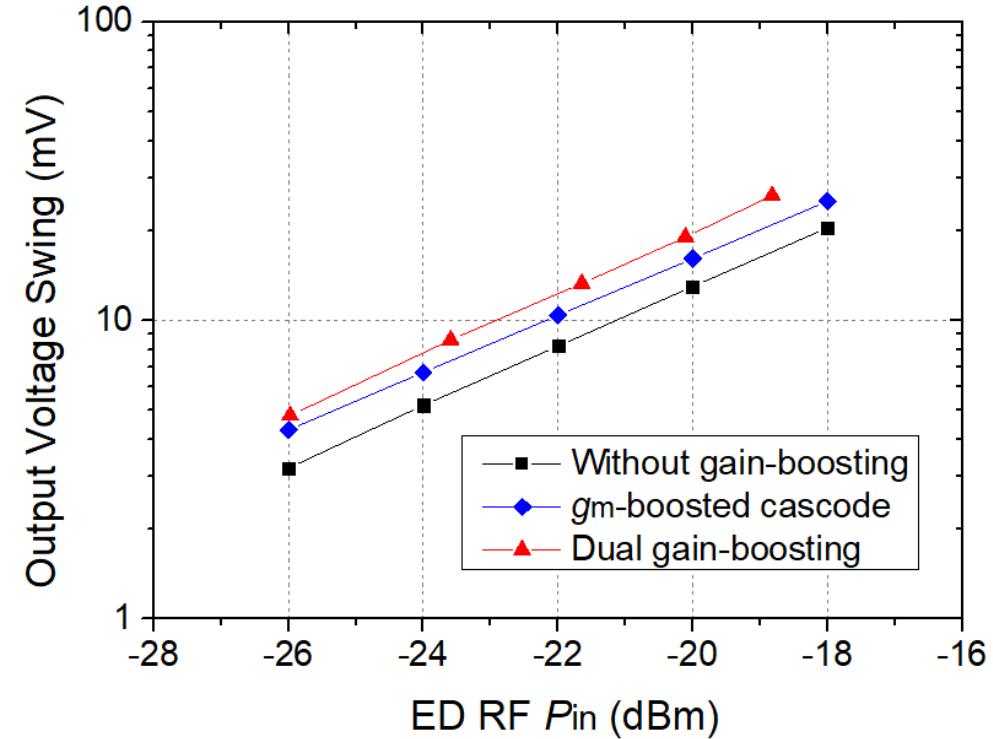
# ED Design – Transient Behavior

- To increase relative RF swing,  $C_C$  is utilized.
- Monitor transient behavior while  $C_C \downarrow$

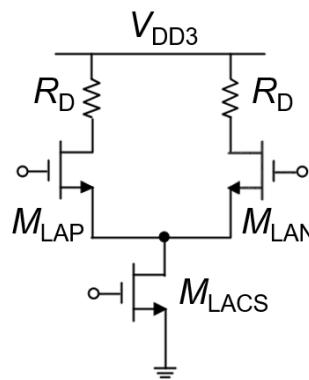
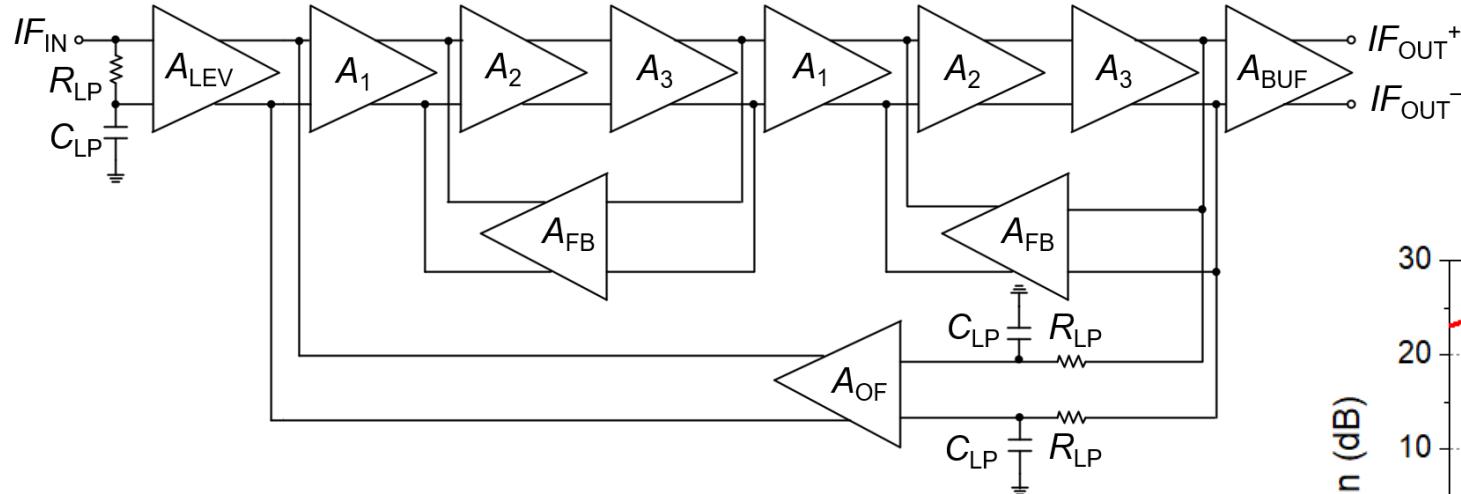


# ED Design – Responsivity

- Responsivity is improved by dual gain-boosting.

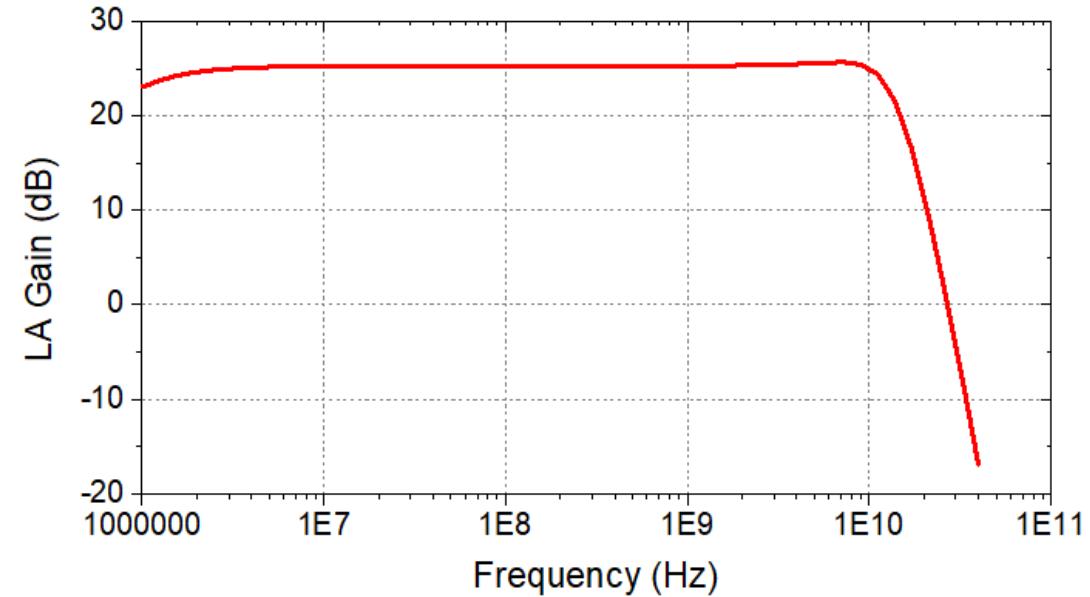


# Limiting Amplifier Design



Stage	$M_{LAP}/M_{LAN}$	$M_{LACS}$	$R_D (\Omega)$
$A_{LEV}$	$2 \times 10 \mu\text{m} / 100 \text{ nm}$	$2 \times 36 \mu\text{m} / 200 \text{ nm}$	123
$A_1$	$4 \times 6 \mu\text{m} / 100 \text{ nm}$	$4 \times 22 \mu\text{m} / 200 \text{ nm}$	117
$A_2/A_3$	$4 \times 8 \mu\text{m} / 100 \text{ nm}$	$4 \times 22 \mu\text{m} / 200 \text{ nm}$	131
$A_{BUF}$	$4 \times 8 \mu\text{m} / 100 \text{ nm}$	$4 \times 22 \mu\text{m} / 200 \text{ nm}$	105
$A_{FB}$	$1.5 \times 2 \mu\text{m} / 100 \text{ nm}$	$2 \times 6 \mu\text{m} / 200 \text{ nm}$	N/A
$A_{OF}$	$2 \times 3 \mu\text{m} / 100 \text{ nm}$	$2 \times 12 \mu\text{m} / 200 \text{ nm}$	N/A

$V_{G3}$  0.5 V,  $V_{DD3}$  1.2 V,  $R_{LP}$  74 k $\Omega$ ,  $C_{LP}$  5 pF

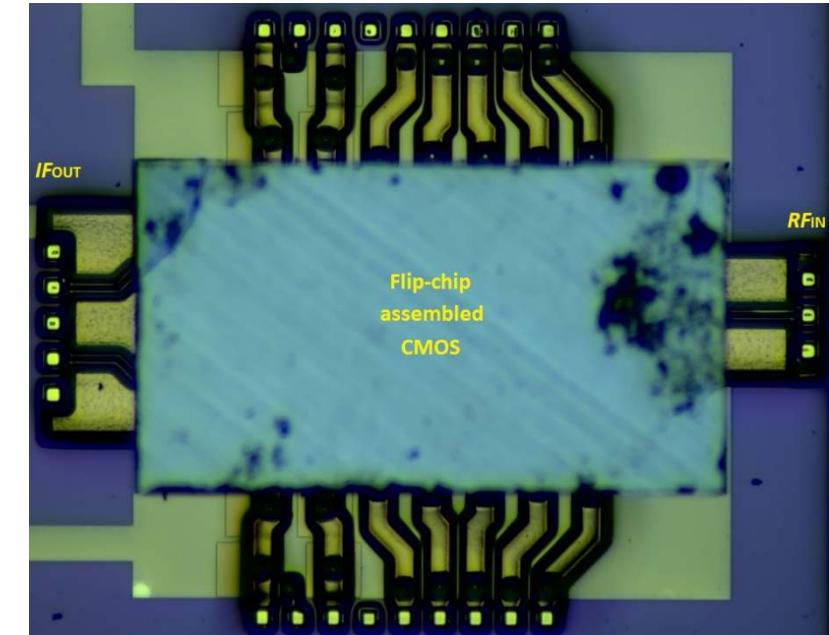
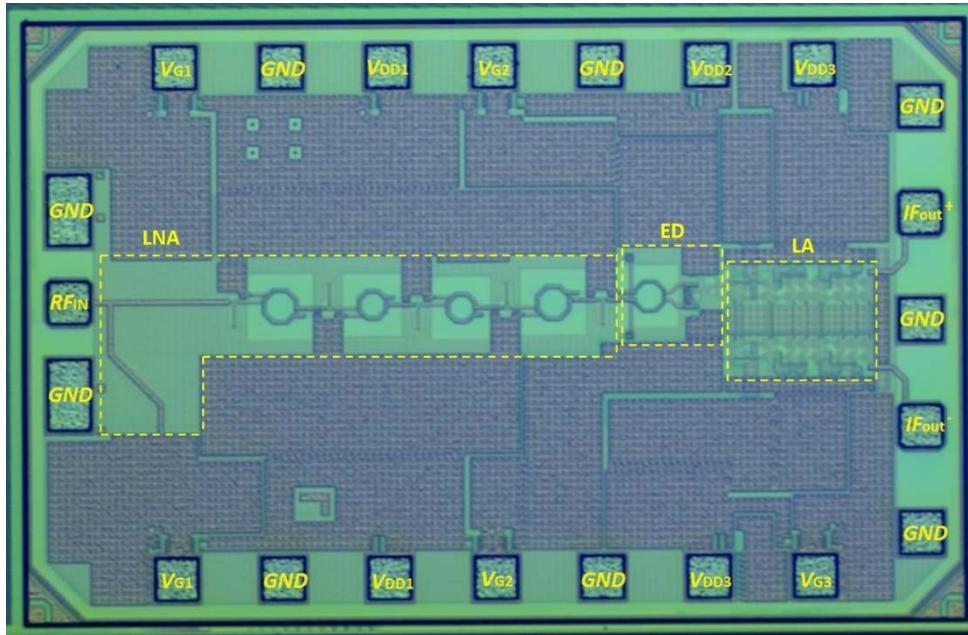


# Outline

- Introduction
- Circuit design
- Chip implementation and measurement
- Conclusion

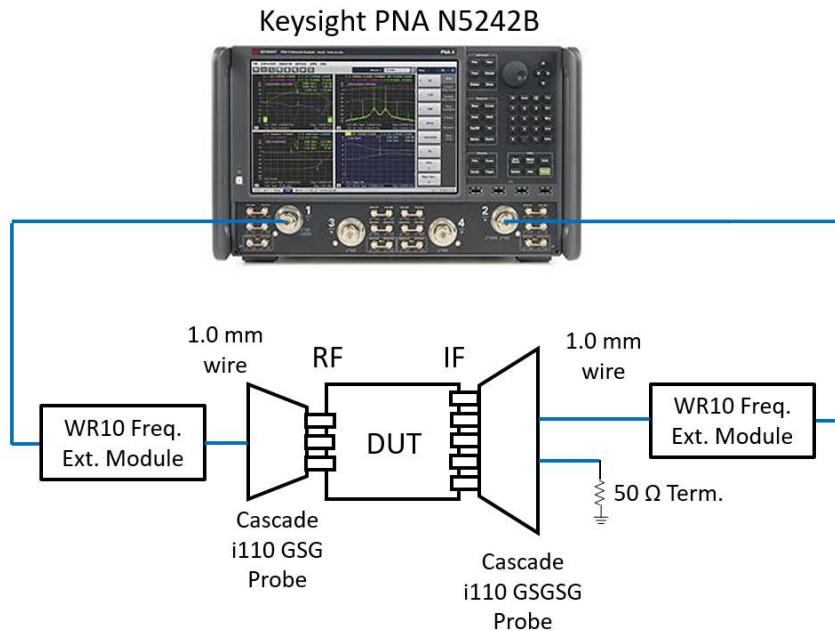
# Chip Implementation

- The OOK receiver is implemented in 90-nm CMOS and flip-chip assembled onto IPD carrier.

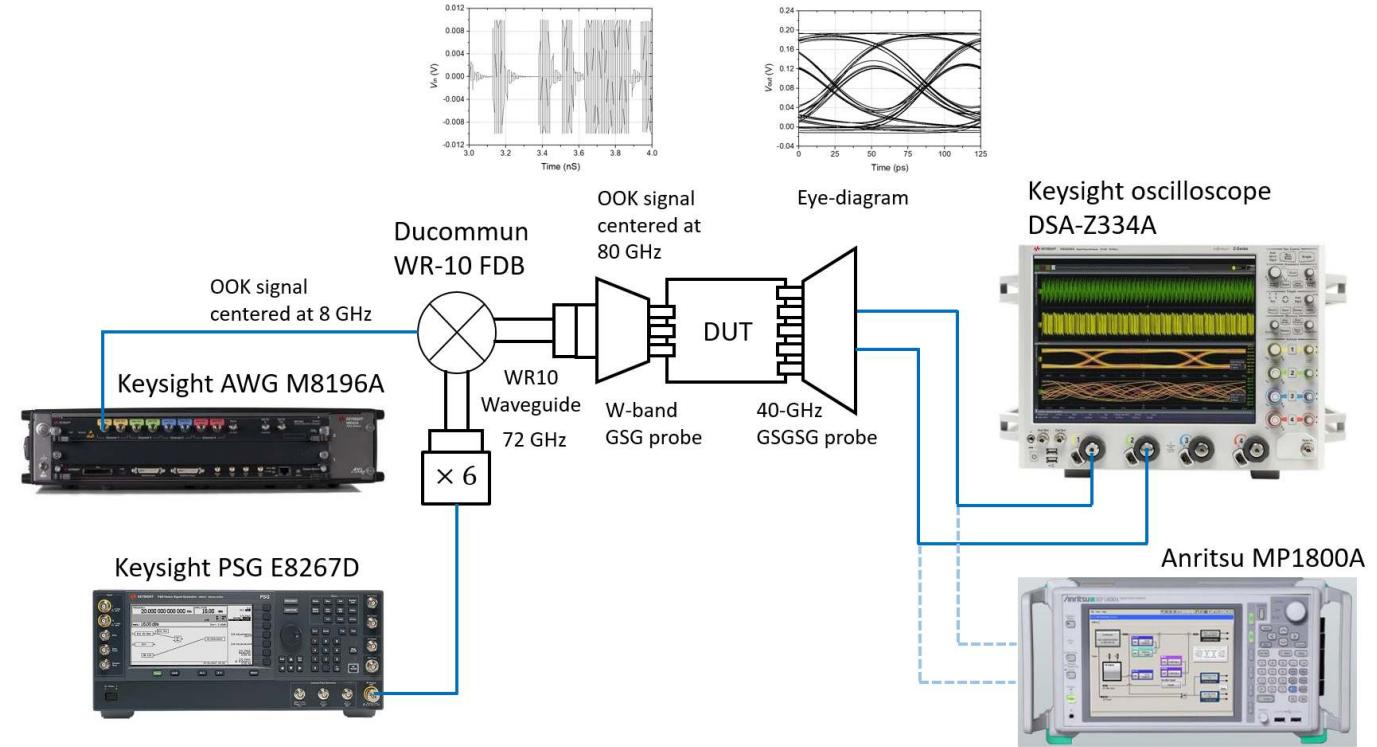


# Measurement Setup

- Setup of S-parameter measurement.

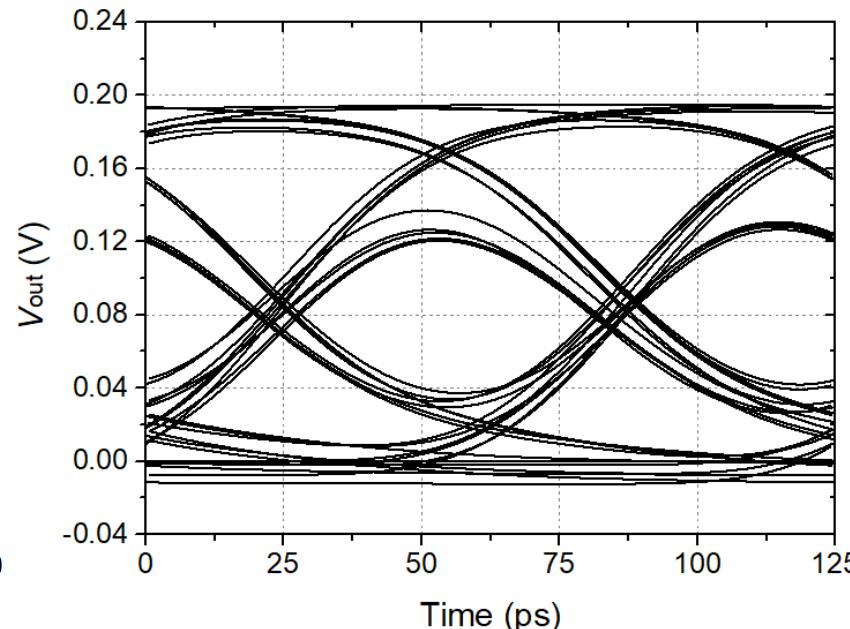
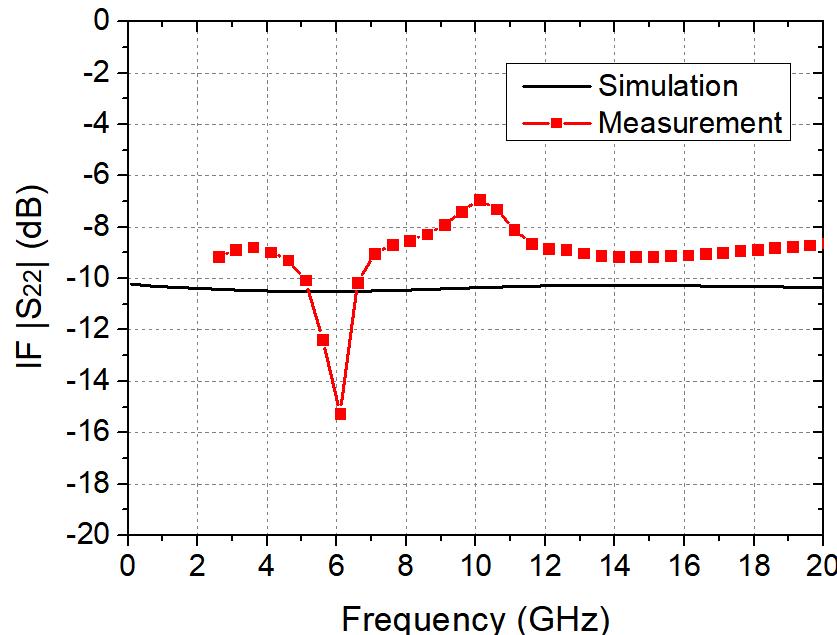
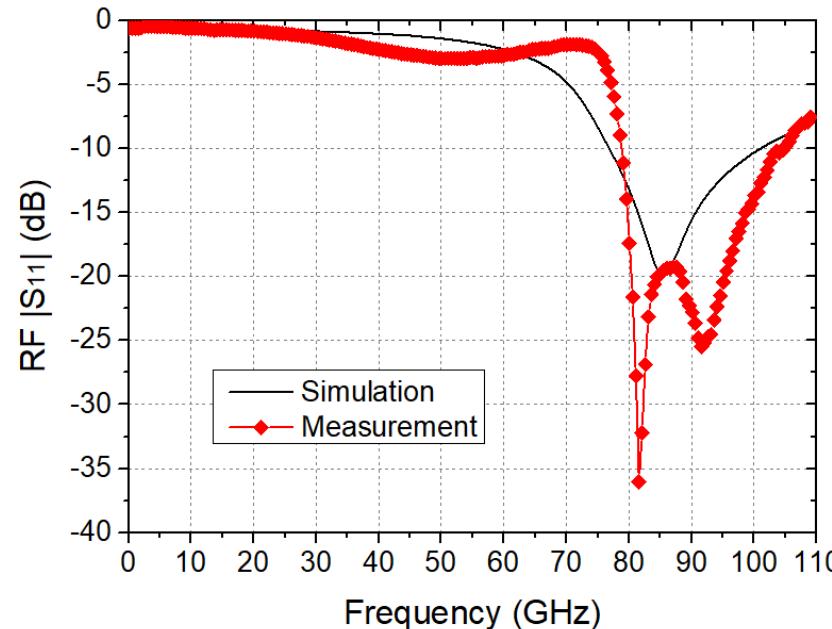


- Setup for OOK signal measurement



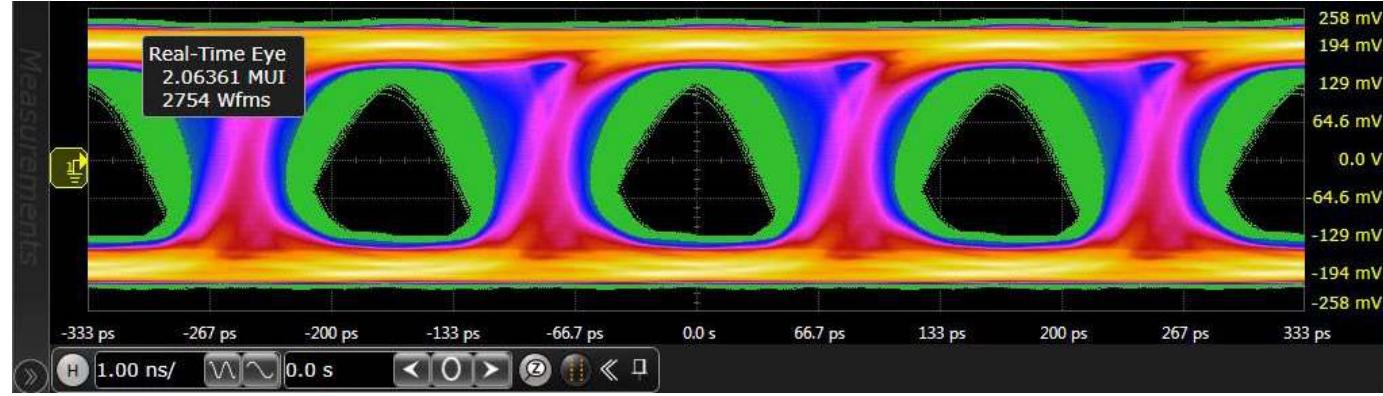
# Measurement and Simulation Results

- Reflection coefficients measurement at RF ( $|S_{11}|$ ) and IF ( $|S_{22}|$ ).
- Simulated OOK Eye-diagram for 16 Gb/s

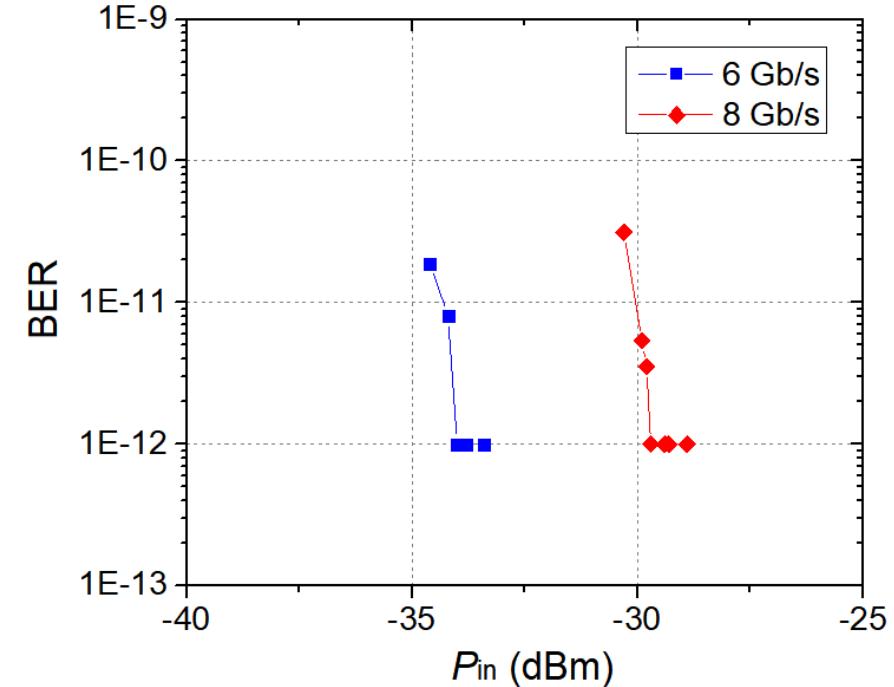
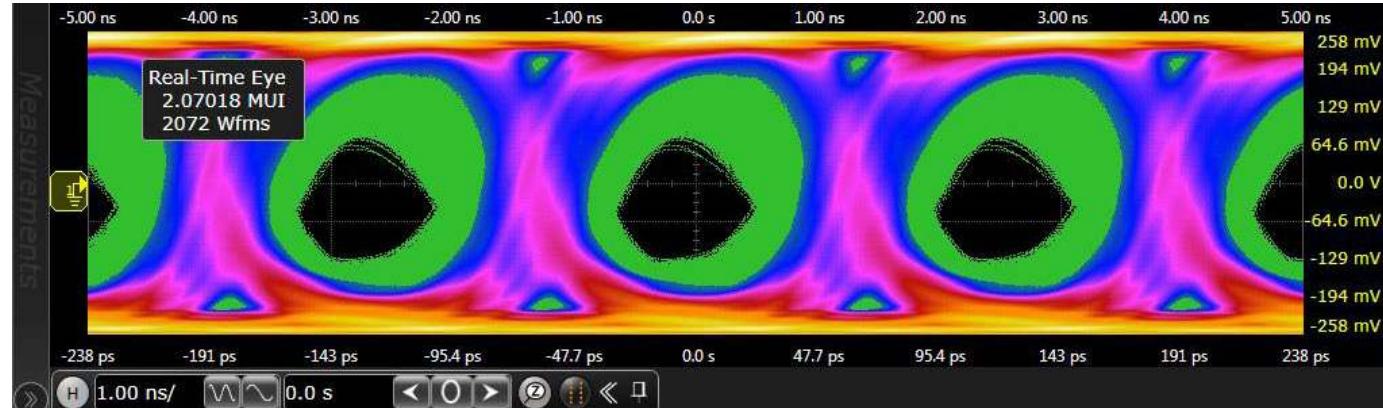


# OOK Measurement Results

6 Gb/s



8 Gb/s



# Comparison Table

Ref.	Frequency (GHz)	Technology (all CMOS)	Integration	Modulation	PRBS	Data rate (Gb/s)	BER	Sensitivity (dBm)	P <sub>DC</sub> (mW)	Energy per bit (pJ/bit)
This work	80	90-nm	IPD carrier / LNA / ED / LA	OOK	$2^7 - 1$	8	$10^{-12}$	-29.7	53.3	6.66
[1]	120	28-nm	Dielectric fiber / ED / LA	OOK	N/A	4	$10^{-12}$	-20	25.1	6.28
[2]	80 / 100	65-nm	Antenna / LNA / ED / LA	OOK	$2^7 - 1 / 2^{31} - 1$	23	$10^{-11}$	-23.6 / -25.6	153.7	6.68
[6]	60	65-nm	LNA / ED / LA	BPOOK	$2^7 - 1$	3	$10^{-7}$	-43	22	7.33
[7]	140	65-nm	Pre-amplifier / ED	OOK	$2^9 - 1$	10	N/A	N/A	32.5	3.25
[8]	60	90-nm	Antenna / LNA / ED / LA	OOK	$2^7 - 1$	10.7	$10^{-12}$	-32.5	36	3.36

# Outline

- Introduction
- Circuit design
- Chip implementation and measurement
- Conclusion

# Conclusion

- A flip-chip assembled W-band OOK RX is demonstrated for high-speed wireline/wireless communication.
- An OOK data rate of 8 Gb/s is measured with a sensitivity of -29.7 dBm at a standard BER  $10^{-12}$ .

# Acknowledgment

This work is supported by the Ministry of Science and Technology, Taiwan (MOST 110-2221-E-007-123 and MOST 110-2224-E-007-005). The authors thank Taiwan Semiconductor Research Institute for chip fabrication and measurement.

# Reference

- [1] S. Ooms and P. Reynaert, "Design and packaging of a robust 120-GHz OOK receiver used in a short-range dielectric fiber link," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 42-45, 2020.
- [2] K. Nakajima et al., "23Gbps 9.4pJ/bit 80/100GHz band CMOS transceiver with on-board antenna for short-range communication," in *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2014, pp. 173-176.
- [3] X. Yu et al., "An 18.7-Gb/s 60-GHz OOK demodulator in 65-nm CMOS for wireless network-on-Chip," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 799-806, March 2015.
- [4] G. Feng et al., "An 88.5–110 GHz CMOS low-noise amplifier for millimeter-wave imaging applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 2, pp. 134-136, Feb. 2016.
- [5] "NRZ bandwidth (-3 dB HF cutoff vs SNR) how much bandwidth is enough," Mindspeed technologies, Newport Beach, California, USA. [Online]. Available: <https://cdn.macom.com/whitepapers/02XXX-WTP-001-A.pdf>
- [6] Y. Wang et al., "A 60-GHz 3.0-Gb/s spectrum efficient BPOOK transceiver for low-power short-range wireless in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1363-1374, May 2019.
- [7] B. Suh, H. Lee, S. Kim, and S. Jeon, "A D-Band multiplier-based OOK transceiver with supplementary transistor modeling in 65-nm bulk CMOS technology," *IEEE Access*, vol. 7, pp. 7783-7793, 2019.
- [8] C. W. Byeon, C. H. Yoon, and C. S. Park, "A 67-mW 10.7-Gb/s 60-GHz OOK CMOS transceiver for short range wireless communications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3391–3401, Aug. 2013.
- [9] S. Moghadami, F. Hajilou, P. Agrawal and S. Ardalani, "A 210 GHz fully-integrated OOK transceiver for short-range wireless chip-to-chip communication in 40 nm CMOS technology," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 5, pp. 737-741, Sept. 2015.