Tu01D-4

A 74.8-88.8 GHz Wideband CMOS LNA Achieving +4.73 dBm OP1dB and 6.39 dB Minimum NF

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Outline

- Motivation and Challenges
- Wideband LNA in 55nm CMOS
- Measurement Results
- Conclusions

Motivation

- Broadband mmWave transceivers are needed to support 5G and beyond high data-rate wireless communication and high-resolution wireless sensing applications
- Nanoscale CMOS is attractive offering high integration density, cost-efficient and high-yield solutions
- LNA plays an important role in defining the receiver noise figure (NF) and bandwidth (BW)

Challenges and Proposed Solutions

- Challenging to simultaneously achieve NF, BW, linearity and area efficiency
  - Wide bandwidth is achieved at the expense of a large die area and severe passive network loss
  - Transmitter leakage and isolation between antennas degrade linearity
  - Broadband input matching limits the noise performance
- Proposed solutions
  - Hybrid broadband inter-stage network for wide BW
  - Inductor-feedback common-gate-shorting for high gain and high OP1dB
  - Out-of-phase-dual-coupling for low noise and high gain

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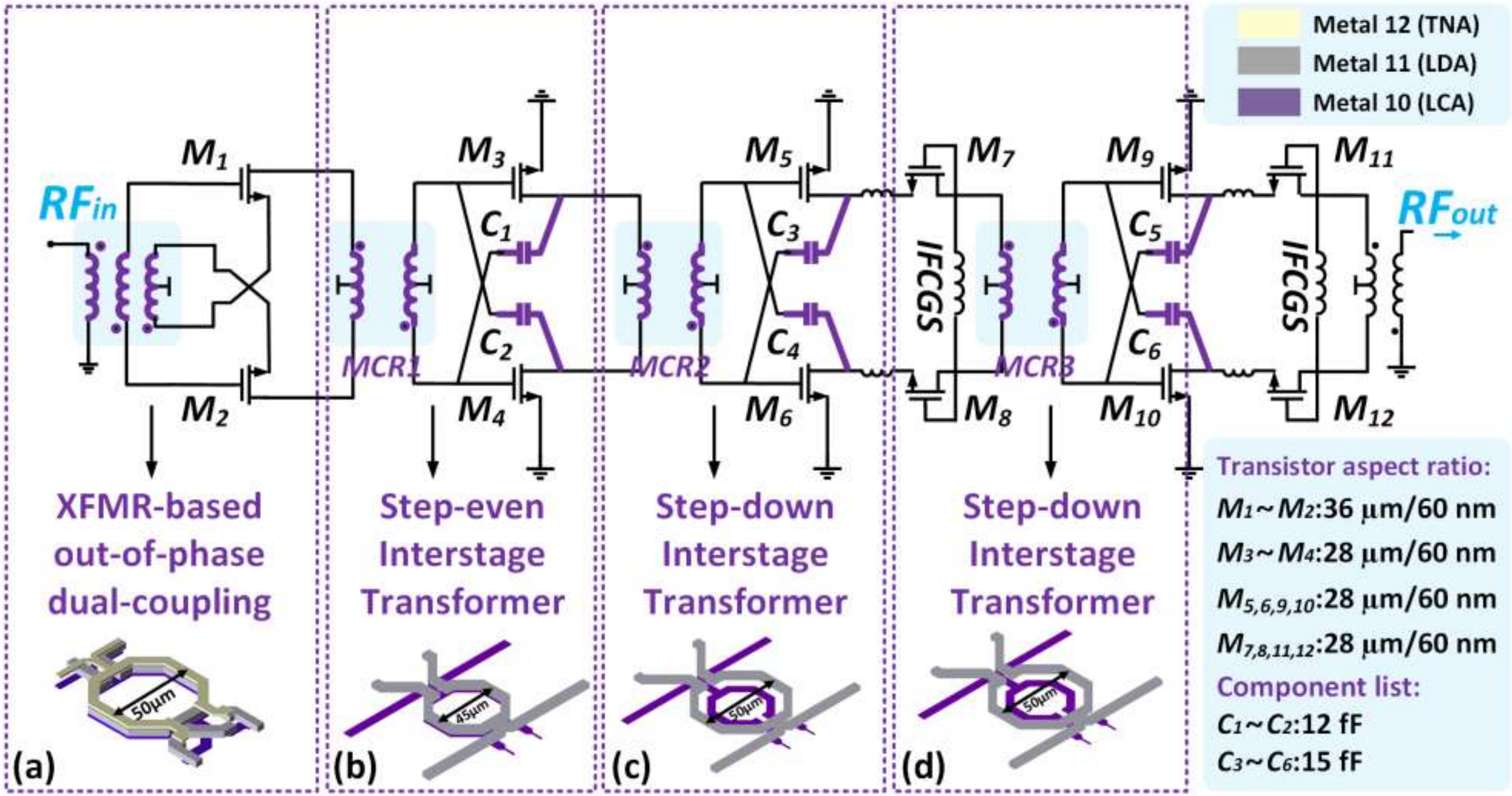
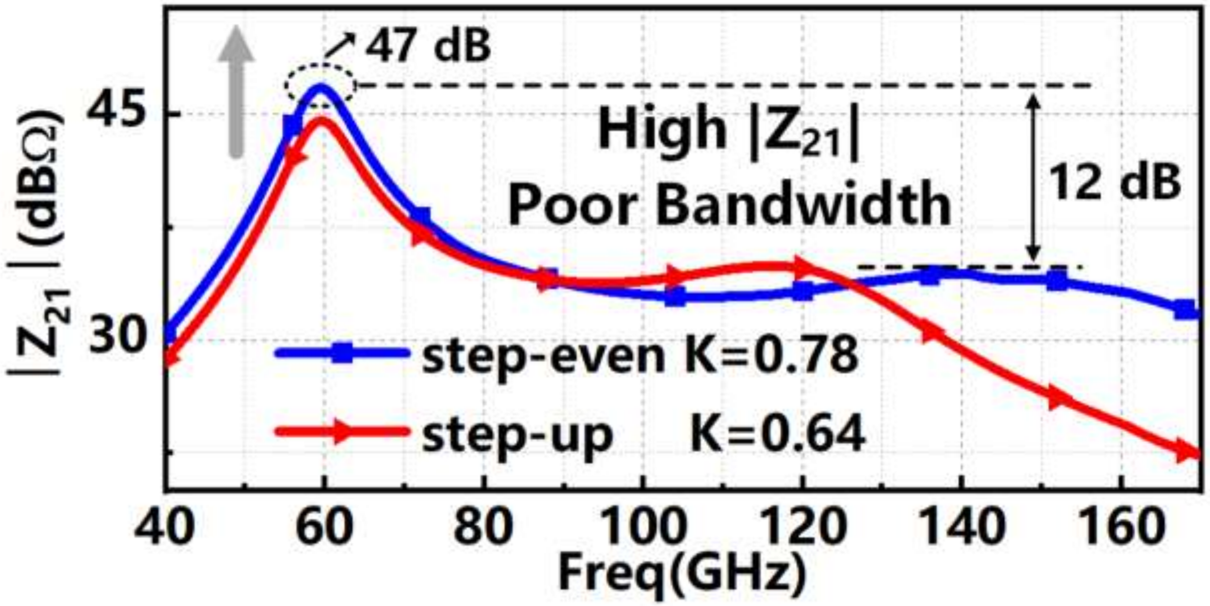
74.8-88.8 GHz CMOS LNA

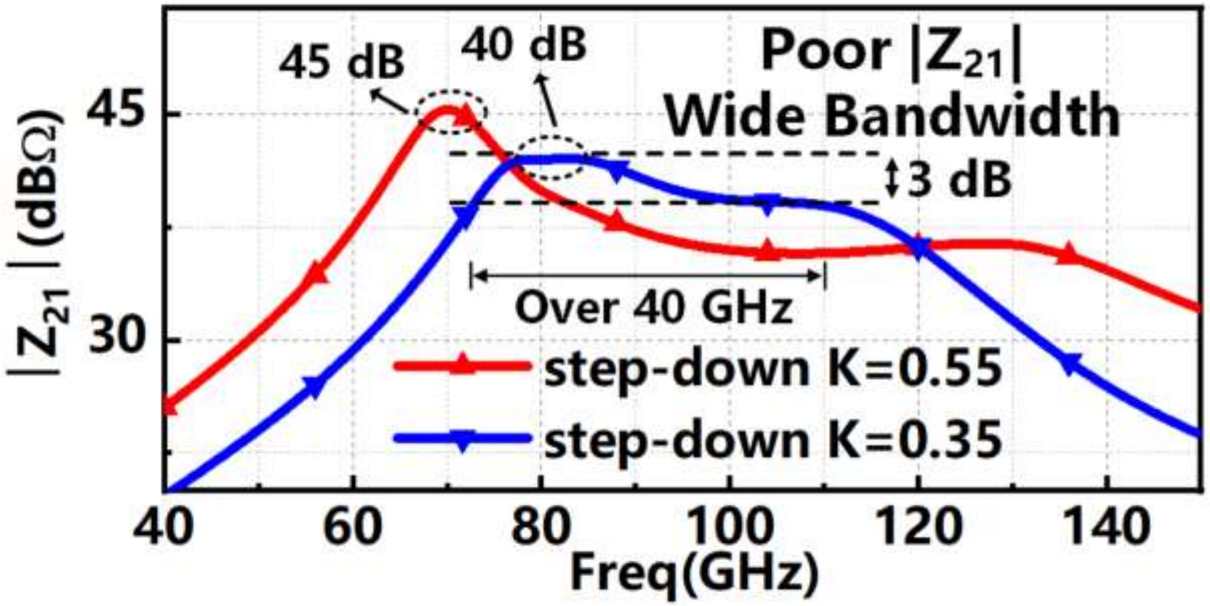


4 stage : 1 CG+1 CS+2 Cascode, differential topology, single-ended input and output

Hybrid Broadband Interstage Network (HBIN) for Wide Bandwidth

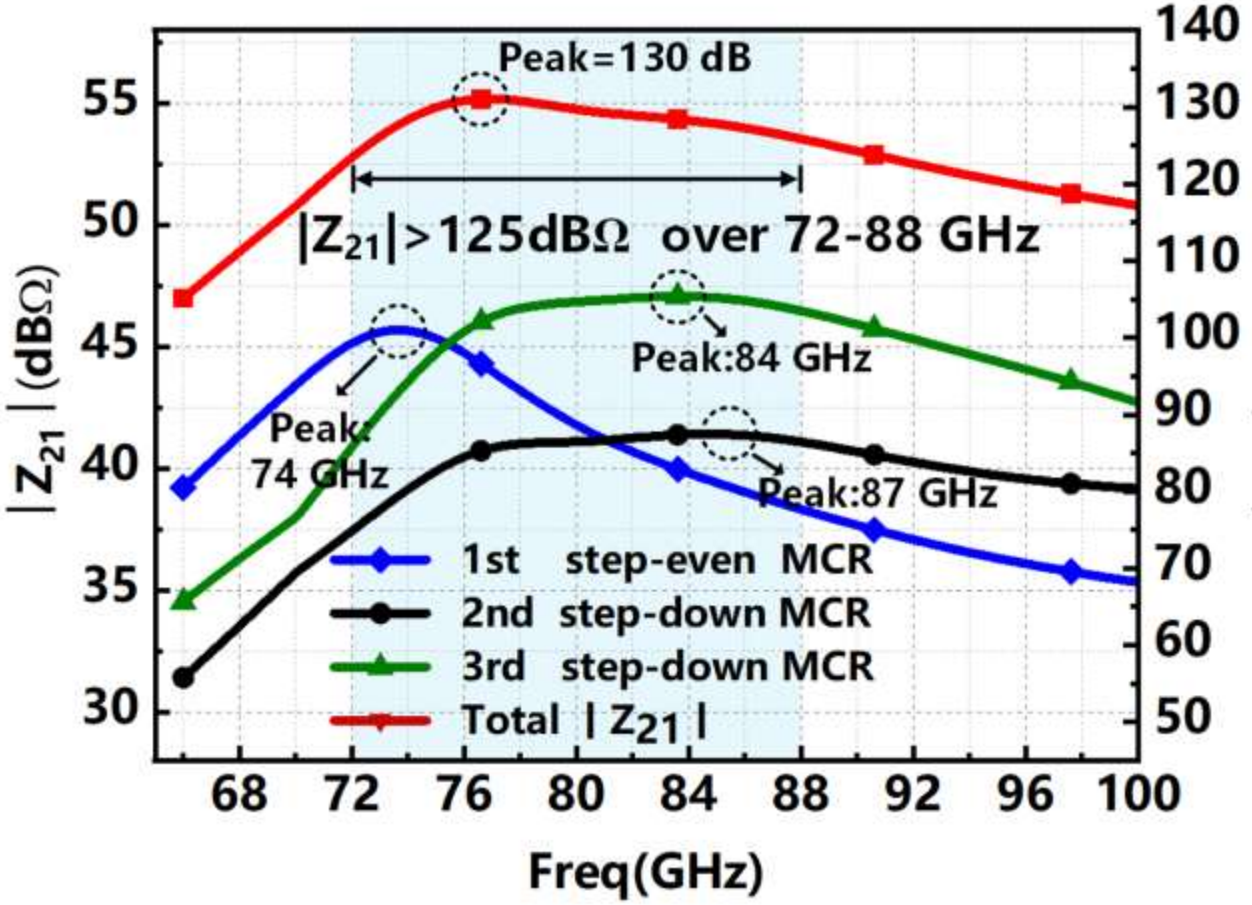


(a) $|Z_{21}|$ of step-even/up transformer

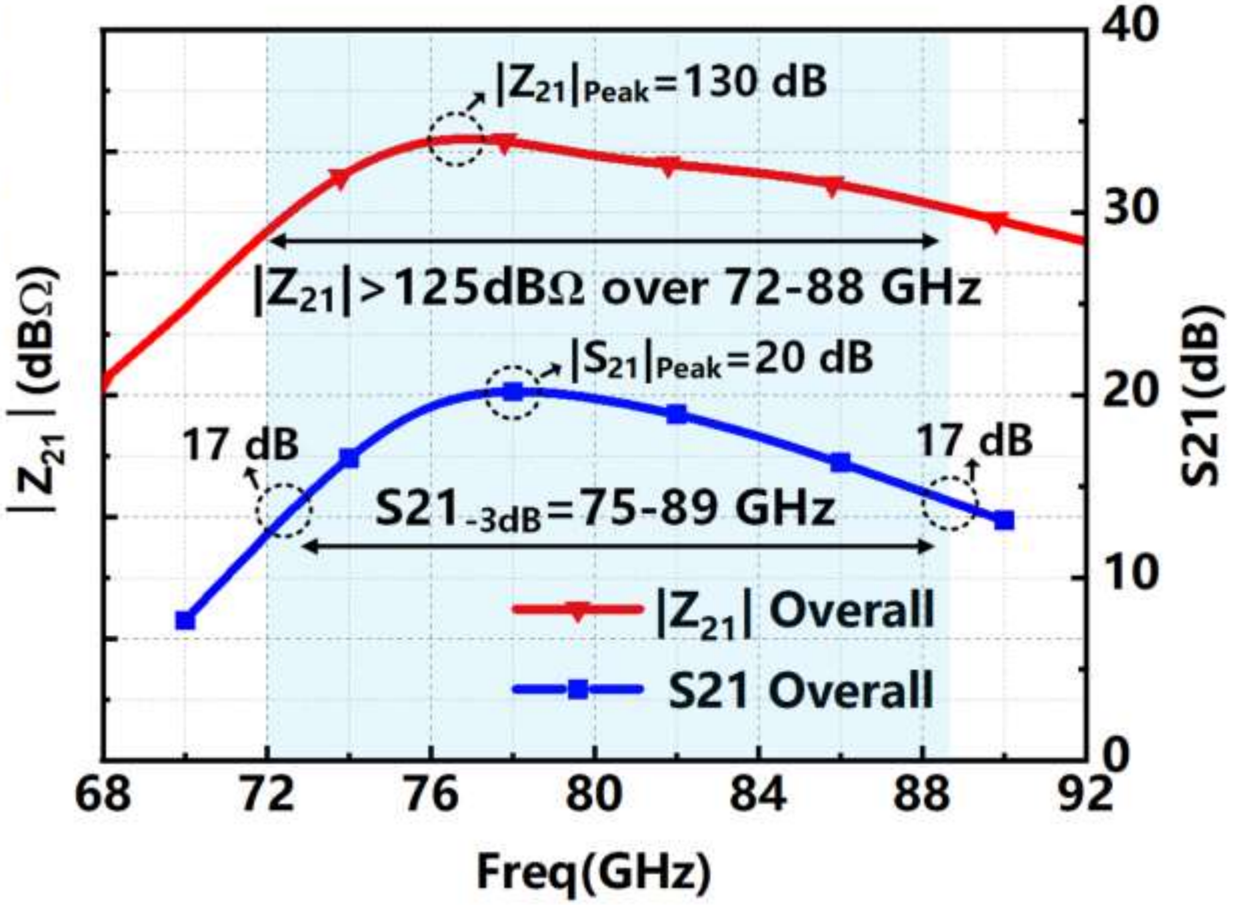


(b) $|Z_{21}|$ of step-down transformer

Simulation Results of HBIN

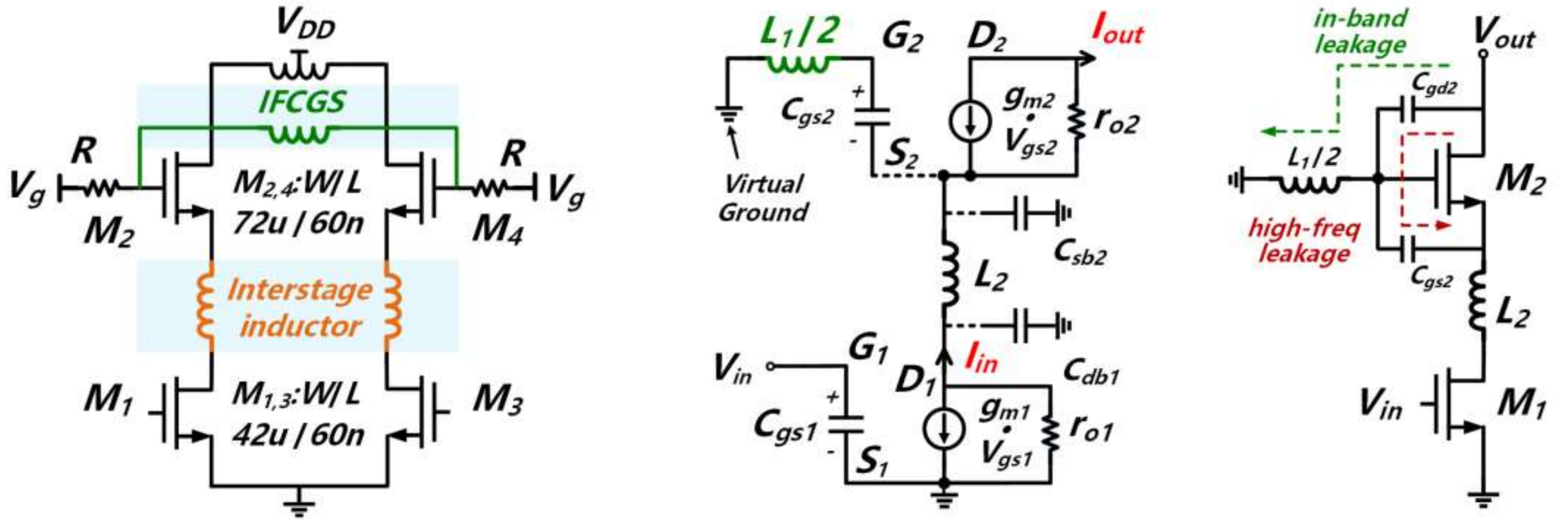


(a) $|Z_{21}|$ of Interstage Coupling network



(b) Comparison of Overall S_{21} and $|Z_{21}|$

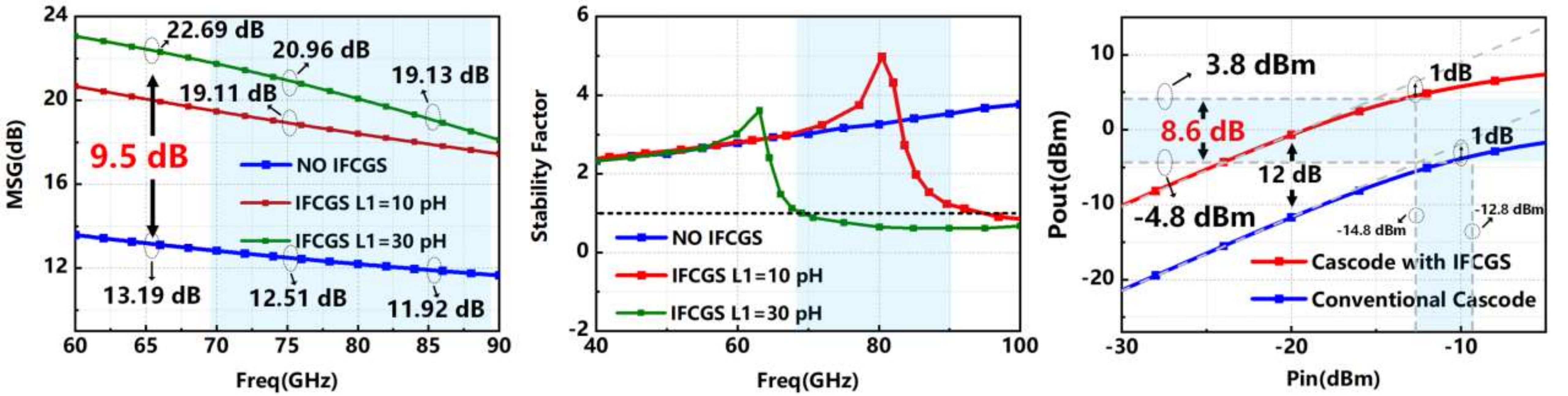
Inductor-Feedback Common-Gate-Shorting (IFCGS) for High Gain and High OP1dB



(a) IFCGS circuit (b) Equivalent circuit (c) Leakage analysis

$$I_{out} \approx I_{in} \cdot \frac{g_m}{\left\{ g_m + s\left[C_{sb2}\left(1 - \omega^2 \frac{L_1}{2} C_{gs2}\right) + C_{gs2} \right] \right\}}$$

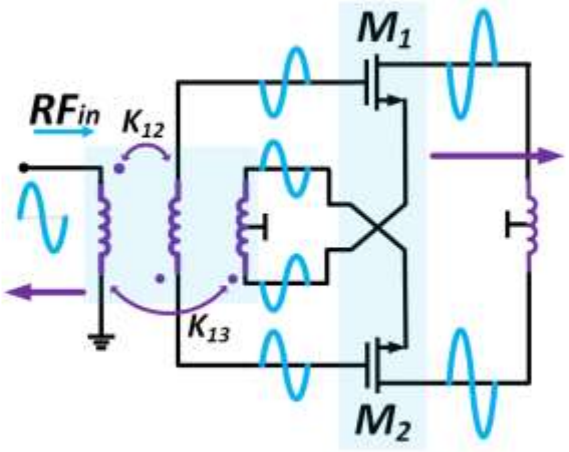
Simulation Results of IFCGS



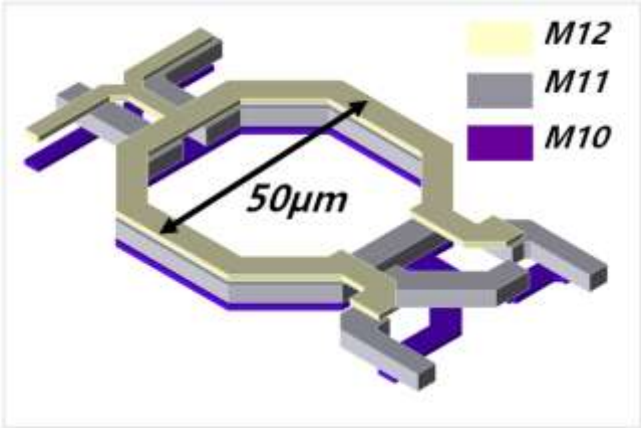
(a) MSG simulation (b) Stability simulation (c) OP1dB simulation

L1=10 pH, MSG improved by 9.5 dB, OP1dB improved by 8.6 dB

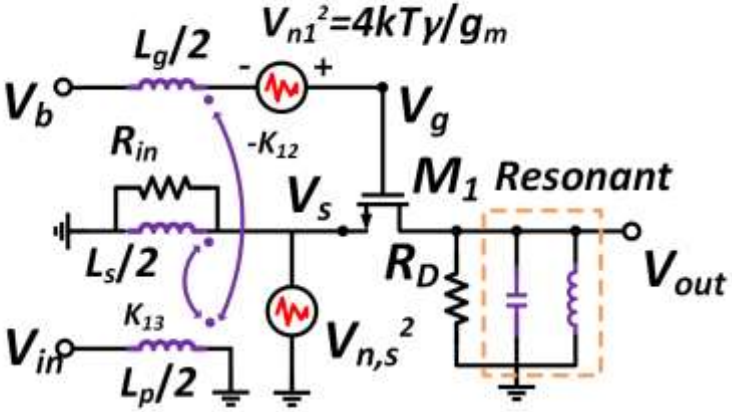
Out-of-Phase-Dual-Coupling (OPDC) for Low Noise and High Gain



(a) OPDC CG circuit



(b) Input balun



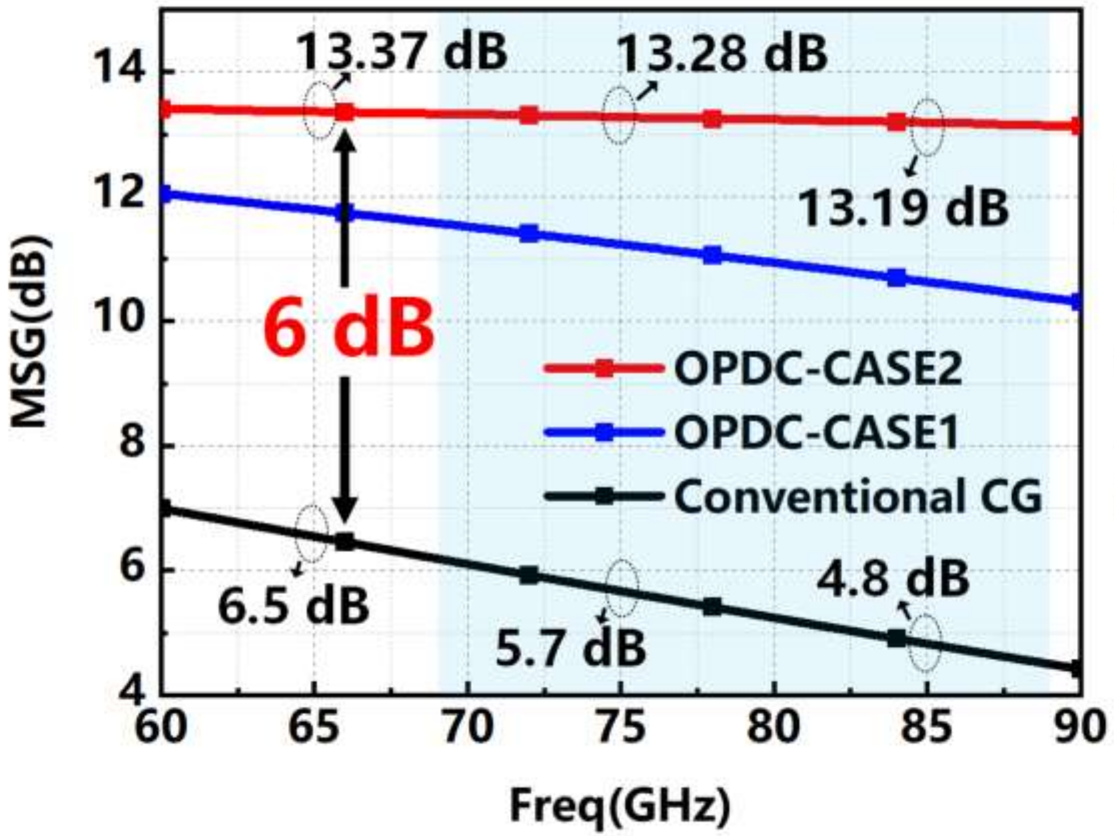
(c) Equivalent circuit

voltage gain: $$\frac{V_{out}}{V_{in}} = (n_g K_{12} + n_s K_{13})\, g_m R_D$$

Noise figure: $$NF = 1 + \frac{\gamma}{(n_g K_{12} + n_s K_{13})} + \frac{4}{(n_g K_{12} + n_s K_{13})\, g_m R_D}$$

Simulation Results of OPDC

CASE1: K_{12}=0.65 K_{13}=0.67 L_g=129pH L_s=180pH
CASE2: K_{12}=0.73 K_{13}=0.74 L_g=129pH L_s=136pH



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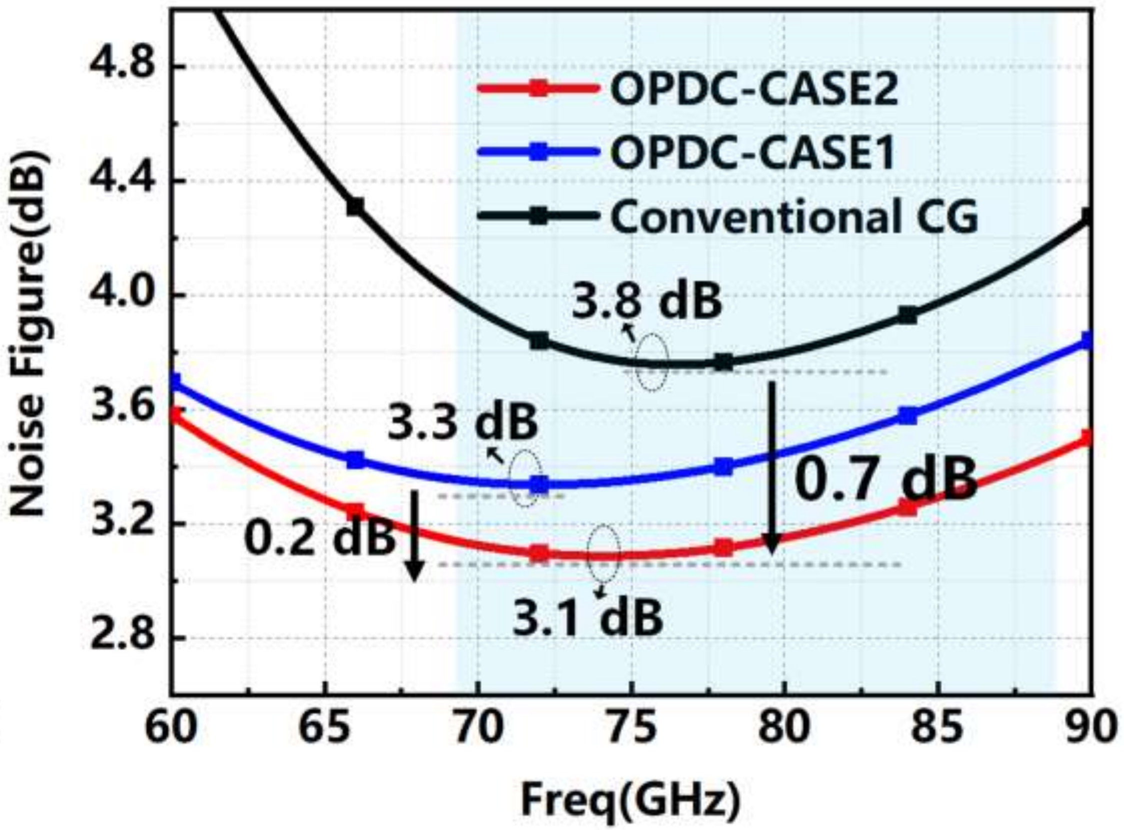

In CASE2, MSG improved by 6 dB, NF decreased by 0.7 dB

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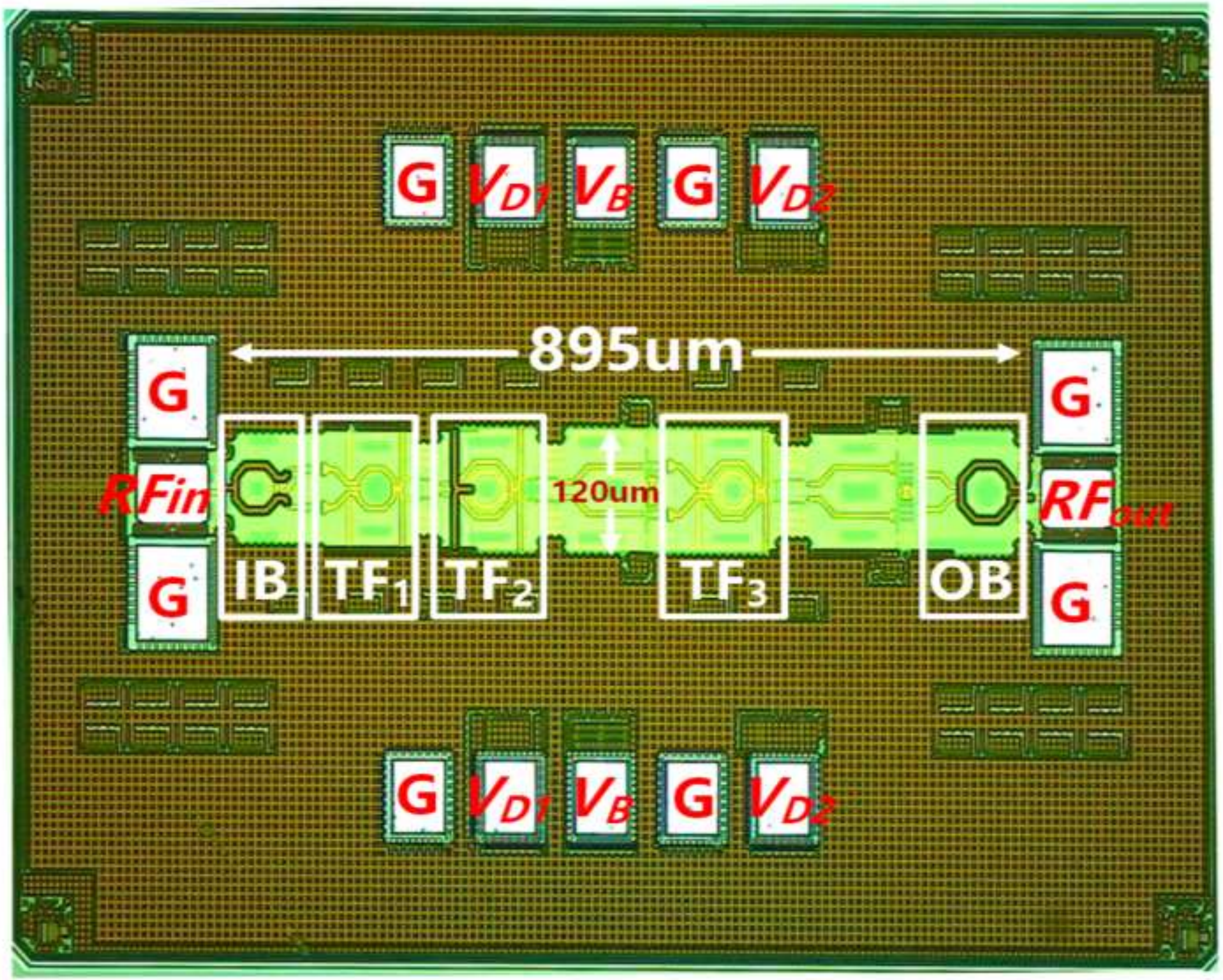
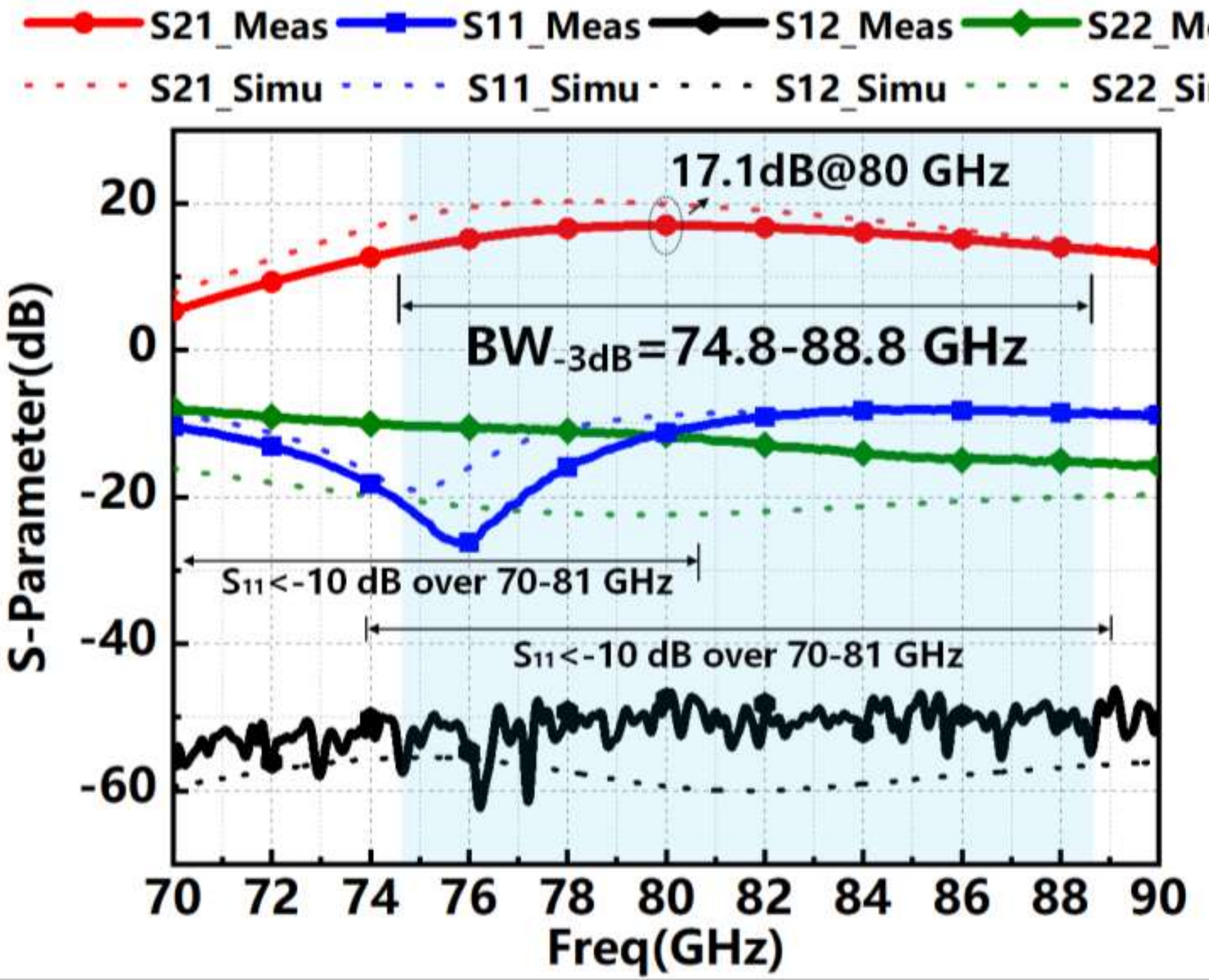
Die Photo of the Proposed LNA

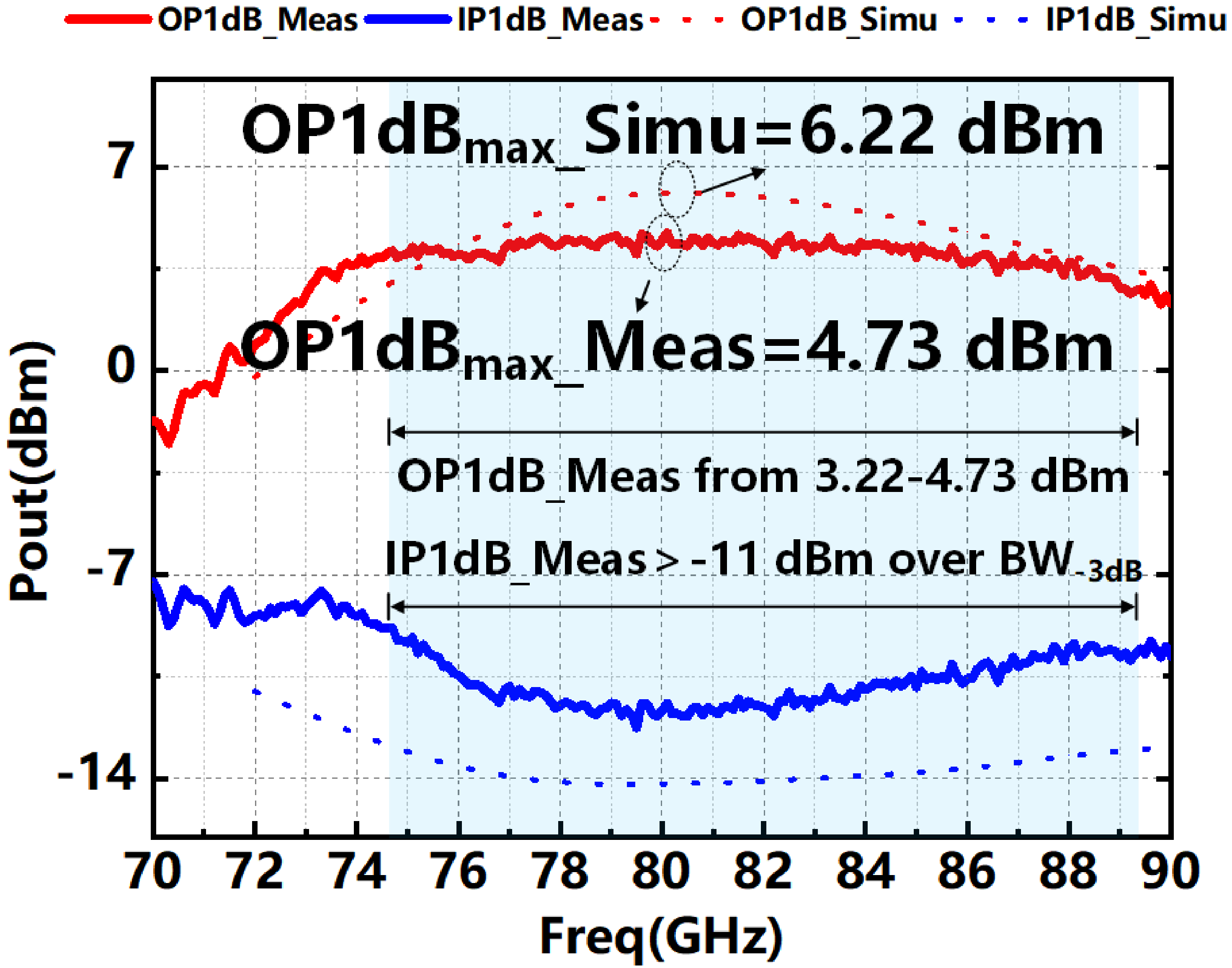


Process: 55-nm CMOS, Area: 895*120μm^2

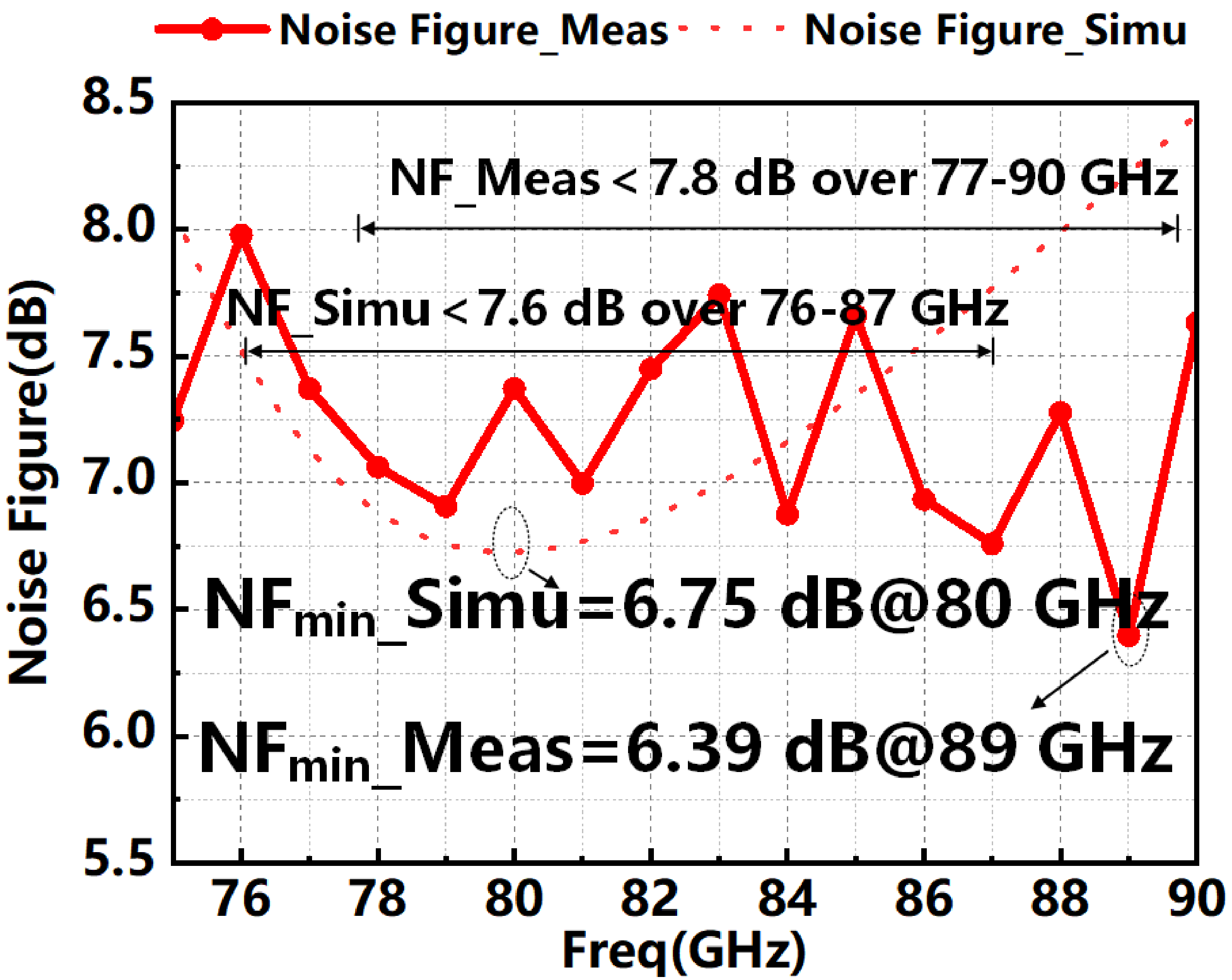
Simulated and Measured S-parameters



Large Signal Measurement Results



NF Measurement Results



Performance Comparison

Ref	[10] JSSC 2017	[11] TMTT 2020	[12] RFIC 2020	[8] IMS 2020	[13] MWCL 2022	This Work
Technology	28nm CMOS	22nm FDSOI	65nm CMOS	55nm CMOS	40nm CMOS	**55nm CMOS**
Topology	1-stage CG 4-stage CS	3-stage CSCG	3-stage CS	2-stage CS 1-stage CSCG	3-stage CS	**1-stage CG 1-stage CS 2-stage CSCG**
Structure	Differential	Single-ended	Differential	Differential	Differential	**Differential**
Peak Gain(dB)	29.6	24	25	15	19	**17.1**
BW_{3dB}(GHz)	28.3 (68.1-96.4)	13 (70.5-83.5)	7.5 (53.5-61)	7.6 (78.9-86.5)	16.1 (76.5-92.6)	**14 (74.8-88.8)**
Minimum NF(dB)	6.4	4.6	4.8	5	5.7	**6.39**
IP1dB(dBm)	-28.1	-26.8	-22	-13.2	-19	**-12.37**
OP1dB(dBm)	+1.5	-2.8#	+3.0#	+1.8#	0#	**+4.73**
P_{DC}(mW)	31.3	16	47	72.7	23.4	**72.4**
Area(mm^2)	0.675	0.35	0.26	0.08	0.17	**0.107***
FOM_1	12.57	14.28	8.86	13.01	26.84	**24.29**

Estimated values

* Area excluding bondpads

$$FOM_1 = Gain[lin] \cdot BW_{-3dB}[MHz] \cdot IP1dB[lin]/\{P_{dc}[mW] \cdot (F-1)\}$$

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Conclusions

- Hybrid step-even and step-down interstage coupling network to achieve high bandwidth
- Inductor-Feedback Common-Gate-Shorting to simultaneously obtain high gain and high OP1dB
- Out-of-Phase-Dual-Coupling to achieve high gain and low noise
- Measurement results of the 55nm CMOS LNA demonstrated a -3dB bandwidth of 14 GHz, a 17.1 dB peak gain, a minimum NF of 6.39 dB, and 4.73 dBm OP1dB

Thank you!

Q&A