# Tu1E-2

# A *V*-band CMOS Sextuple Sub-harmonically Injection-locked VCO using Transformer and Cascade-series Coupling with FTL

**Wei-Cheng Chen, Hong-Yeh Chang**

**Depart. of Electrical Engineering, National Central University, Taoyuan, Taiwan**

# Outline



- Introduction
- Circuit Design
  - Referred Reported Approach
  - Circuit Analysis
- Experimental Results
- Comparison Table
- Conclusion
- Reference

# Introduction

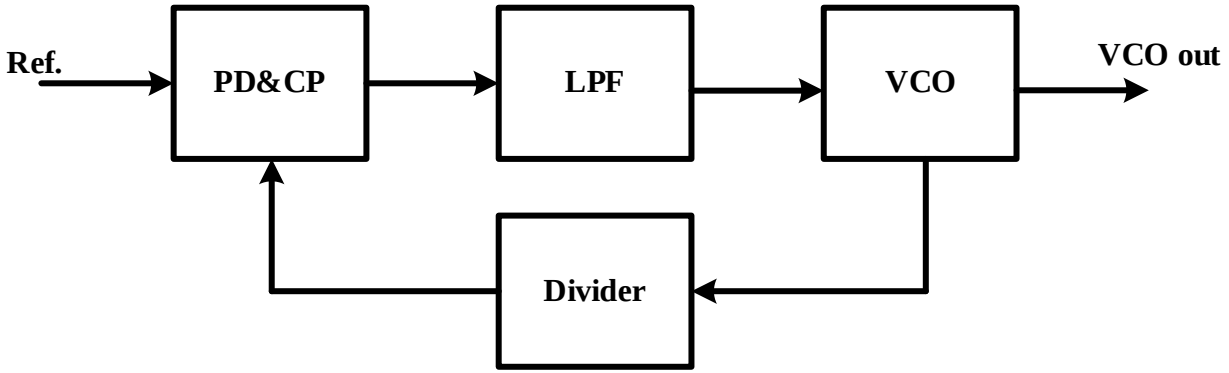


- For modern millimeter-wave (MMW) applications, such as radar, and 5G communication [1], the local oscillator (LO) is a critical component.
- Phase-locked loop(PLL) is generally used to be the local oscillator in the transceiver system.
- As the operating frequency is up to MMW bands, the phase noise and DC power consumption have been challenged.

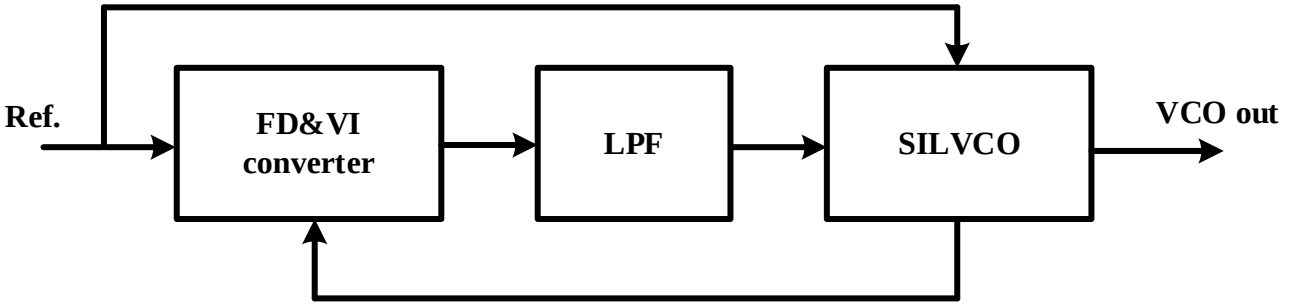
# Introduction (Cont'd)



- Frequency-tracking loop (FTL) used injection-locked technique can provide low phase noise, and its DC consumption is lower than PLL due to the divider-less topology.
- But the frequency ratio of the reference frequency to output frequency can not be too high.

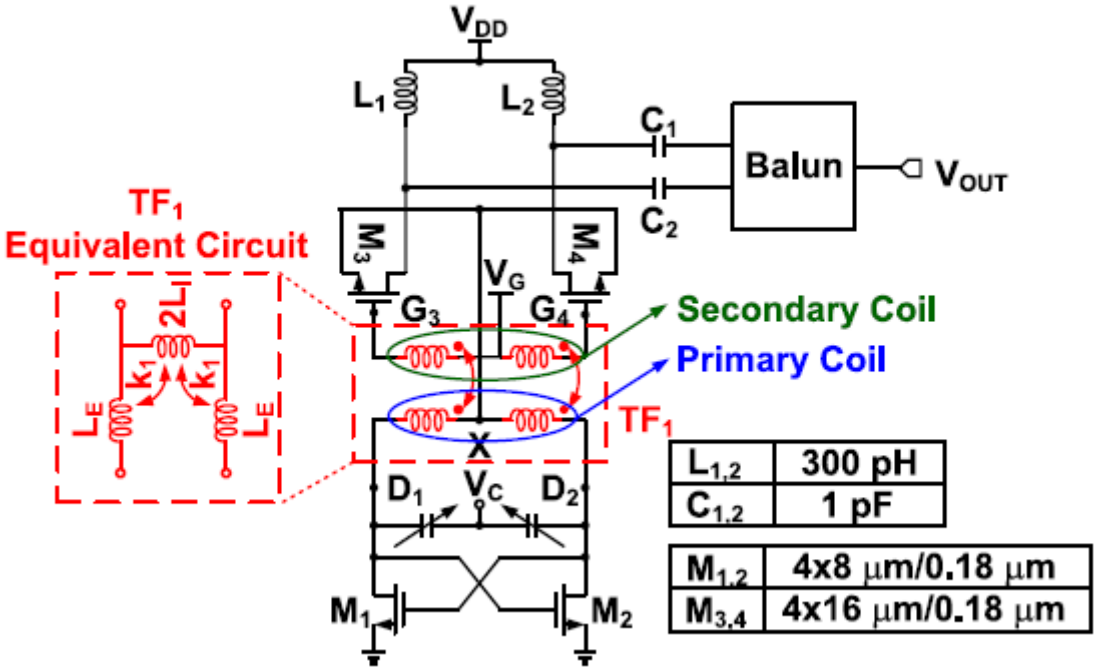


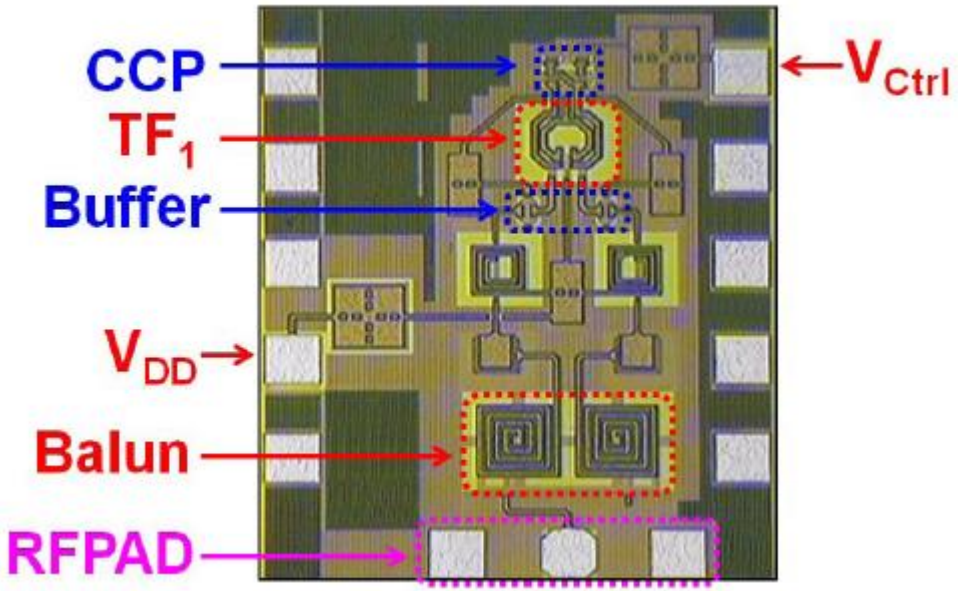

(a)Phase-locked loop




(b)Frequency-tracking loop

# Previously Reported Approach [4]



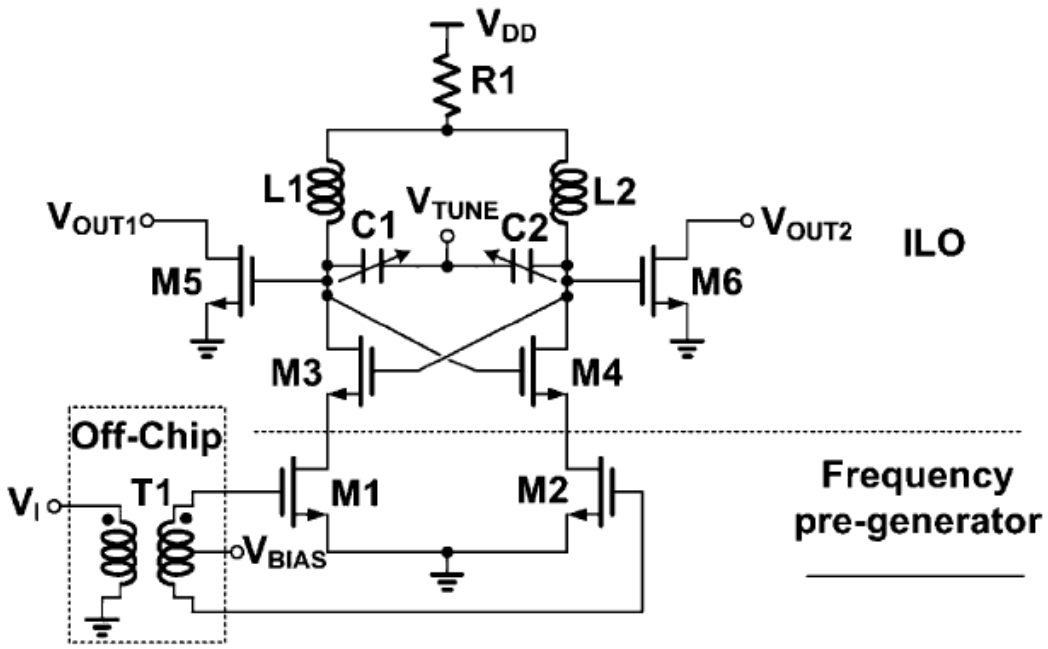



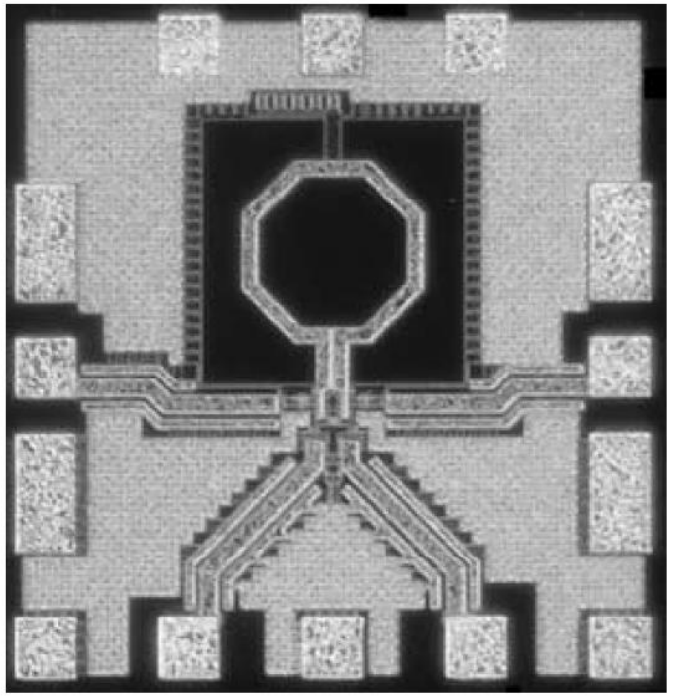

- **Operating frequency is from 22.35 to 25.31 GHz.**
- **Peak output power and peak efficiency are 4.37 dBm and 10.9%.**


[4] Y.-T. Chang and H.-C. Lu, "A K-band high-efficiency VCO using current reused technique," *IEEE Microw. Compon. Lett.*, vol. 27, no. 12, pp. 1134-1136, Dec. 2017.

# Previously Reported Approach [15]





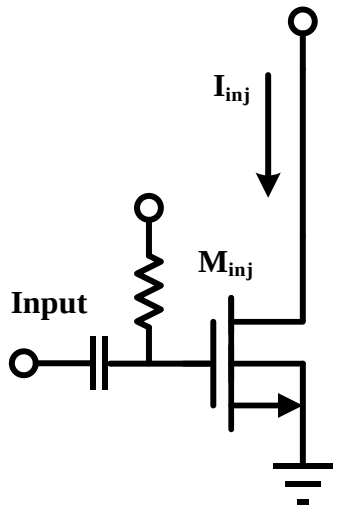



- K- and V-band subharmonic injection-locked frequency triples.
- K-band locking range is 1.1 GHz, V-band locking range is 1.4 GHz.

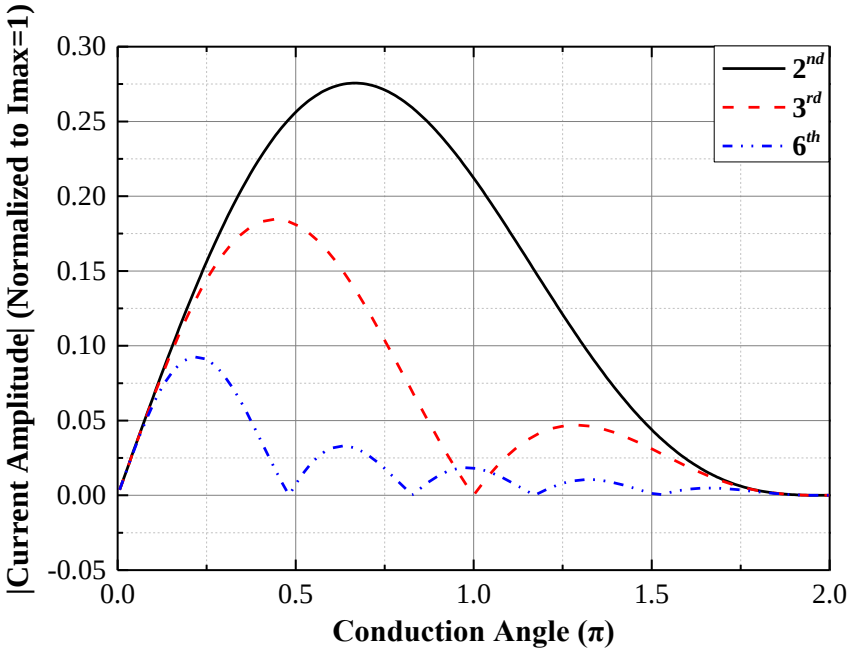
[15]M.-C. Chen and C.-Y. Wu, "Design and analysis of CMOS subharmonic injection-locked frequency triplers," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 8, pp. 1869–1878, Aug. 2008.

# Single-Stage Injector



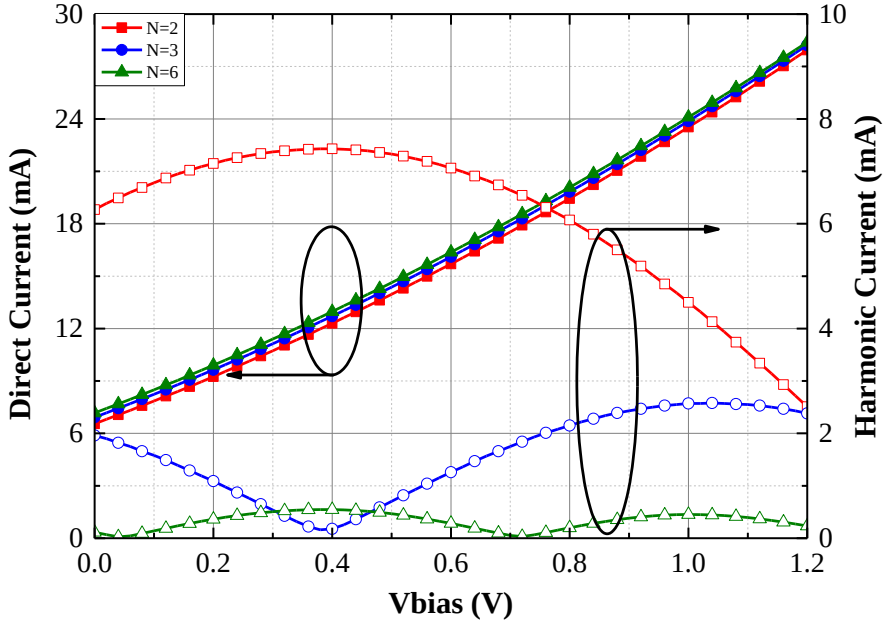



## Conductor Angle




- Calculation of the normalized amplitude for 2nd, 3rd, and 6th harmonic drain currents versus conduction angle.

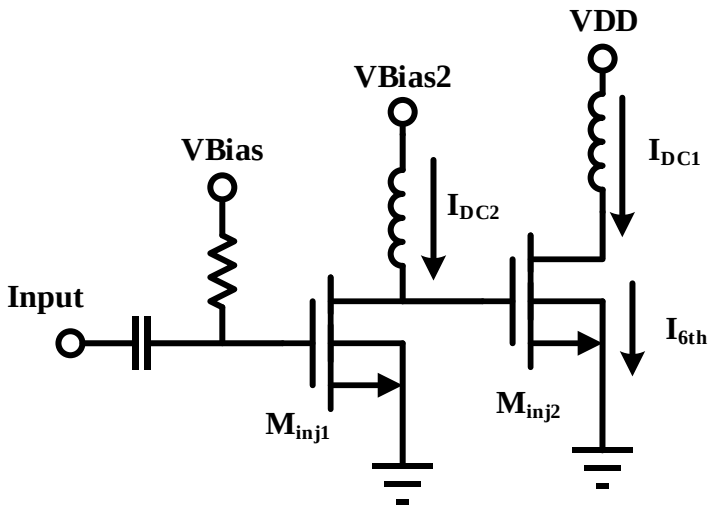
## DC & Harmonic Current vs. Vbias



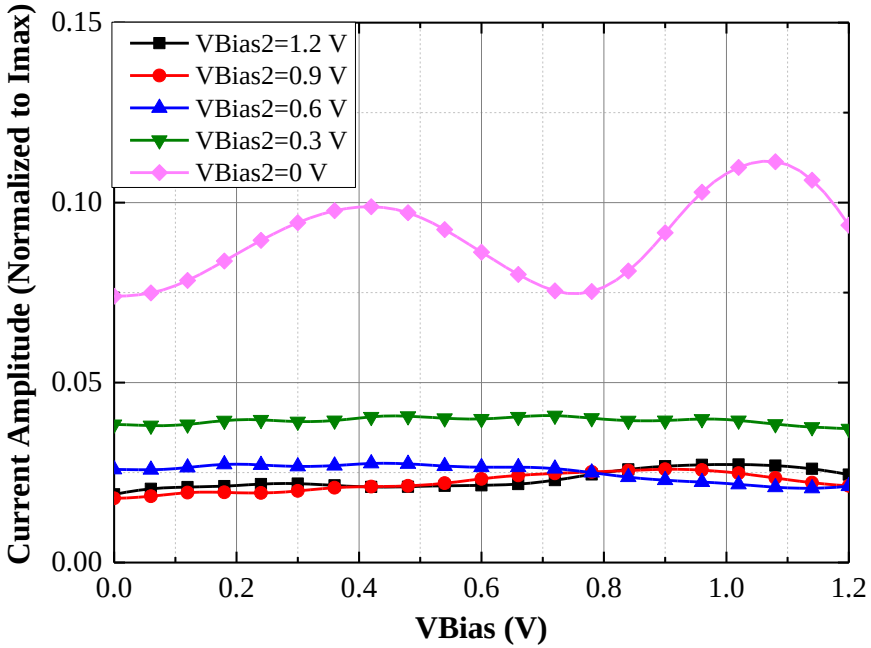

- Simulation of the 2nd, 3rd, and 6th direct current and harmonic current versus Vbias.

# Cascade Injector

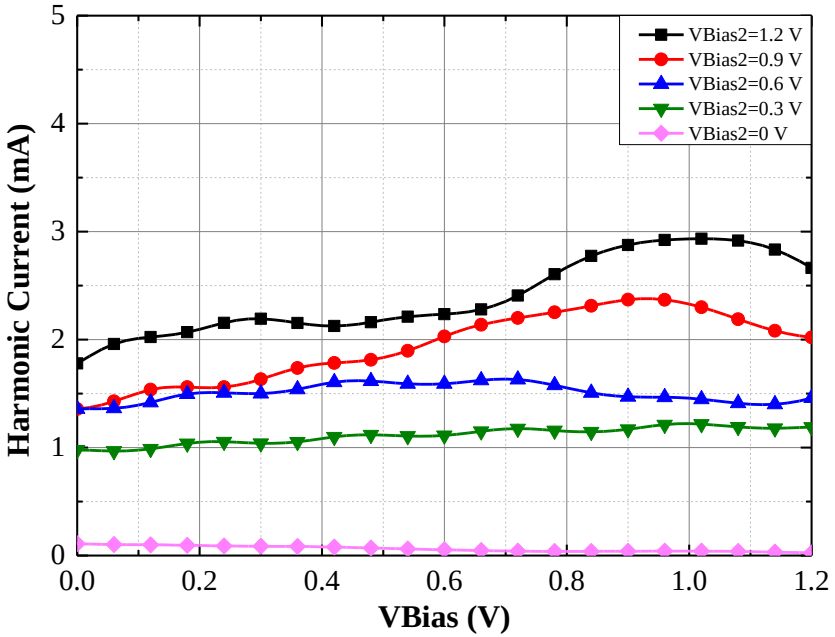





Normalized Harm. Current vs. Vbias



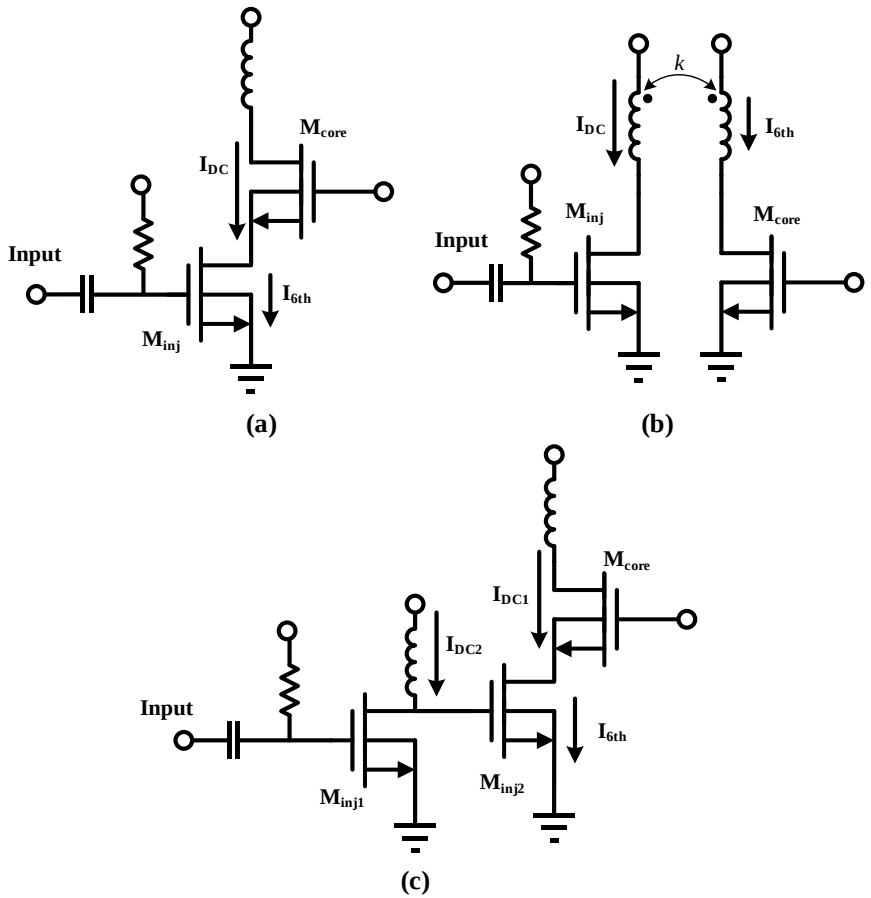

Harmonic Current vs. Vbias



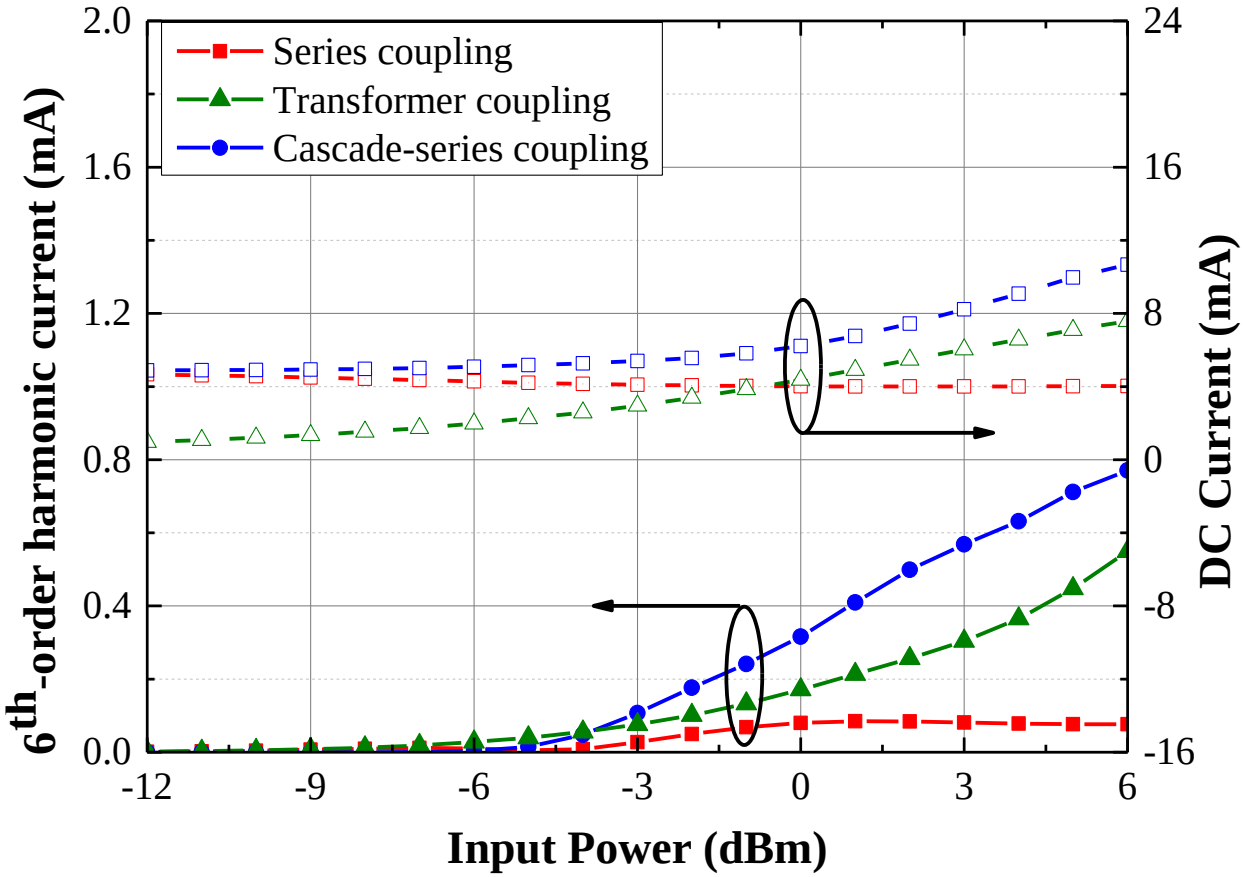

- VBias=0.1 V and VBias2=0.6 V

# Comparison of Injectors



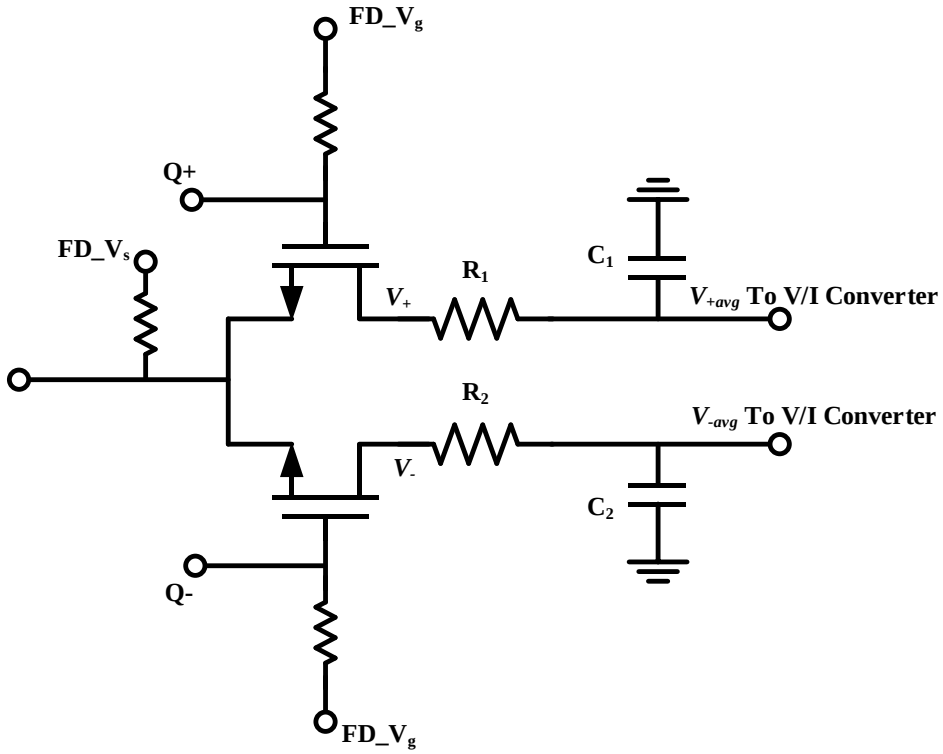


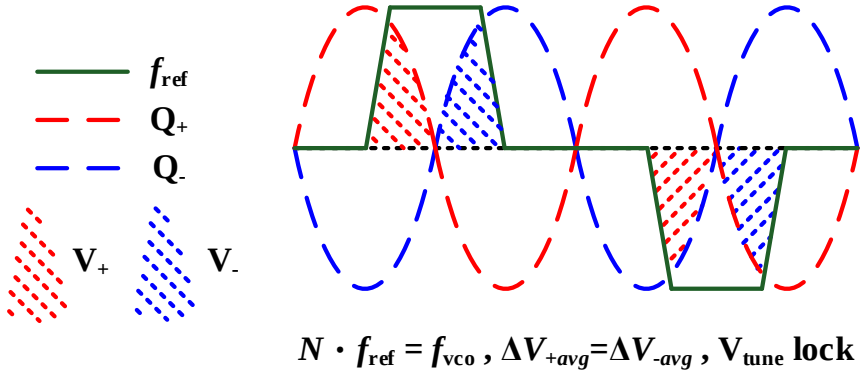

(a)Series coupling (b) Transformer coupling and (c)cascade-series Coupling



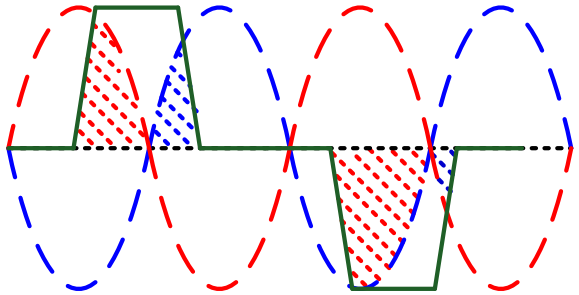
# How Frequency Detector works



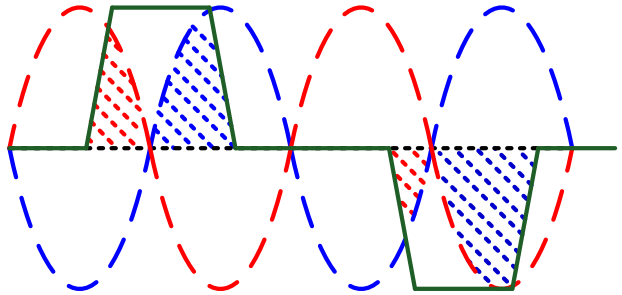



$N \cdot f_{ref} = f_{vco}$ , $\Delta V_{+avg} = \Delta V_{-avg}$ , $V_{tune}$ lock



$N \cdot f_{ref} > f_{vco}$ , $\Delta V_{+avg}\downarrow$ $\Delta V_{-avg}\uparrow$, $V_{tune}\uparrow$

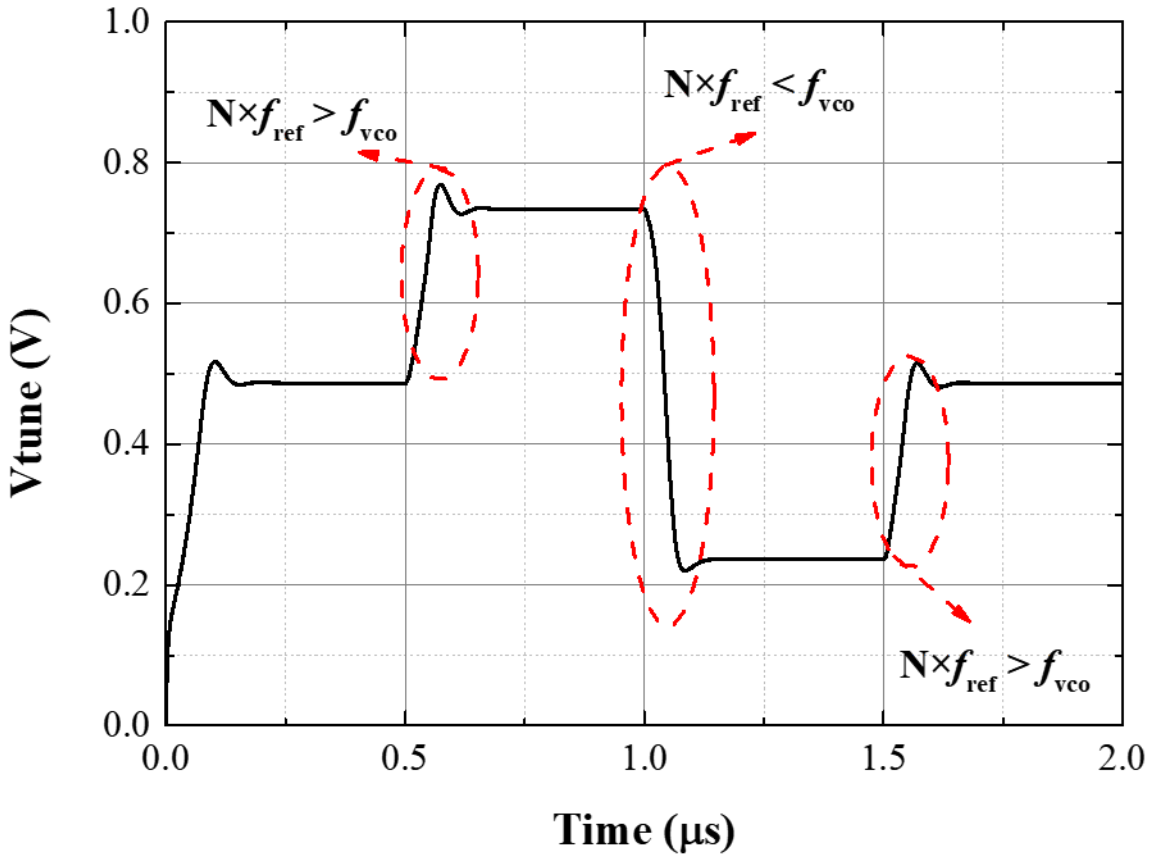


$N \cdot f_{ref} < f_{vco}$ , $\Delta V_{+avg}\uparrow$ $\Delta V_{-avg}\downarrow$, $V_{tune}\downarrow$

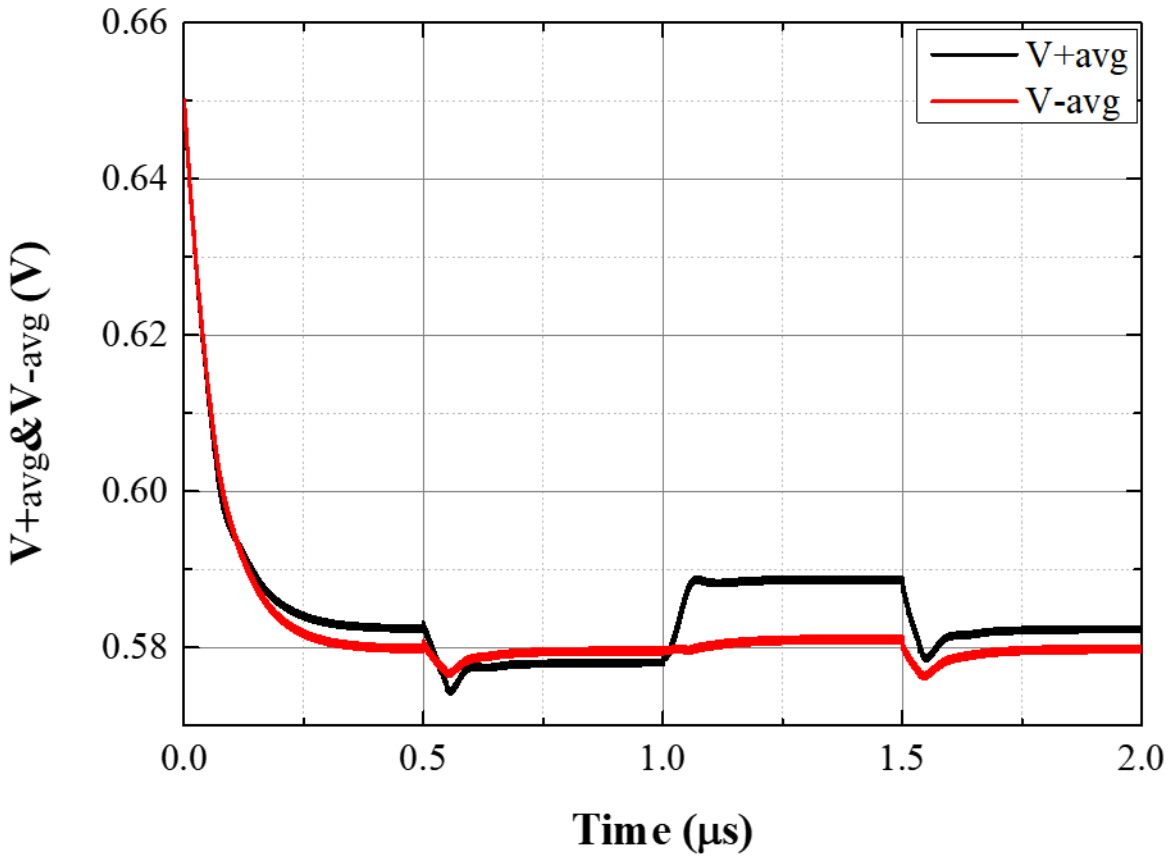
- As the SILVCO output frequency is compared to the injected signal, the frequency detector's output voltages V+ and V- would correspond to the frequency lead and lag.
- The average voltages $V_{+avg}$ and $V_{-avg}$ after the C1 and C2 will be amplified using the V/I converter to control the output frequency of the SILVCO.

# Illustrated Waveform of FTL

Output Voltage of Vtune




Compared Voltage



# TSMC 90 nm CMOS Process



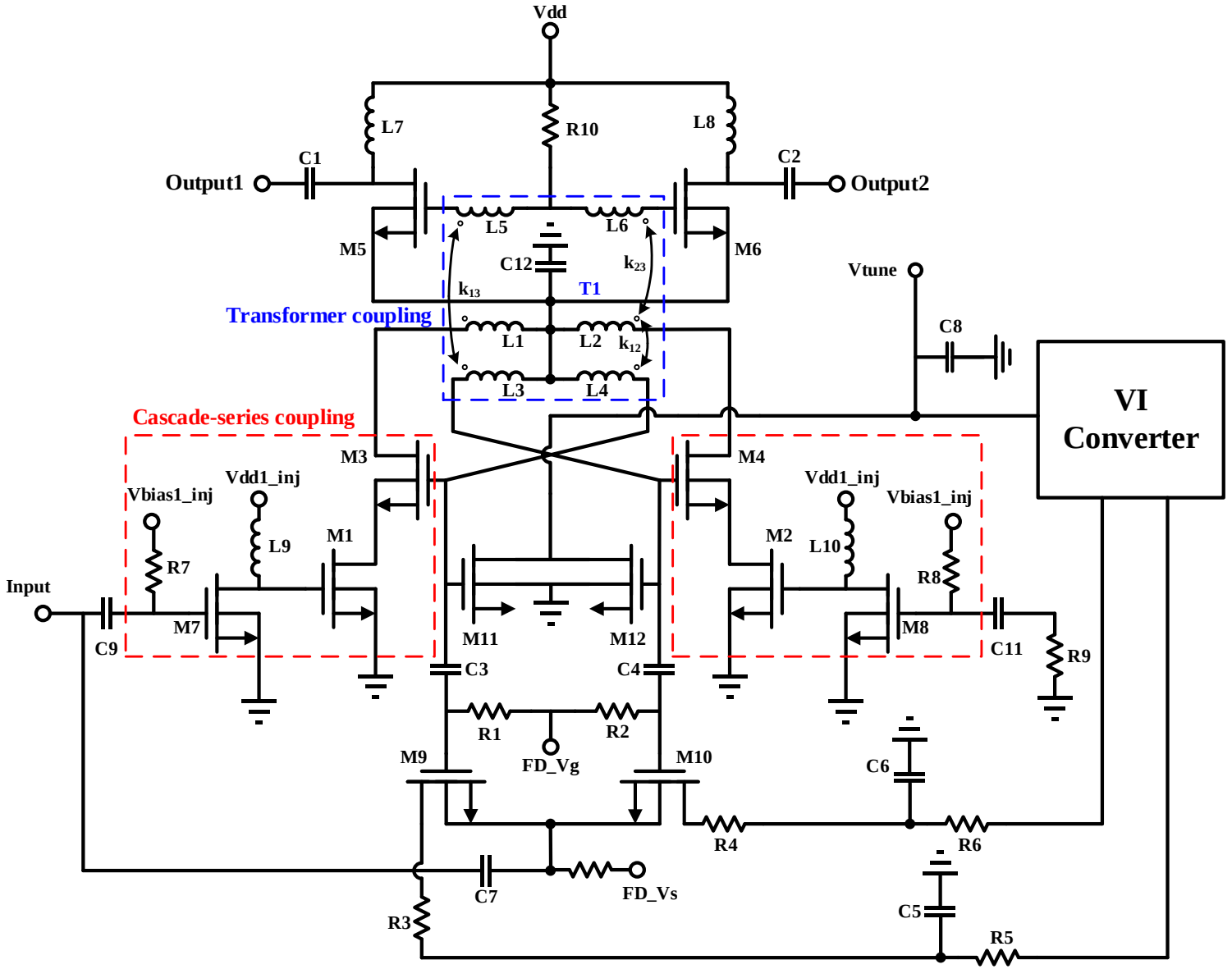
- Taiwan Semiconductors Manufacturing Company (TSMC) commercial 90 nm CMOS process.
- NMOS unity current gain frequency ($f_T$) is higher than 100 GHz.
- NMOS maximum oscillation frequency ($f_{max}$) is higher than 150 GHz.
- Metal-insulator-metal capacitor and polysilicon resistors are available in the process.

# Schematic of the Proposed Circuit



- M3-M4 Cross-coupled Pair
- M5-M6 Output Buffer
- M1-M2,M7-M8 Injector
- M9,M10 Frequency Detector

- Vdd=2.1 V/9 mA
- Vdd1 _inj=0.6 V
- Vbias1_inj=0.1 V
- Vdd_v/i=1.2 V
- FD_Vs= 0.8V
- FD_Vg= 0.1V

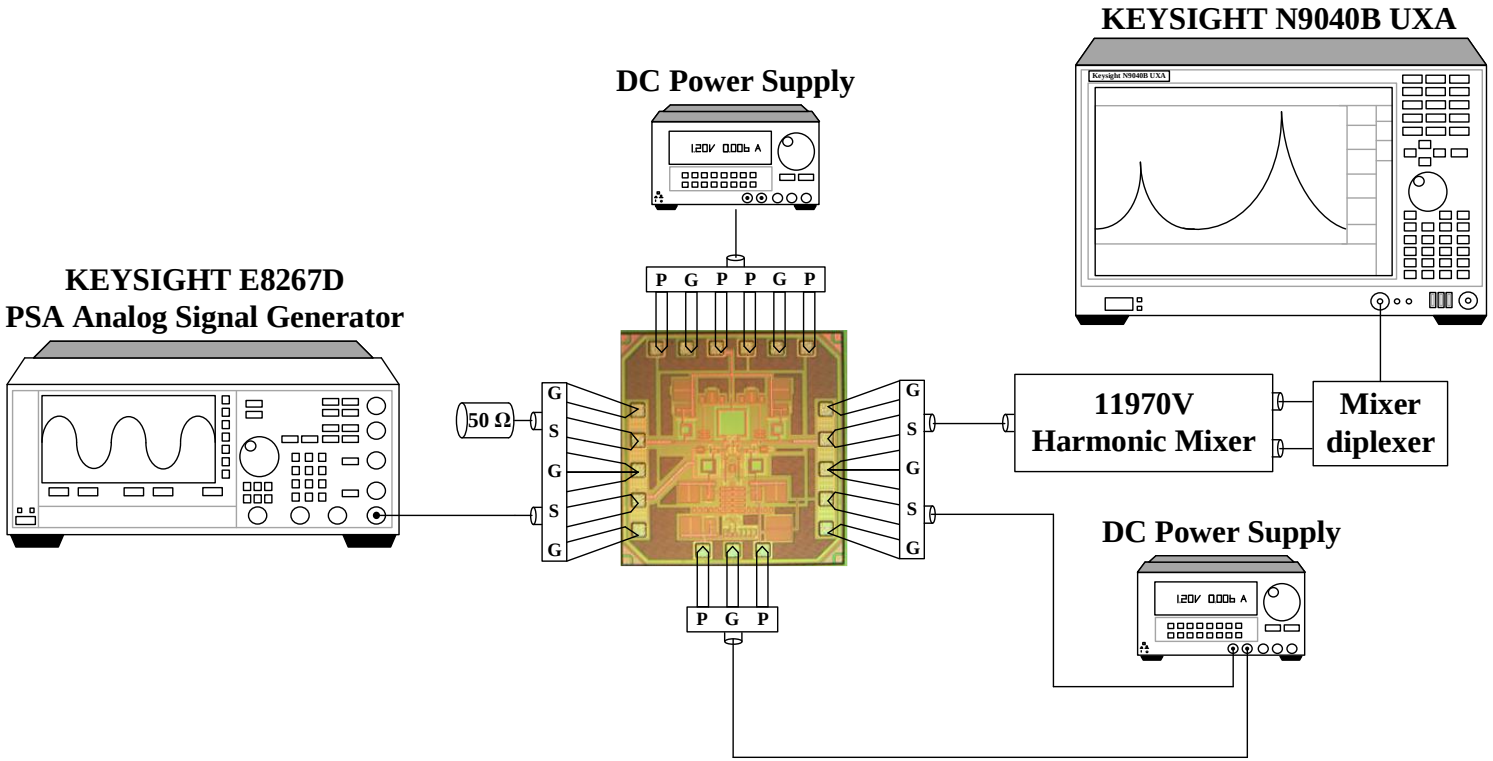


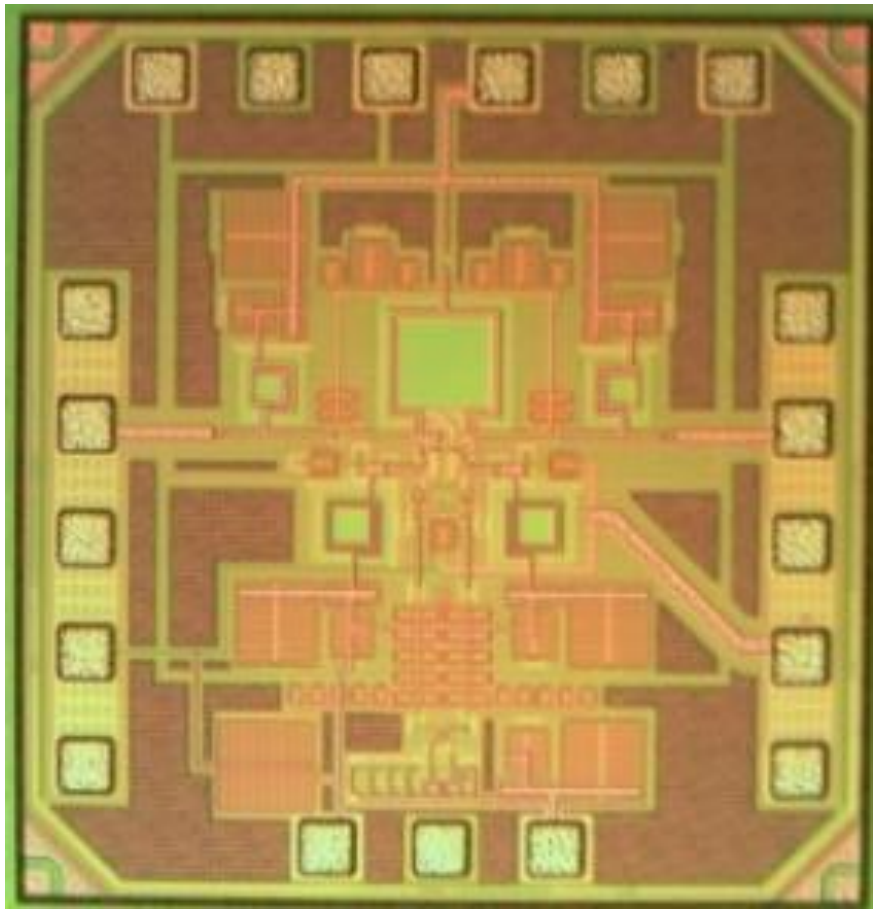
# Chip Photograph & Meas. Setup



- Chip Size:

  $0.746 \times 0.781\ mm^2$

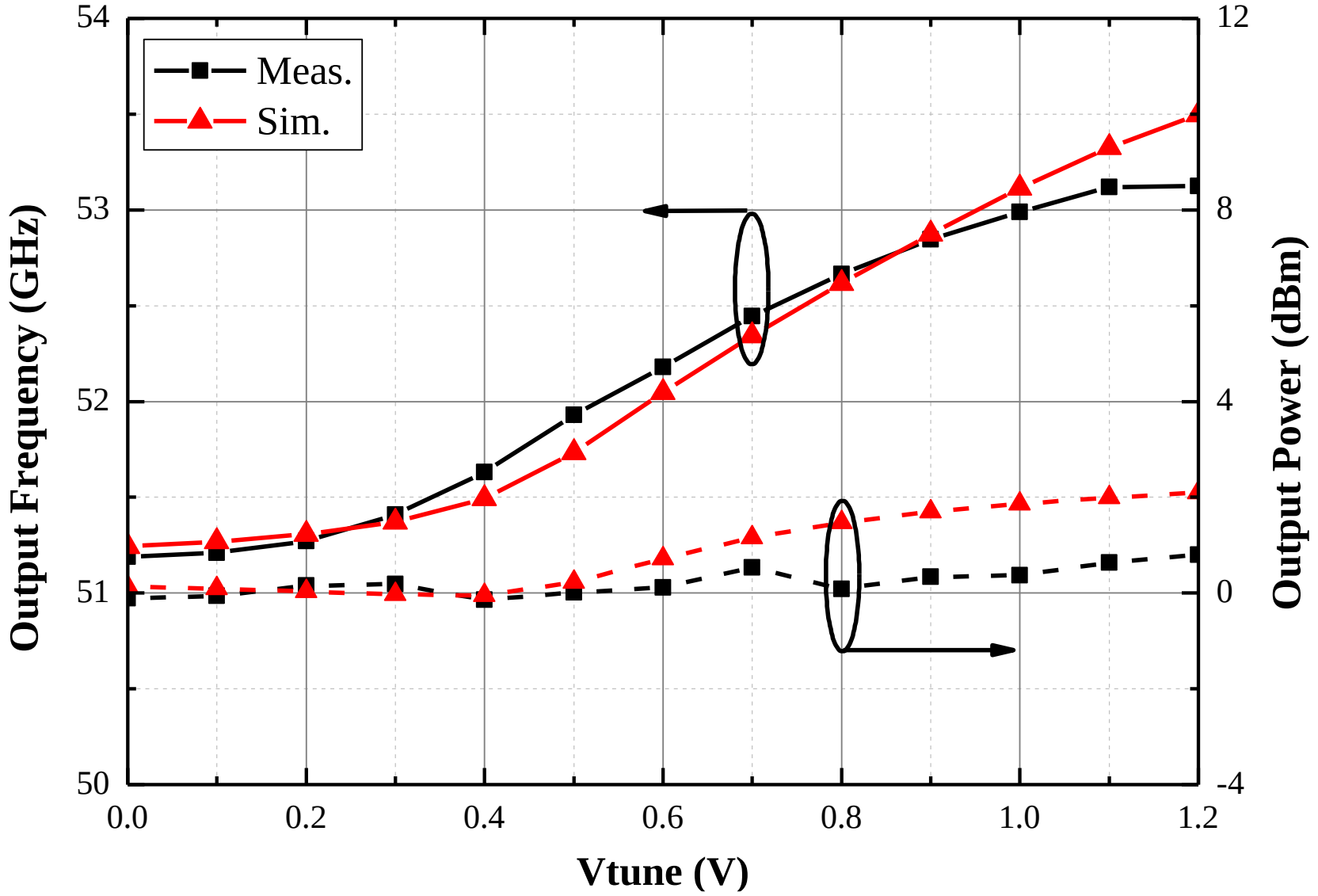


# Meas. Output Freq. & Power

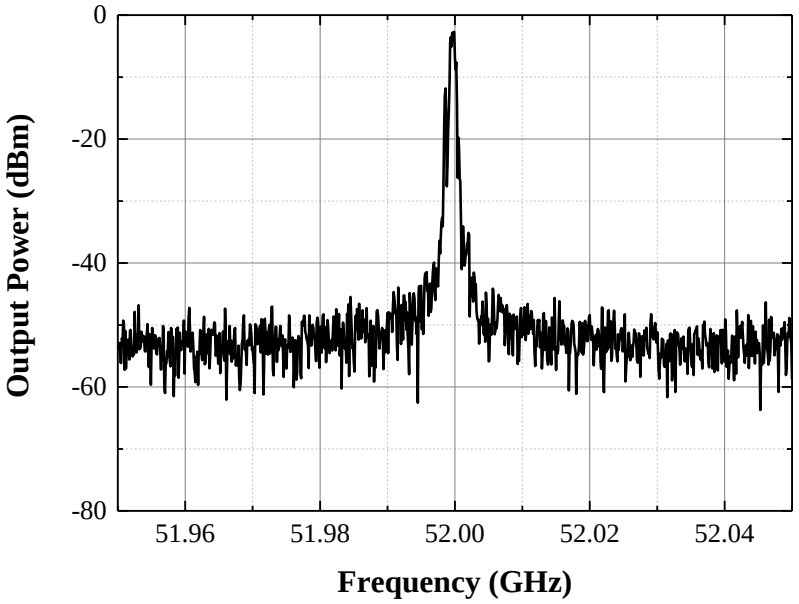


- Operating Frequency:
  51.2~53.13 GHz
- Output Power:
  -0.11~1.19 dBm



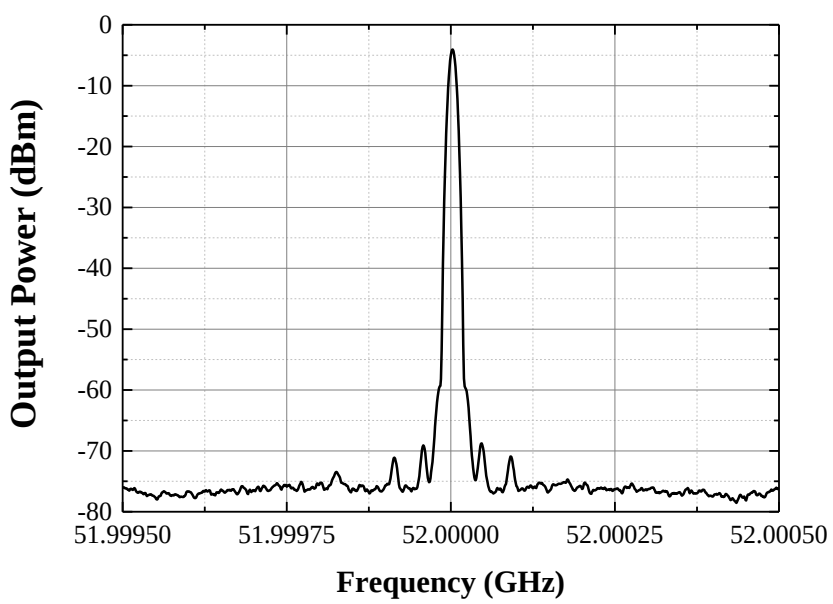
# Meas. Output Spectra

ILO Free-running condition



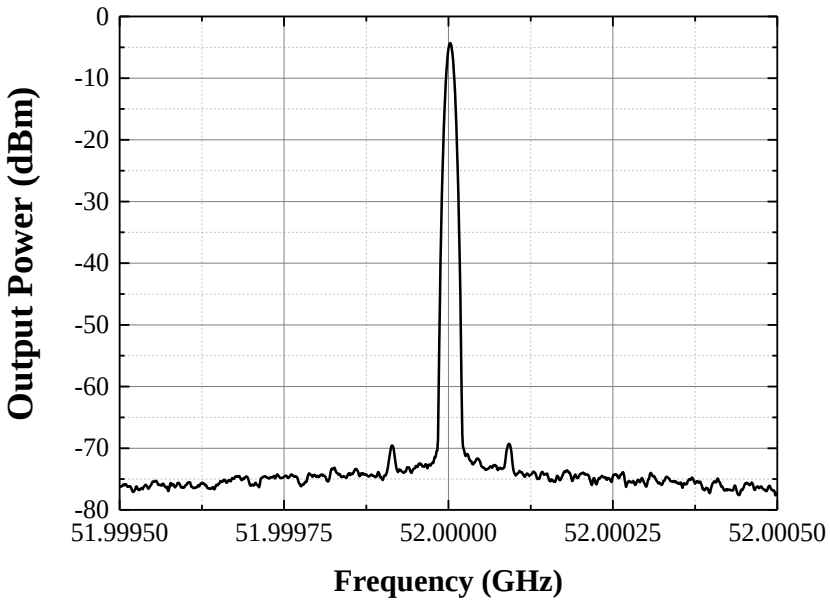

(a)

ILO Under locked condition




(b)

FTL Under locked condition

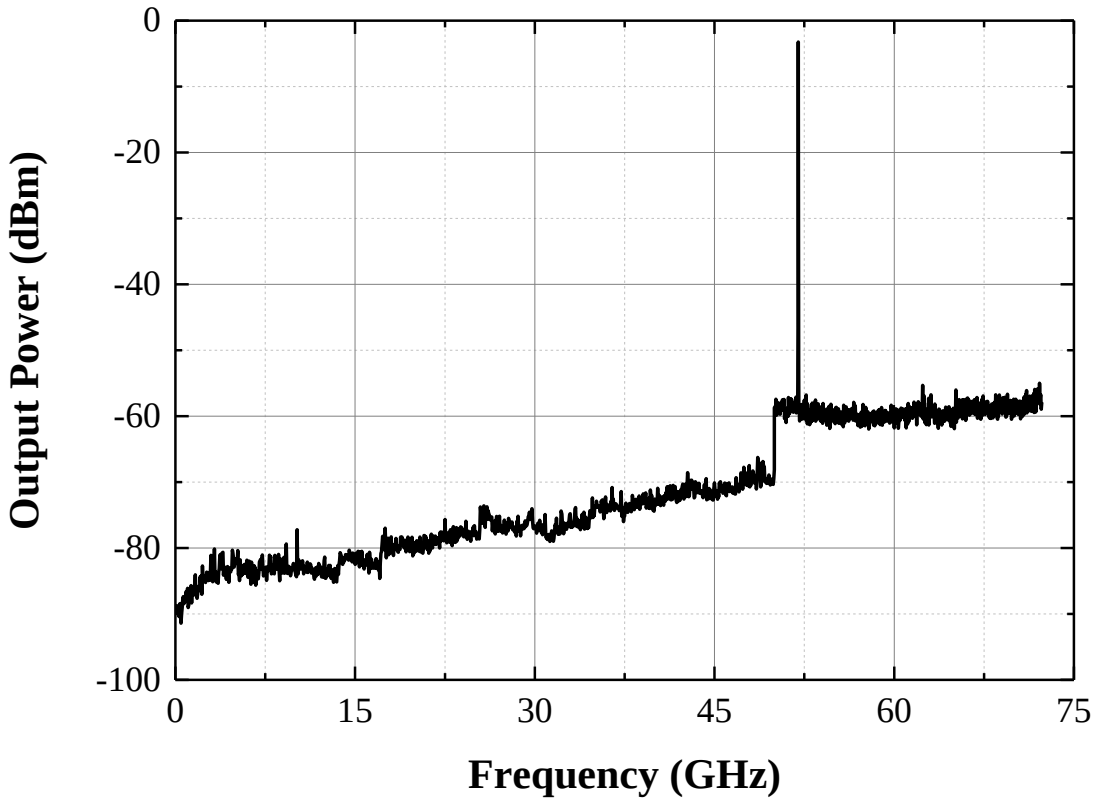



(c)

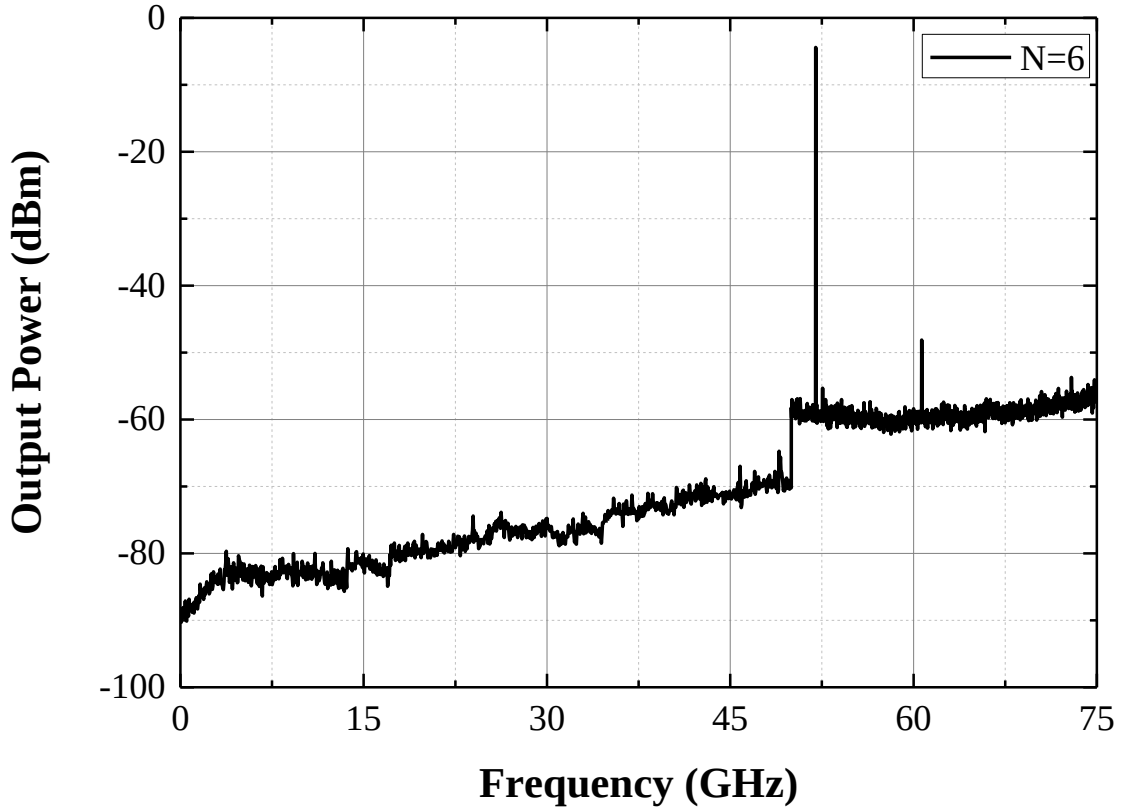
- Measured 52 GHz spectra with (a) free-running (span 100MHz), (b) locked oscillator (span 1MHz), and (c) locked FTL (span 1MHz).

# Meas. Output Spectra (0.1 – 75 GHz)

ILO Free-running condition



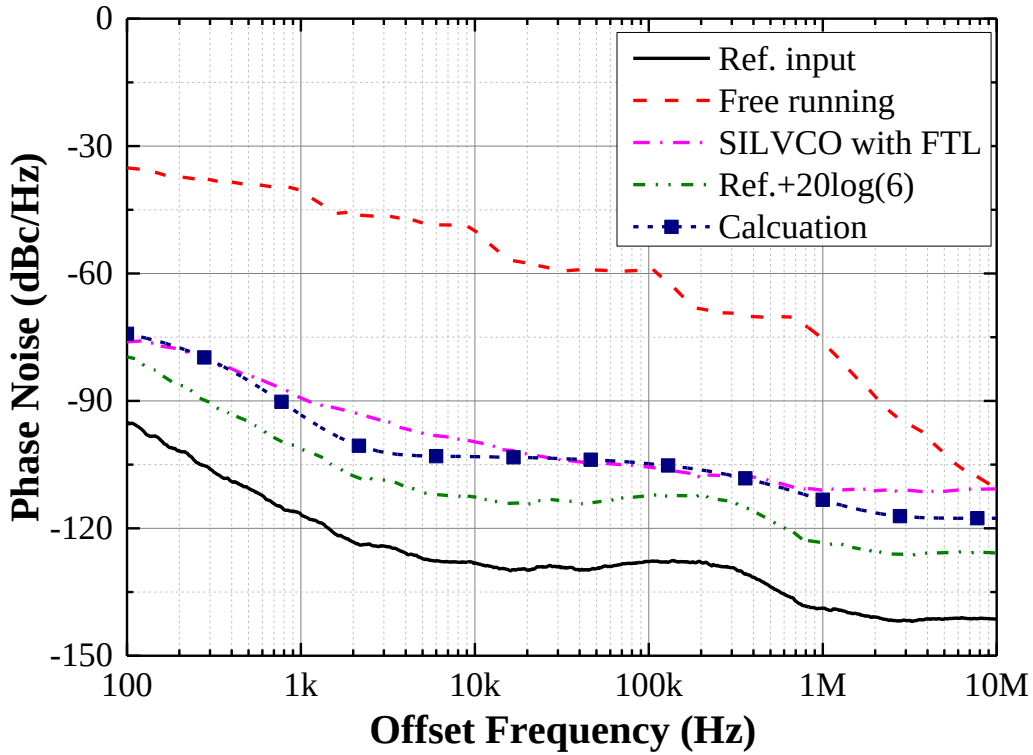

FTL Under locked condition



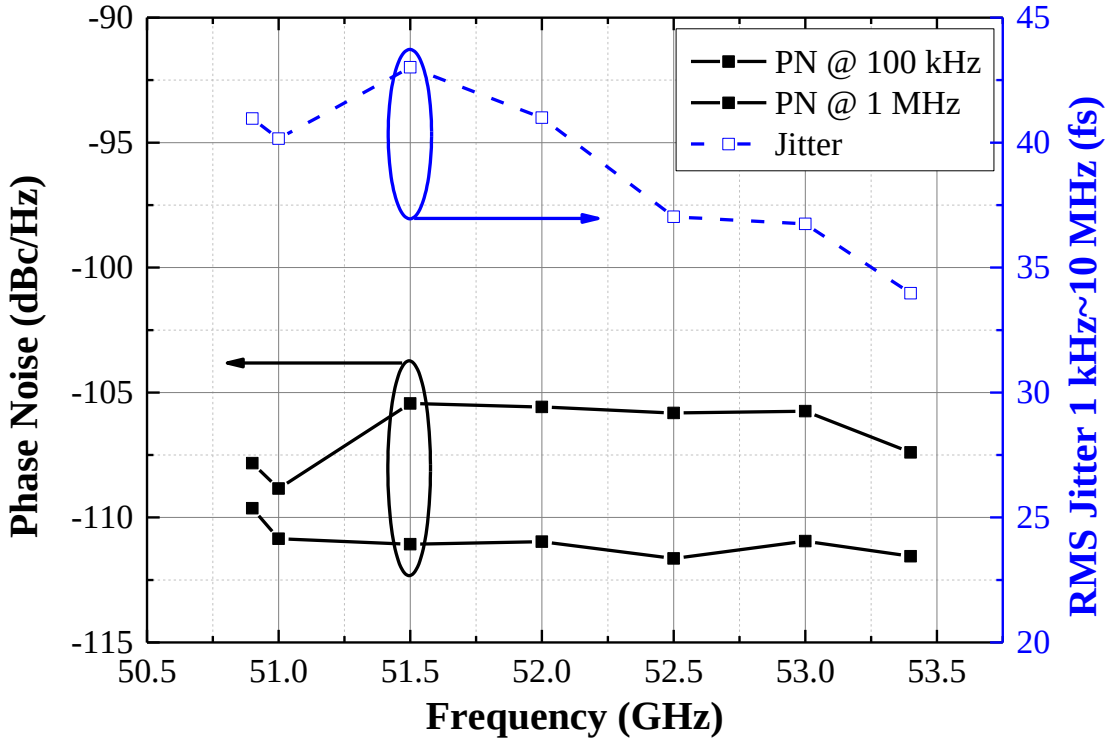

- Harmonic suppression is better than -40 dBc for the locked condition

# Meas. Phase Noise & RMS Jitter

Phase Noise Analysis




Phase Noise & RMS Jitter




- Phase noise@ 100 kHz is lower than -105 dBc/Hz.
- RMS Jitter is within 43.01 fs which integrated 1kHz to 10 MHz.

# Comparison with Prior Art

| Ref. | Tech. (CMOS) | Topo. | Freq. (GHz) | Tuning Range | | Locking Range (GHz) | $P_{out}$ (dBm) | PN@1MHz (dBc/Hz) | $P_{DC}$ (mW) | Area ($mm^2$) | FoM | $FoM_P$ | N |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | (GHz) | (%) | | | | | | | | |
| **[5]** | 90 nm | SILQVCO | 59 | 2.4 | 4.2 | 3.5 | -15 | -126.8 | 19.8 | 0.12[#] | -186.2 | -177.2 | 3 |
| **[6]** | 0.13 µm[&] | Dif. ILVCO | 54.1 | 9.6 | 17 | <1.4 | -10.9 | -105 | <6.6 | 0.02 | -164.7 | -156.8 | 8 |
| **[7]** | 65 nm | Quad. FTL | 33 | 6 | 18.2 | 6.6 | -8 | -130.3 | 31.3 | 0.7 | -191.6 | -189.6 | 3 |
| **[8]** | 90 nm | Mod. FTL | 39 | 2 | 5.1 | 3.1 | -12 | -126 | 60 | 1.24 | -184.8 | -178.8 | 4 |
| **[10]** | 90 nm | SILQFLL | 50.2 | 2.4 | 4.9 | 3.5 | -12 | -103.4 | 75.4 | 1.47 | -164.4 | -158.4 | 32 |
| **This work** | 90 nm | TC & CSC FTL | 52.2 | 1.94 | 3.7 | 2.48 | 0 | -109.4@100 kHz<br>-111.6@1 MHz | 23 | 0.58 | -197.9<br>-180.1 | -199.1<br>-181.3 | 6 |

- [#] core only, [$] quadrature output power, [&]BiCMOS

# Conclusion



- A V-band sextuple SILVCO with FTL is successfully developed using a 90-nm CMOS process.
- The locking range is highly enhanced using the cascade-series coupling, and the sub-harmonic number is up to 6.
- This work features low-phase noise, compact size, and high frequency.

# Acknowledgment



- The chip was fabricated by TSMC in Hsinchu City, Taiwan. This work was supported by the National Science and Technology Council (NSTC), Taiwan, under Grant MOST 110-2221-E-008-029-MY3, and the Taiwan Semiconductor Research Institute (TSRI), Hsinchu City, Taiwan. The dc and RF probes are supported by GGB Inc., FL, USA.

# Reference(1)



[1] B. Sadhu, *et al.*, "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[2] C.-C. Lee, *et al.*, "A 44-49 GHz low phase noise CMOS voltage-controlled oscillator with 10-dBm output power and 16.1% efficiency," in *2014 IEEE MTT-S Int. Microw. Symp*, 2014, pp. 1-4.

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[4] Y.-T. Chang and H.-C. Lu, "A K-band high-efficiency VCO using current reused technique," *IEEE Microw. Compon. Lett.*, vol. 27, no. 12, pp. 1134-1136, Dec. 2017.

[5] C.-C. Chan, *et al.*, "A V-band low-phase-noise low-jitter sub-harmonically injection-locked QVCO with high quadrature accuracy in the 90-nm CMOS process," in *2017 IEEE MTT-S Int. Microw. Symp.*, 2017, pp. 1359-1362.

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[7] S. P. Sah and D. Heo, "An 8th sub-harmonically injection locked *V*-band VCO for low power LO routing in mm-wave beamformers," in *IEEE Radio Freq. Integr. Circuits Symp.*, 2014, pp. 177-180.

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[8] J.-W. Li, *et al.*, "A 30-36.6 GHz low jitter degradation SIL QVCO with frequency-tracking loop in 65 nm CMOS for 5G frontend applications," in *Eur. Microw. Integr. Circuits Conf.*, 2021, pp. 241-244.

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[13] D. Shin, S. Raman, and K.-J. Koh, "A mixed-mode injection frequency locked loop for self-calibration of injection locking range and phase noise in 0.13 $\mu$m CMOS," in 2016 *IEEE Int. Solid-State Circuits Conf. Dig.*, San Francisco, USA, Jan./Feb. 2016, pp. 50–51.

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[15]M.-C. Chen and C.-Y. Wu, "Design and analysis of CMOS subharmonic injection-locked frequency triplers," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 8, pp. 1869–1878, Aug. 2008.