Tu1E-4

V-Band LC-VCO and Doubler with Wide Tuning Range and Low Phase Noise Using Series-Shunt Anti-Parallel SiGe HBT Switches

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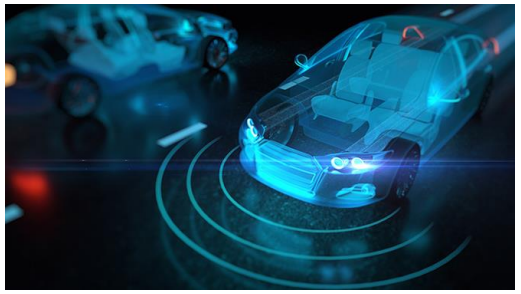
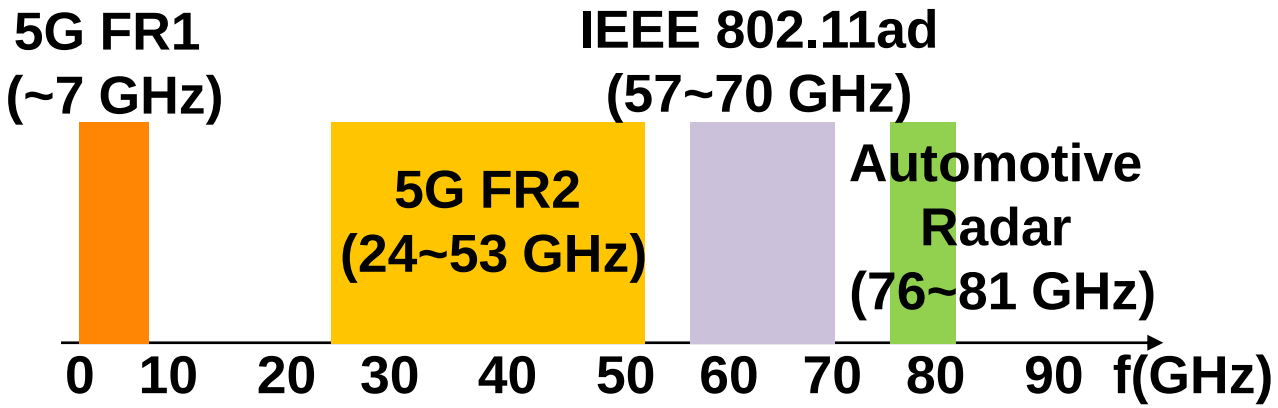
Outline

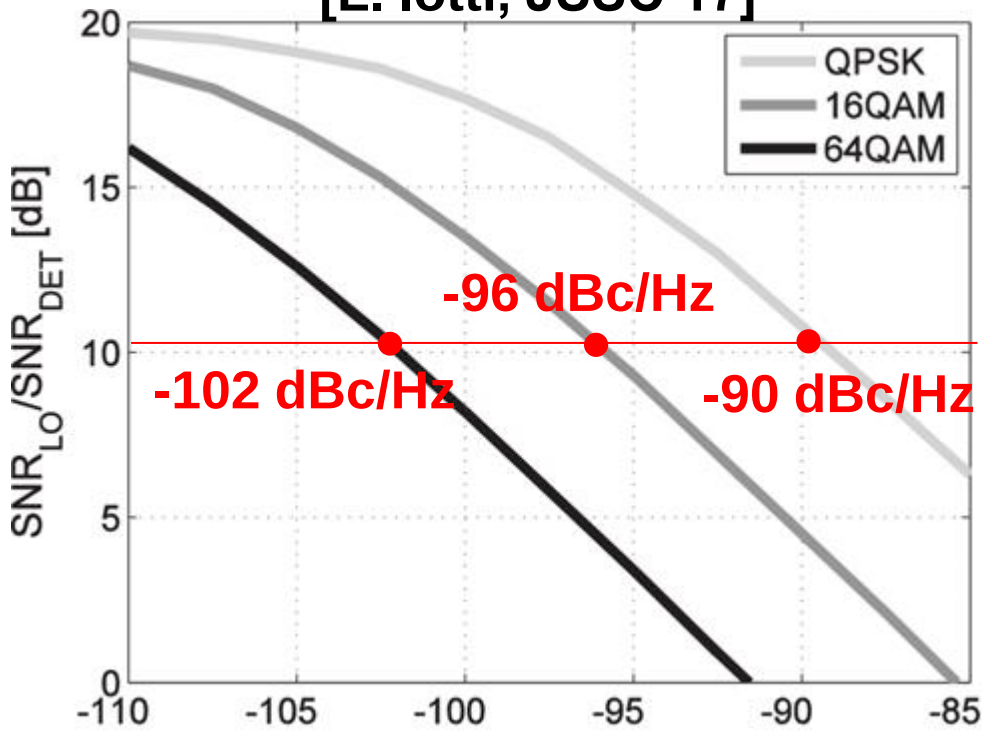
- Motivation and Problem Statement
- Proposed SSAP Capacitor Bank
- VCO Implementation
- Measurement Results
- Summary

Phase Noise Challenges at Mm-wave





[L. Iotti, JSSC'17]



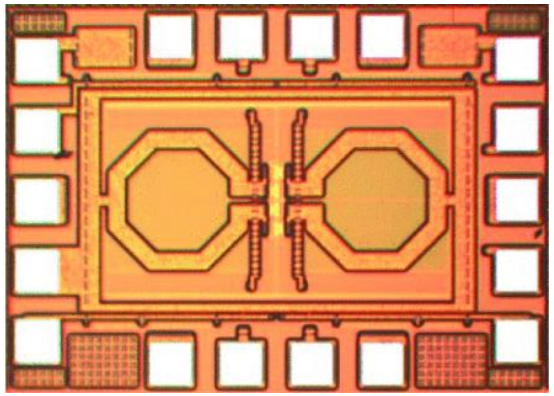
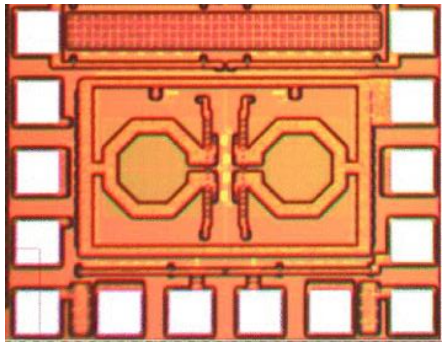
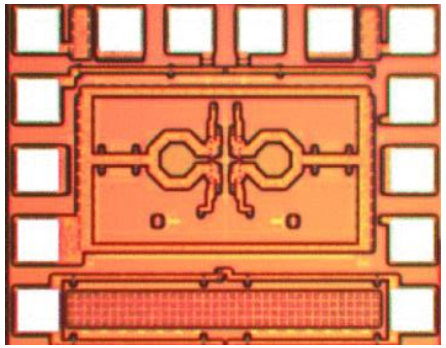
- Mobile communication and radar systems require wide bandwidth and low phase noise

Tuning Range Challenges at Mm-wave

- Tuning range decreases as frequency increases

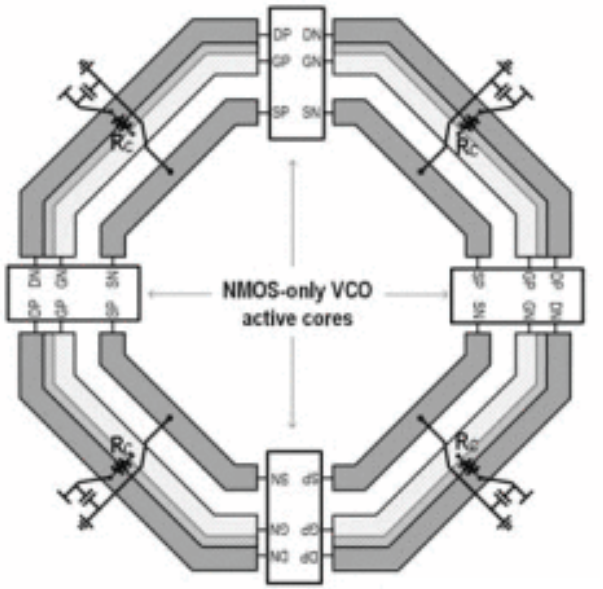
$$f_{osc} = \frac{1}{2\pi\sqrt{L_T(C_{var} + C_b + C_{fix})}}$$

[W. Wang, BCICTS'19]

Layout			
Frequency	10 GHz	20 GHz	40 GHz
Inductance (pH)	438	295	182
Tuning Range (%)	13.7	10.2	4.2

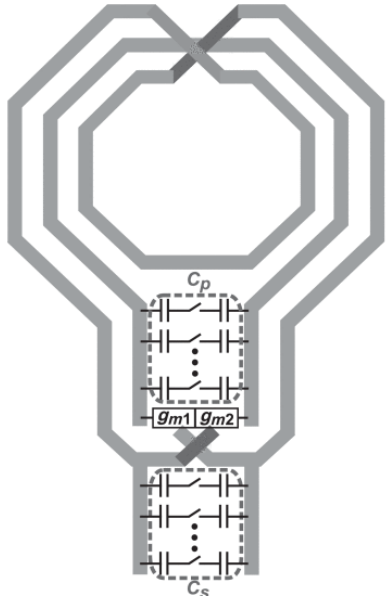
Limitations for Prior Designs

[H. Jia, ISSCC'21]



☺ Low phase noise
☹ Narrow tuning range

[Z. Zong, JSSC'16]



☹ High phase noise
☺ Wide tuning range

- Transformer-coupled QVCO has low PN but narrow FTR
- Magnetically tuned VCO has wide FTR but high phase noise
- How to improve both PN and FTR?

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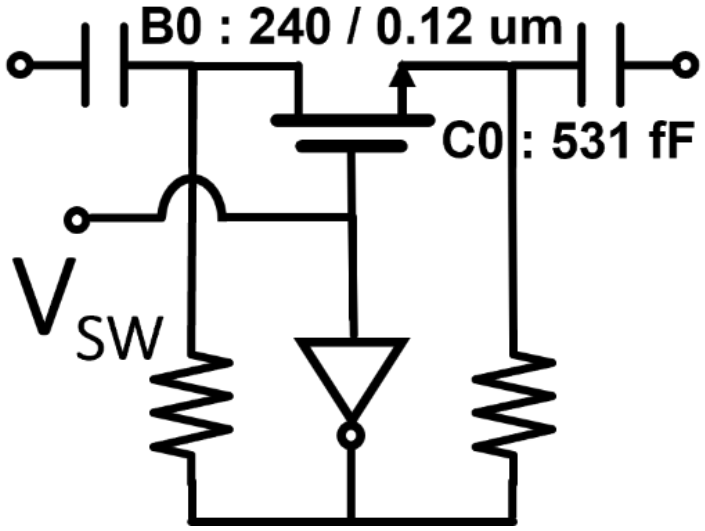
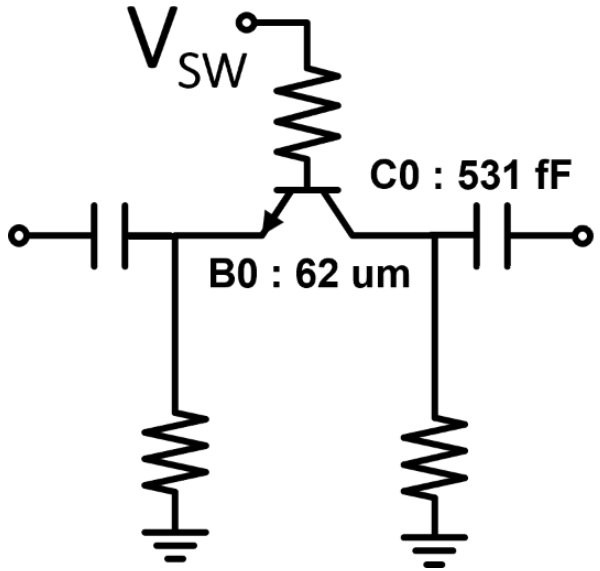
Proposed SSAP SiGe HBT Switch

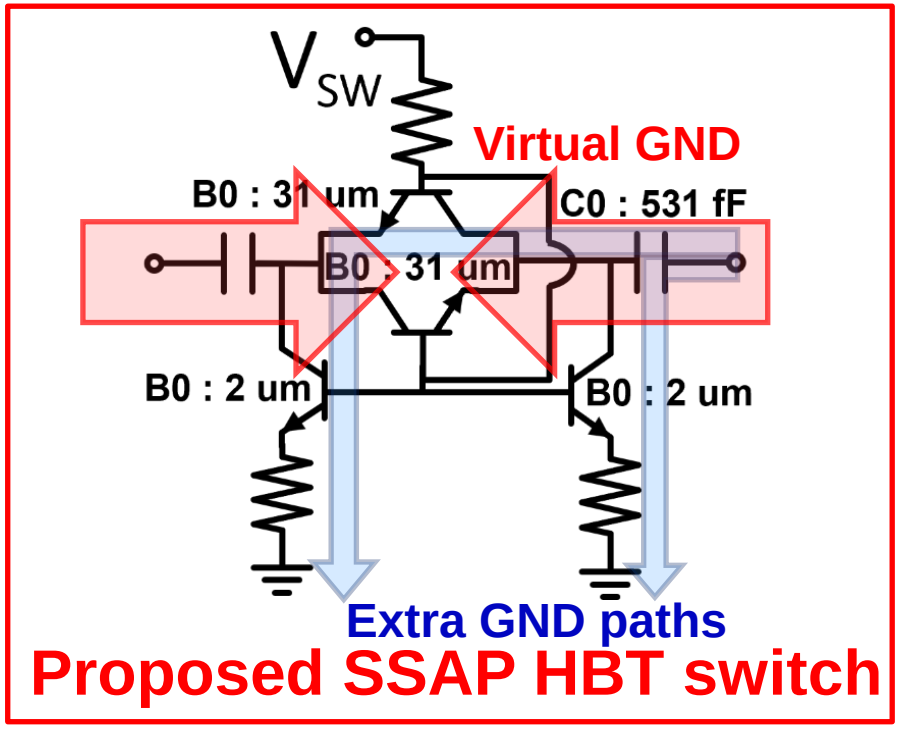
- Series-Shunt Anti-Parallel (SSAP) SiGe HBT switch uses a series-shunt switch topology in an anti-parallel fashion
- Low series R_{on}, high shunt R_{off}, and low parasitic capacitance



CMOS switch



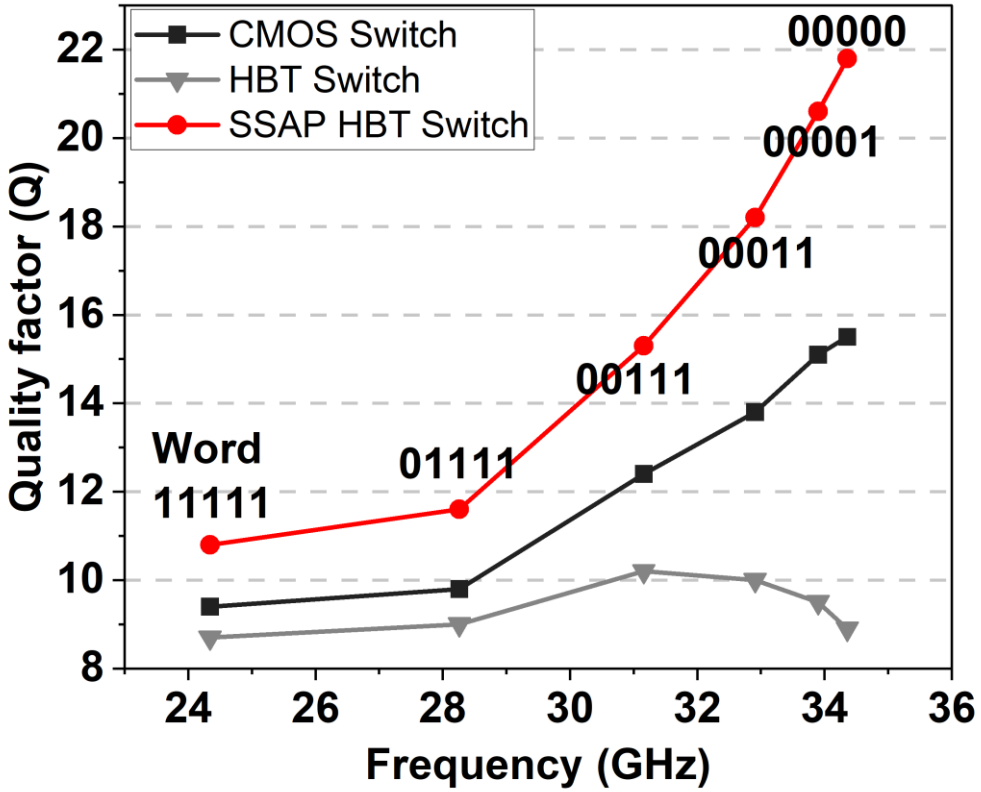
HBT switch



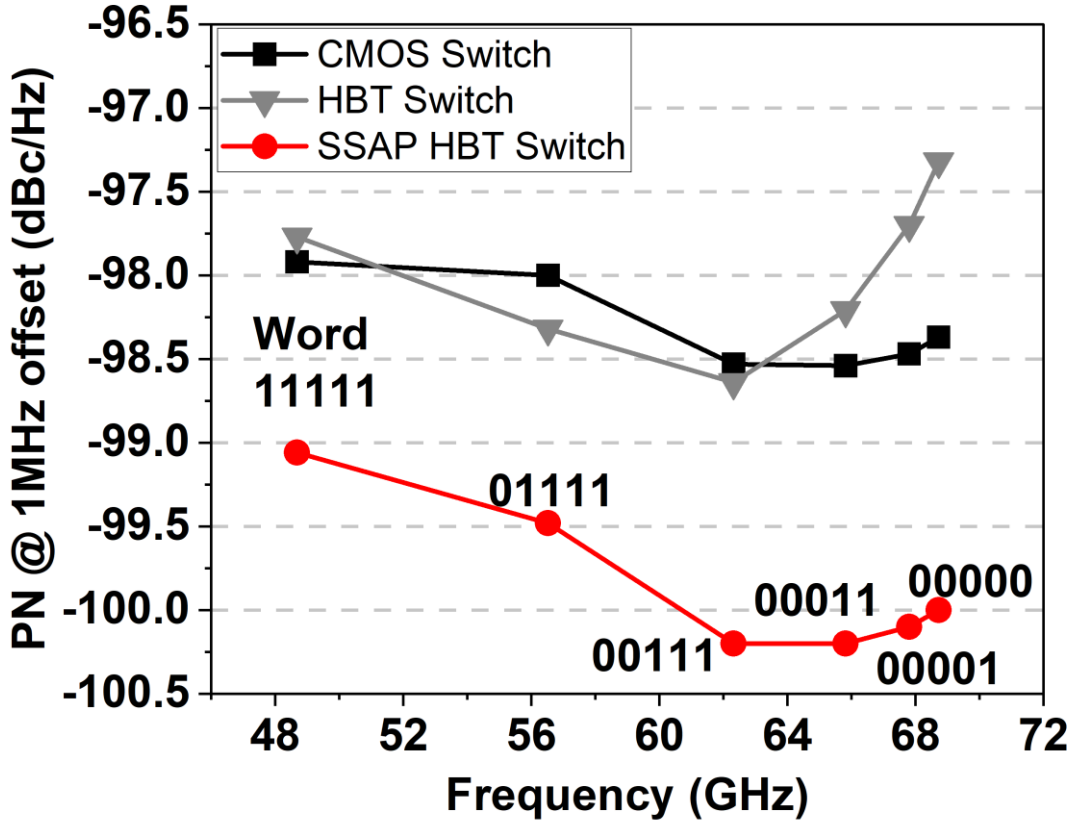
Proposed SSAP HBT switch

Switched Capacitor Bank Comparison

- The proposed SSAP capacitor bank shows 29% higher Q and 1.5 dB PN improvement compared to the CMOS pair



<Quality factor comparison>



<Phase noise comparison>

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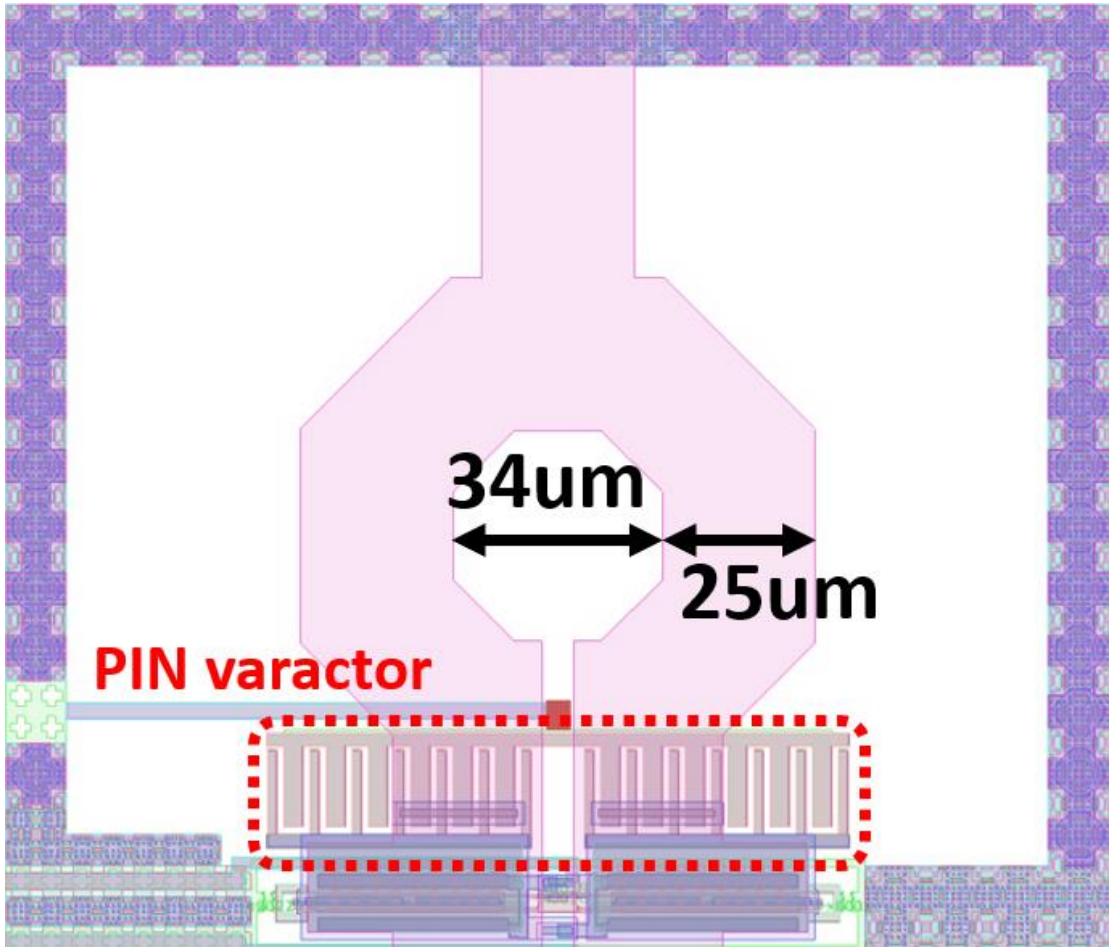
Inductor and Varactor Layout

- 49.4 pH with Q of 27.6 at 30 GHz Inductor
  - low PN and wide FTR

$$FTR = 2\frac{\sqrt{\Delta C_{max} + C_{fix}} - \sqrt{C_{fix}}}{\sqrt{\Delta C_{max} + C_{fix}} + \sqrt{C_{fix}}}$$

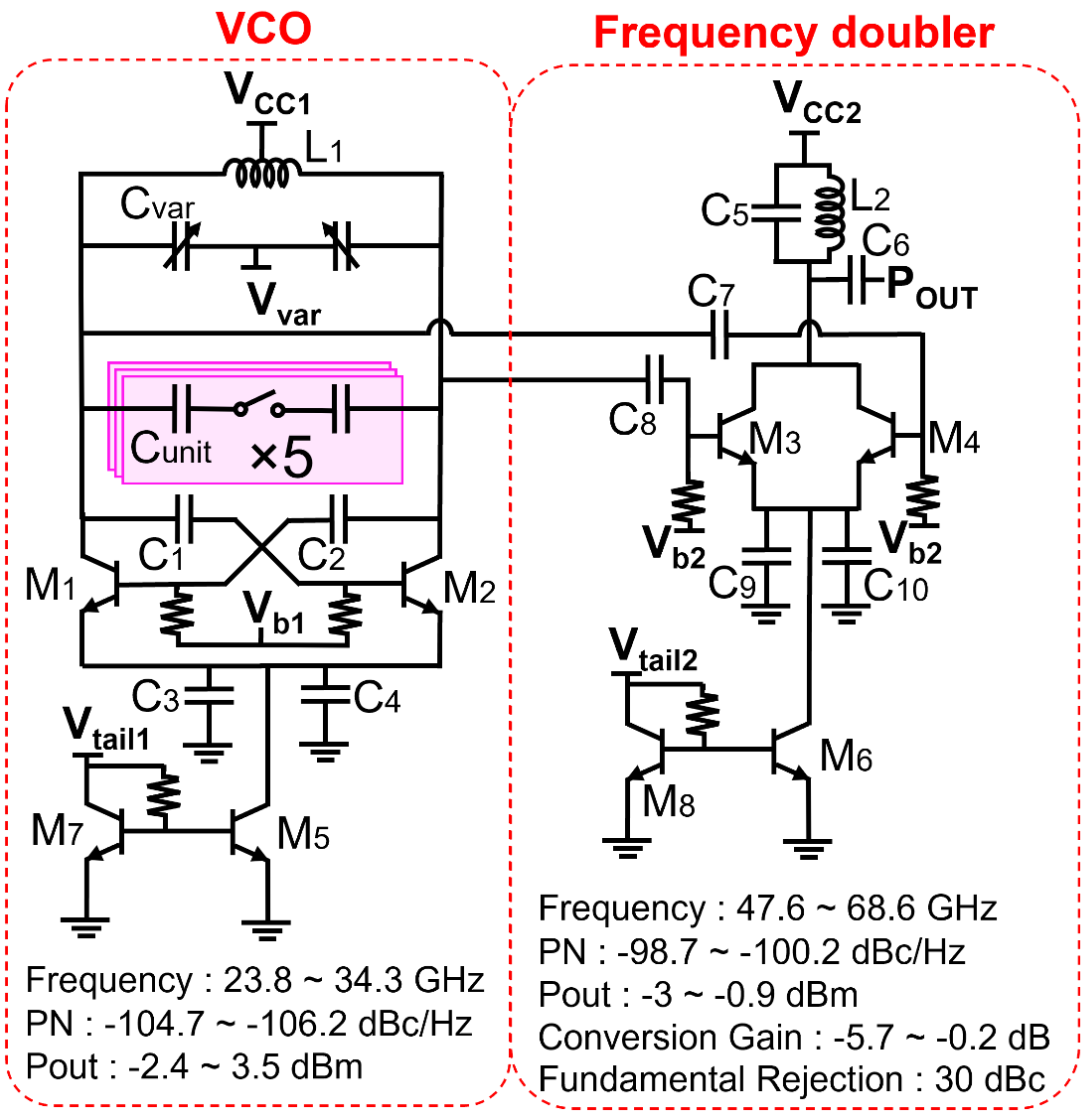
$$PN\,(\Delta w) \propto \frac{w^3 L}{A^2 Q}$$

- A PIN-diode varactor
  - 146.7 ~ 200 fF at 0V ~ 2.3V
  - linear voltage characteristics
- Minimized the length of the transmission lines



Schematic and Simulation Results

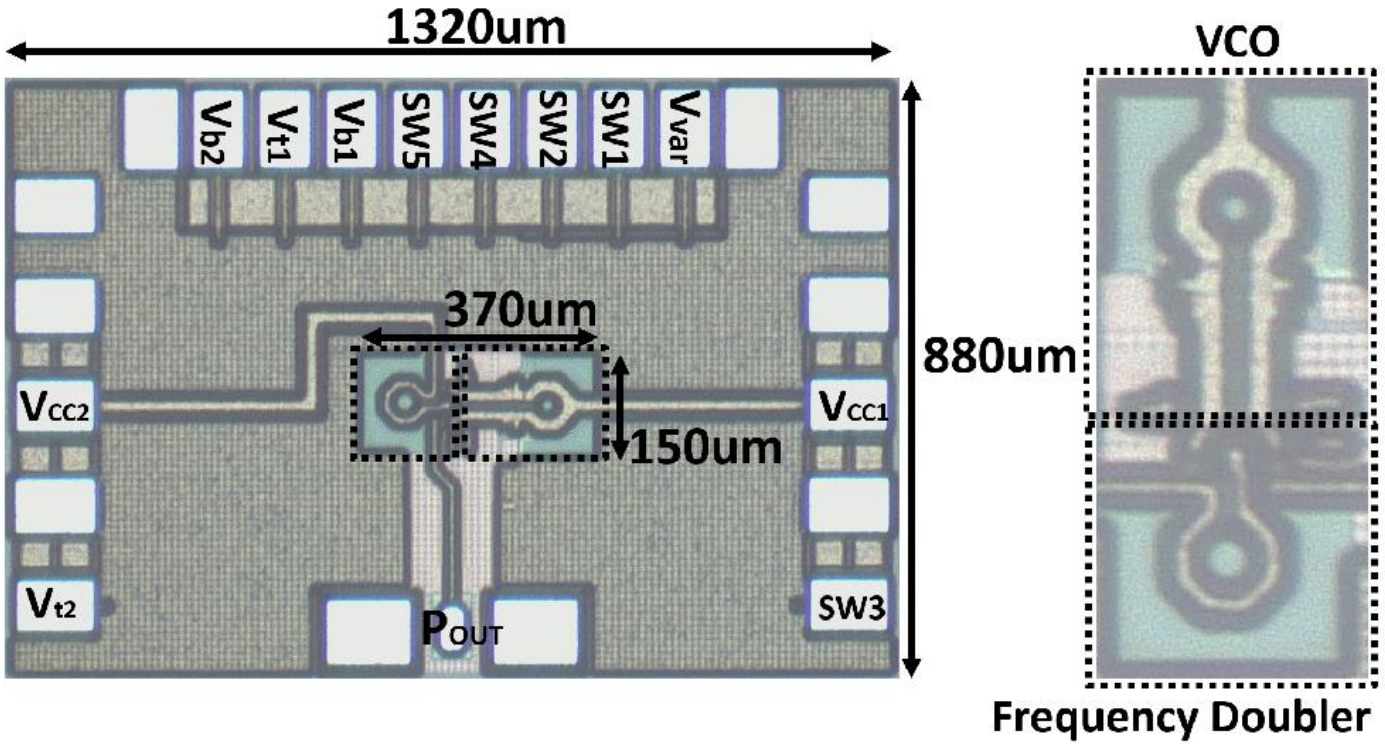
- 5-bit SSAP capacitor bank
- Class C type VCO
  - Low PN
- Independent push-push doubler
  - High Fundamental Rejection



Component name	Value
L_1	49.4 pH
L_2	69 pH
C_{var}	146.7 fF – 200 fF
C_{unit}	25.4 fF
C_1, C_2	270 fF
C_3, C_4	450 fF
C_5	83 fF
C_6	357 fF
C_7, C_8	270 fF
C_9, C_{10}	405 fF
M_1 – M_6	16 μm
M_7, M_8	2.6 μm

Chip Micrograph of the VCO

- 130-nm GlobalFoundries 8XP SiGe BiCMOS process
- Compact die size : 370um × 150um = 0.055mm^2



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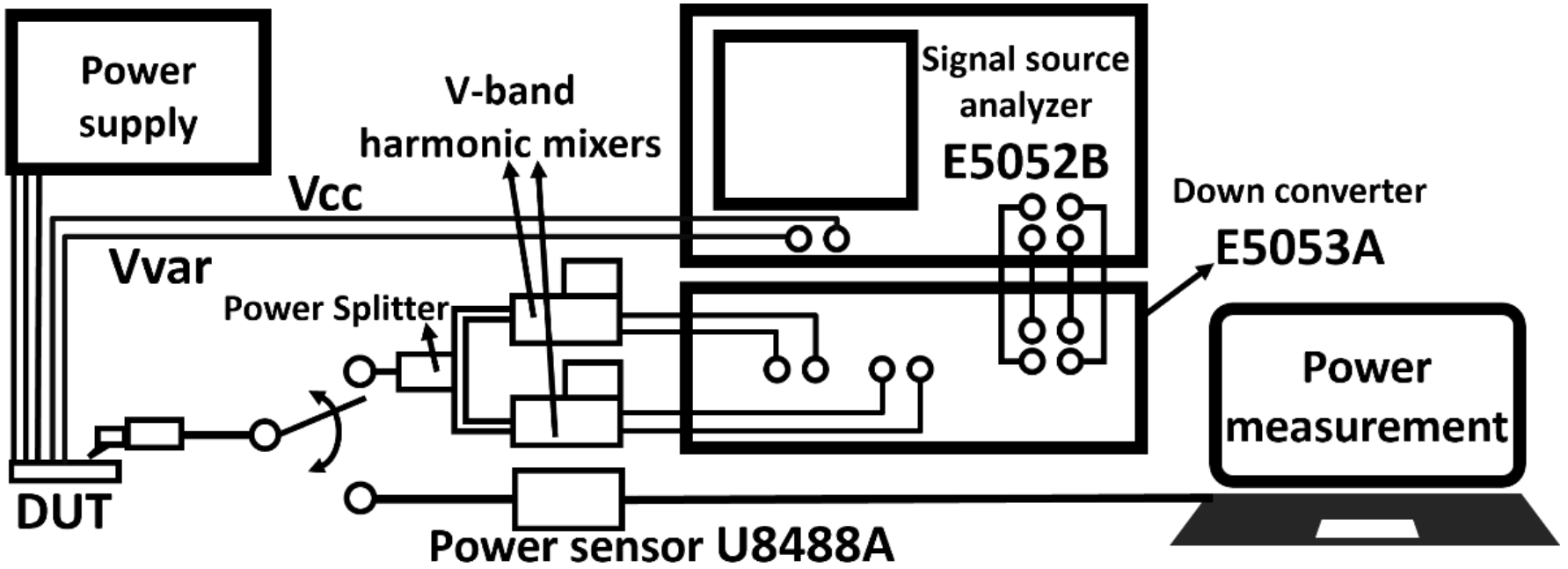
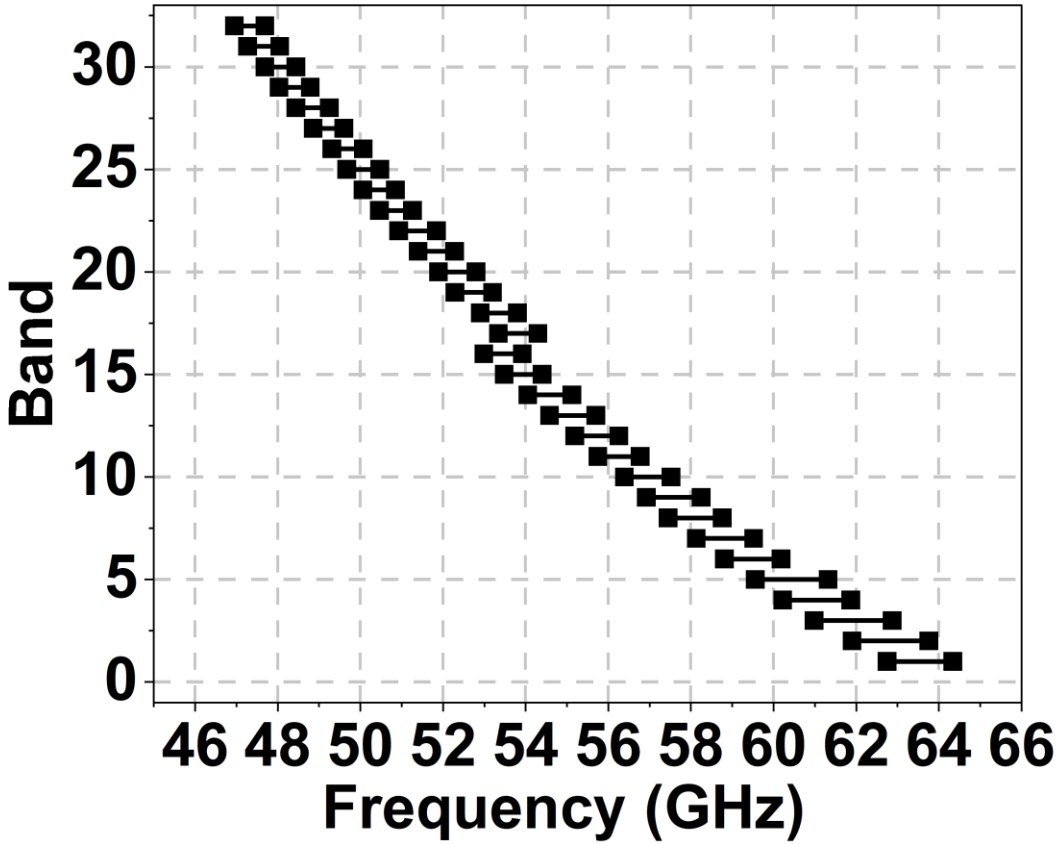
Measurement Setup

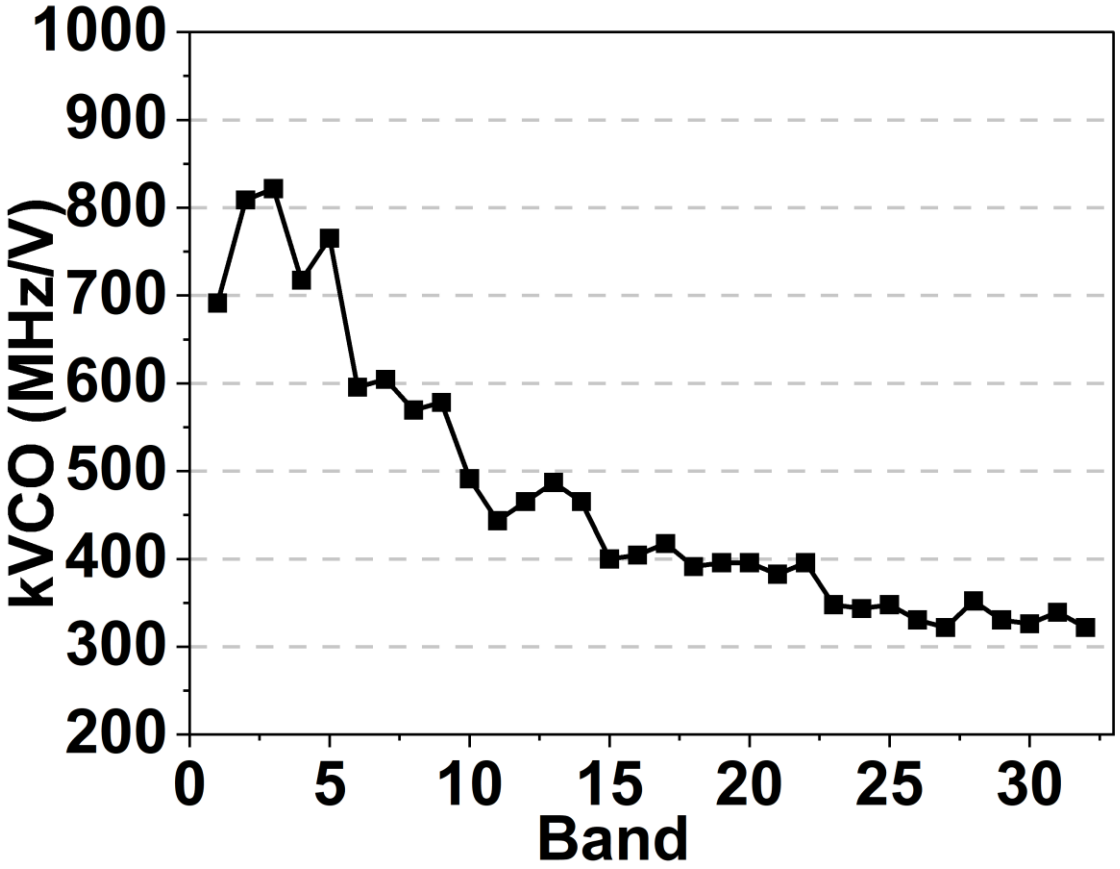
- Keysight E5052B was used to measure operating frequency and the accurate phase noise
- The output power of the oscillator was measured with the Keysight power sensor (U8488A)



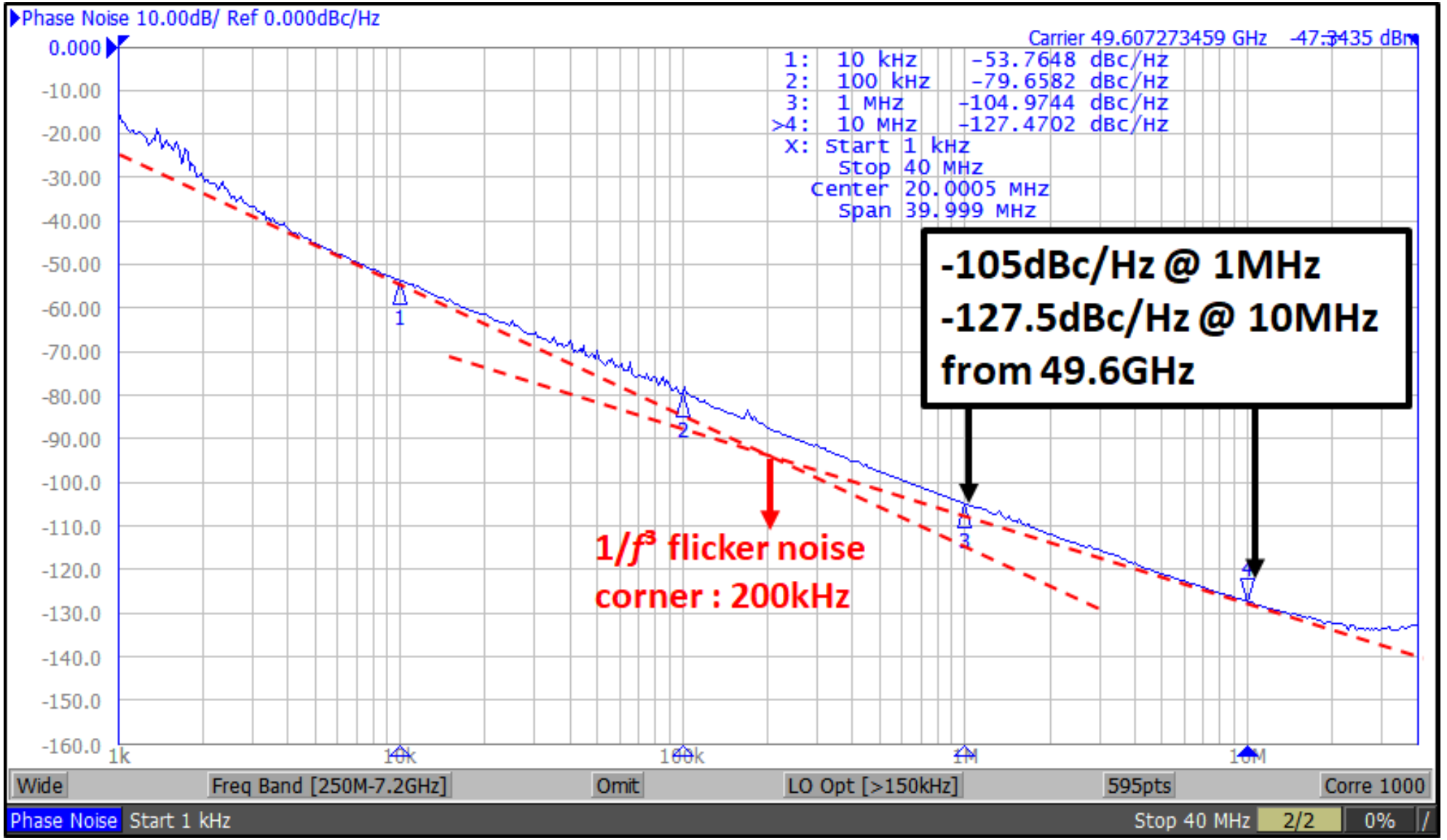
Measured FTR and kVCO

- Oscillation frequency covers 47 GHz to 64 GHz (FTR : 31%)
- kVCO is 470 MHz/V on average, with 820 MHz/V at maximum

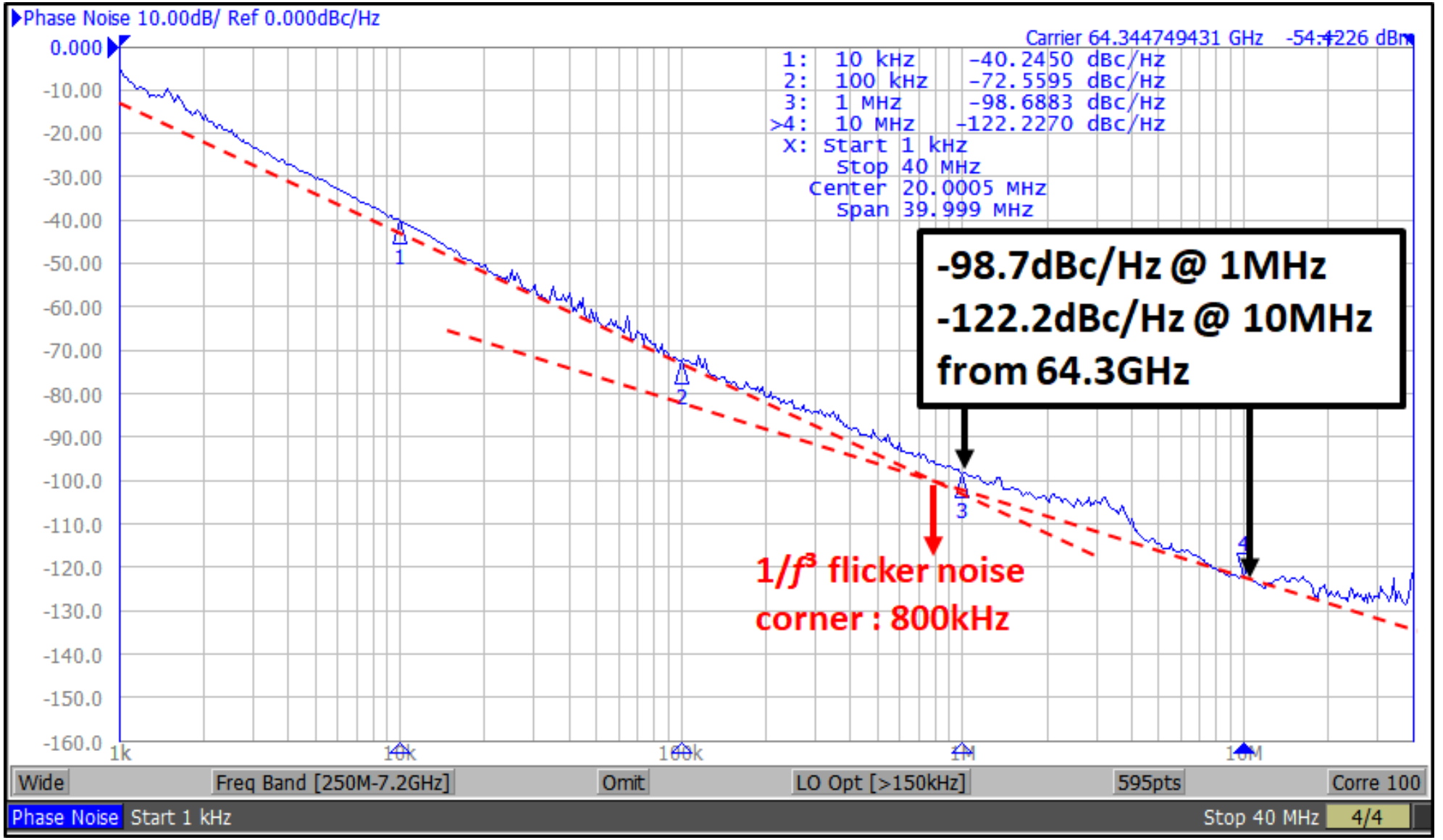




Measured Phase Noise

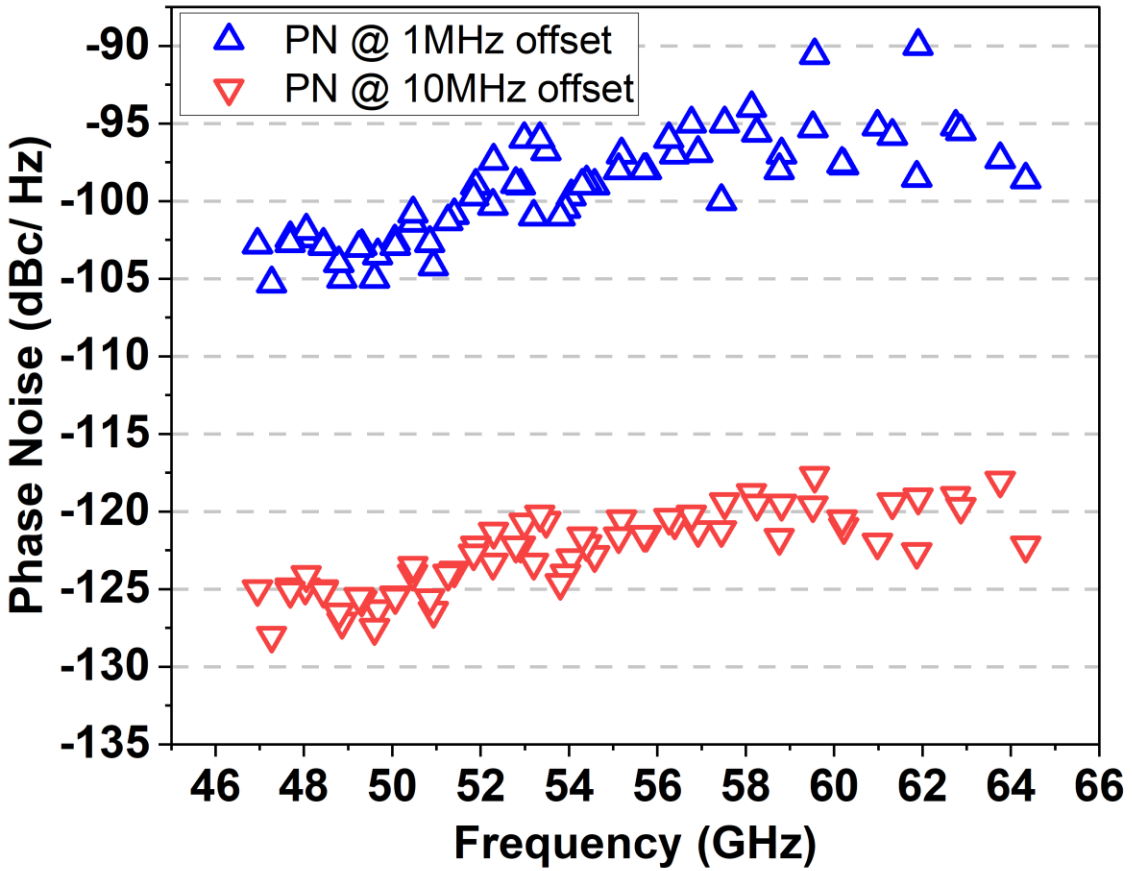


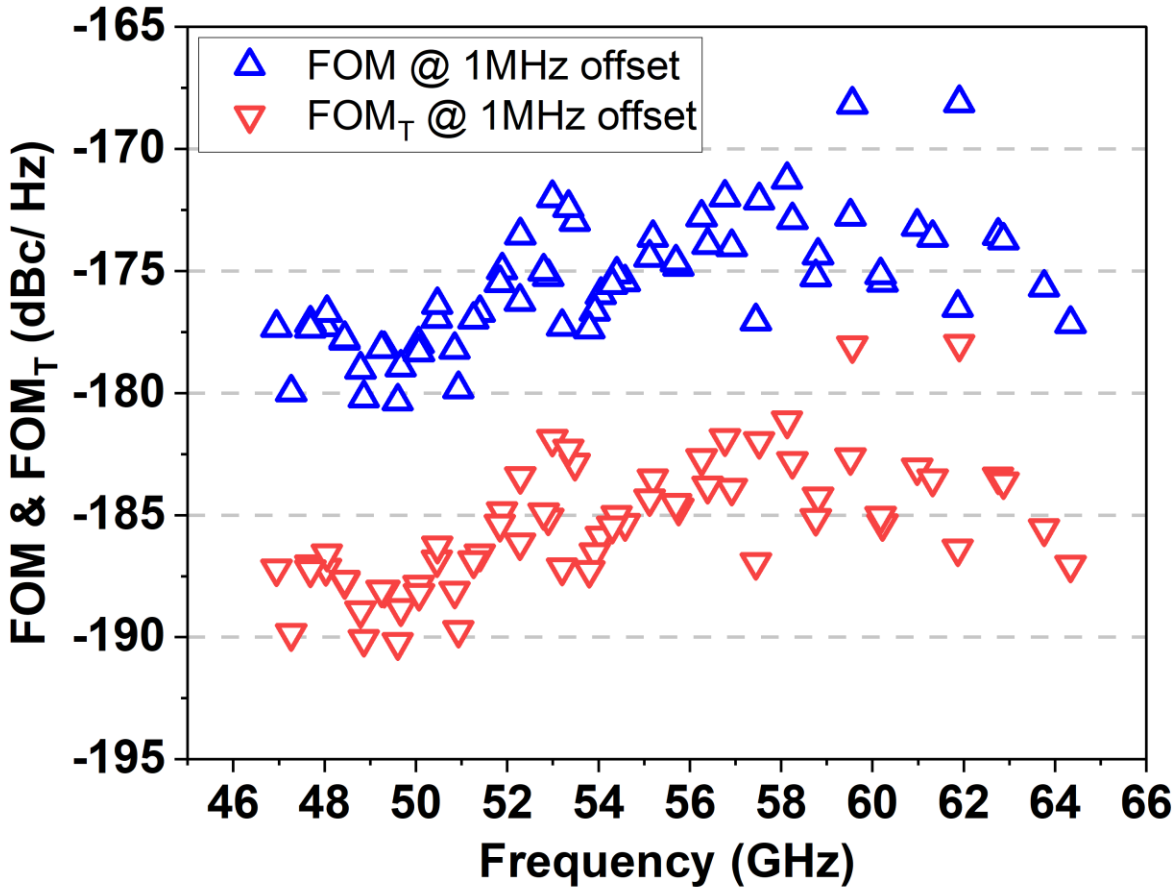
Measured Phase Noise



Measured PN and FOM

- PN @ 1MHz : -95 to -105 dBc/Hz
- FOM @ 1MHz : -171.3 to -180.3 dBc/Hz





Comparison Table

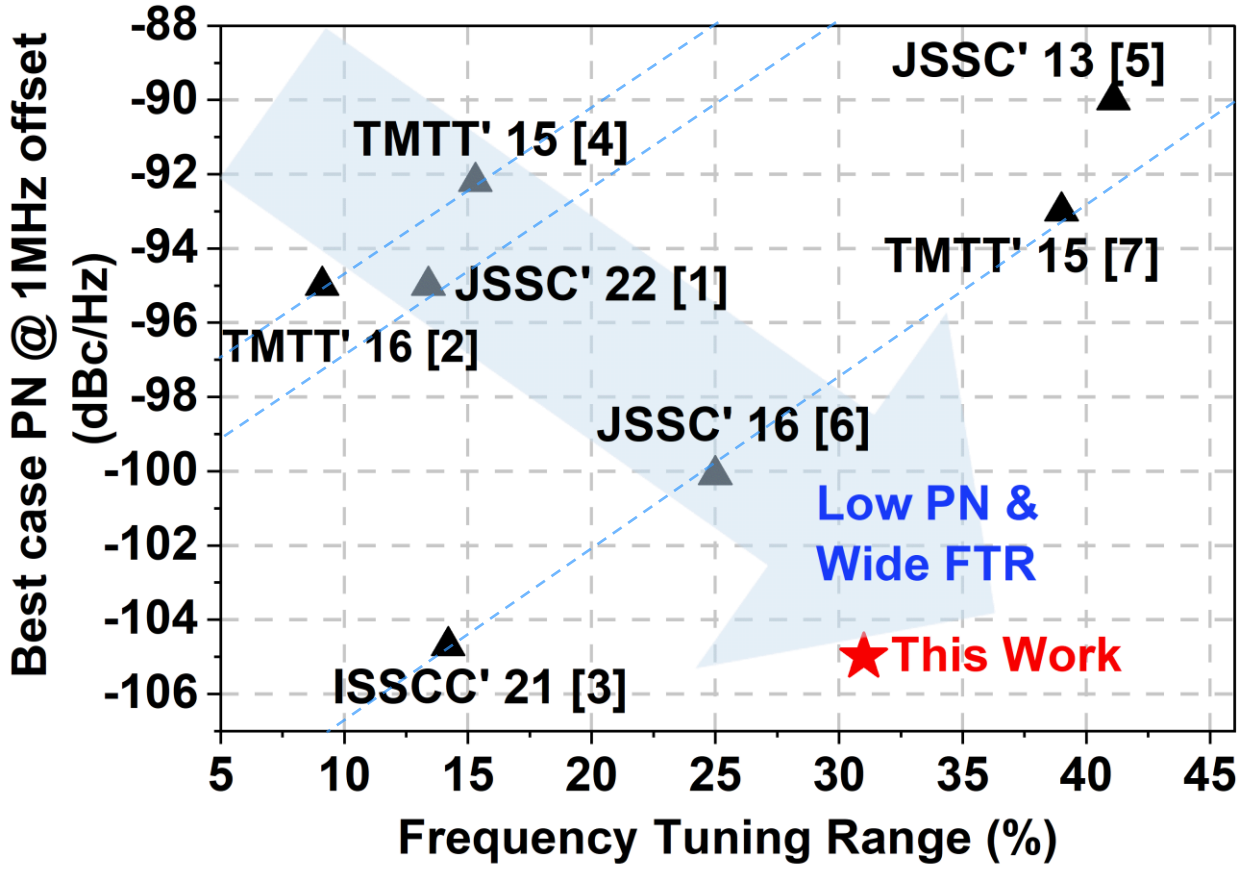
Reference	This Work	JSSC' 22 [1]	TMTT' 16 [2]	ISSCC' 21 [3]	TMTT' 15 [4]	JSSC' 13 [5]	JSSC' 16 [6]	TMTT' 15 [7]
Technology	**130nm SiGe**	28nm CMOS	95nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	65nm CMOS
Number of Cores	**1**	4	4	4	1	1	1	1
Tuning Range (GHz)	**47 to 64.3 (31.2%)**	55 to 62.8 (13.4%)	51.7 to 56.6 (9.1%)	52.4 to 60.4 (14.2%)	55.1 to 70.4 (24.6%)	57.5 to 90.1 (44.2%)	48.4 to 62.5 (25.4%)	47.6 to 71 (39.5%)
Output Power (dBm)	**-7 to 0**	-5 to -1	NA	NA	-15 to -10	-20 to -25	-14 to 6	NA
Power consumption (mW)	**58 to 78**	15.3	24	22.5 to 23.6	21.5	8.4 to 10.8	10.5	8.9 to 10.4
PN @ 1MHz (dBc/Hz)**	**-105**	-95	-95.5	-104.7	-92.2	-86*	-100.1	-92*
PN @ 10MHz (dBc/Hz)**	**-127.5**	-121.7	-119.2	-130*	-115	-112.2	-122.3	-113.4
FOM @ 1MHz (dBc/Hz)**	**-180.3**	-178	-176.7	-186.5	-174.9	-173.9*	-181.5	-176*
FOM @ 10MHz (dBc/Hz)**	**-182.8**	-184.7	-180.4	-191.8	-177.7	-180	-183.7	-179
FOM$_T$ @ 1MHz (dBc/Hz)**	**-190.2**	-180.7	-175.9	-189.6	-182.7	-186.8*	-189.6	-187.8*
FOM$_T$ @ 10MHz (dBc/Hz)**	**-192.7**	-187.4	-179.6	-194.9*	-185.5	-192.2	-191.8	-190.3

$$FOM = PN(\Delta f) + 10\log\left(\frac{P_{DC}}{1mW}\right) - 20\log\left(\frac{f_{osc}}{\Delta f}\right), FOM_T = FOM - 20\log\left(\frac{FTR(\%)}{10\%}\right)$$

* estimated from the Figure; ** Reporting best-case for each publication

PN and FTR Comparison

- Proposed VCO achieved both low PN and wide FTR



<Comparison of PN and FTR with recent 50–63GHz state-of-the-art VCOs>

Summary

- The first VCO using the novel Series-Shunt Anti-Parallel SiGe HBT Switches
  - Symmetric structure
  - 29% higher Q than CMOS pair
- Achieved wide FTR of 31% and low PN of -105 dBc/Hz at 1 MHz offset at 50 GHz
  - FOM_T of -190.2 dBc/Hz at 1MHz offset
- An attractive candidate topology for V-band VCO applications