Tu2B-3

GaN SLCFET Technology for Next Generation mmW Systems, Demonstrating Pout of 10.87 W/mm with 43% PAE at 94 GHz

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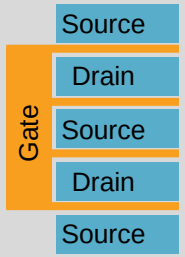
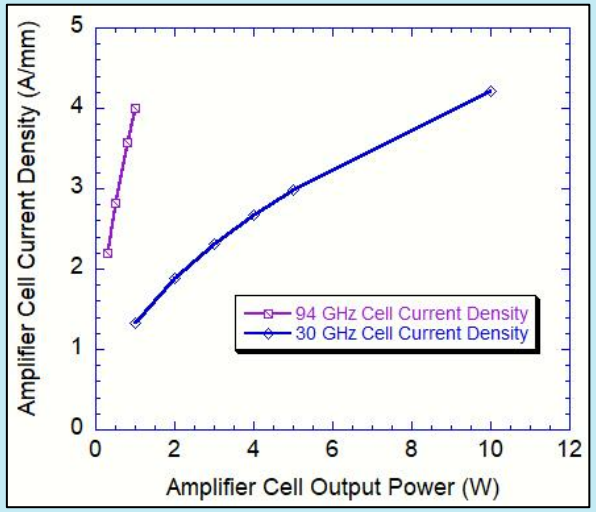
Increasing Output Power Densities at mmW Frequencies Requires Increasing Current Densities

- Next generation RF systems desire higher output powers at mmW frequencies
- mmW frequencies constrain amplifier cell sizes
- 50 Ω impedance of amplifier cell desired in order to maximize efficiency (input/output matching)
- Increased current densities required for high powers to maintain desired cell impedance and maximize operating bandwidth and power efficiency

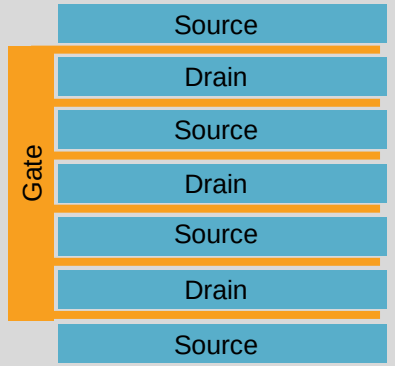
The Compact Amplifier Cells for mmW Applications Require Current Densities of 3-4 A/mm to Maintain 50 Ohm Device Impedance at High Output Power Levels

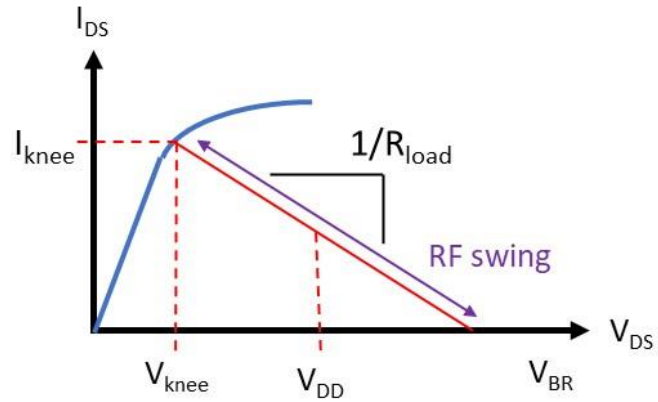
Notional 94 GHz amplifier cell
4 x 25 µm fingers
0.1 mm periphery





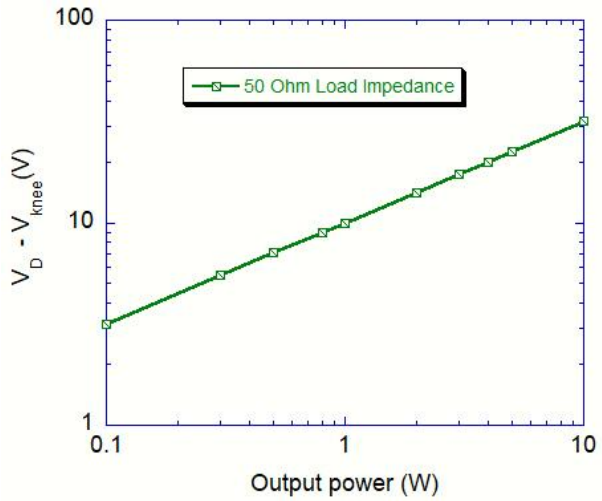
Notional 30 GHz amplifier cell
6 x 50 µm fingers
0.3 mm periphery





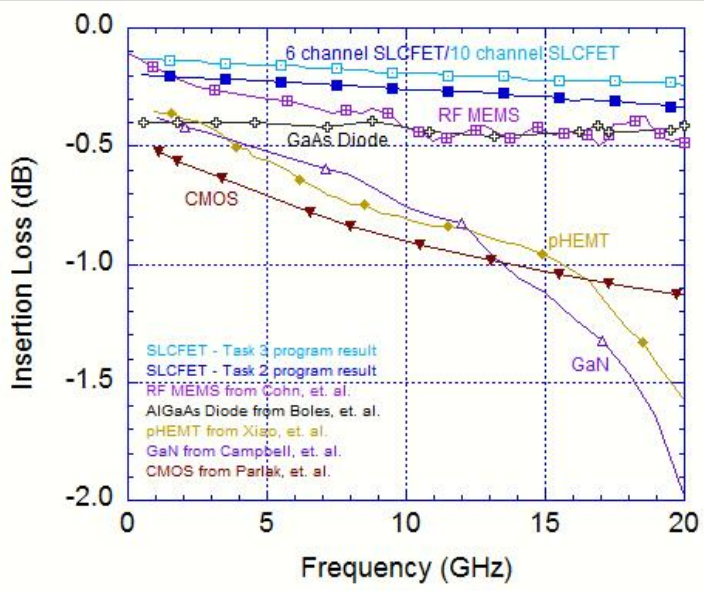
$$Output\ RF\ Power \sim \frac{(V_{DD} - V_{knee})I_{knee}}{4}$$

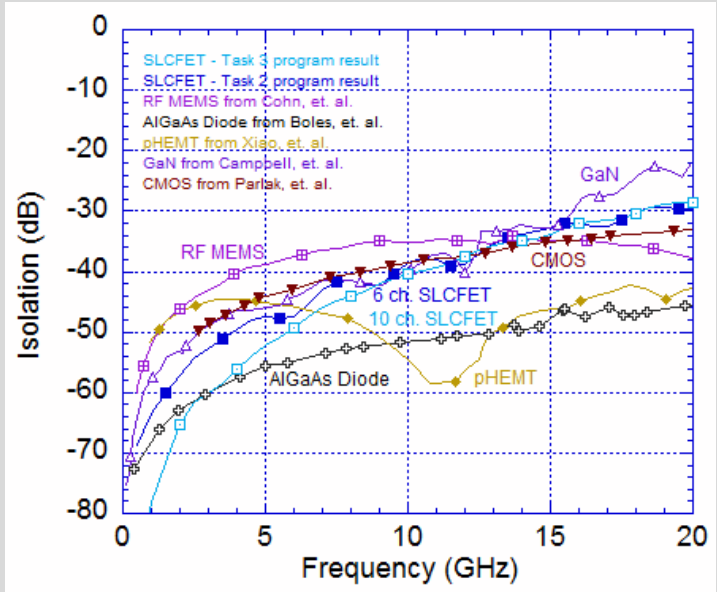
$$R_{Load} \sim \frac{2V_{DD}}{I_{knee}}$$



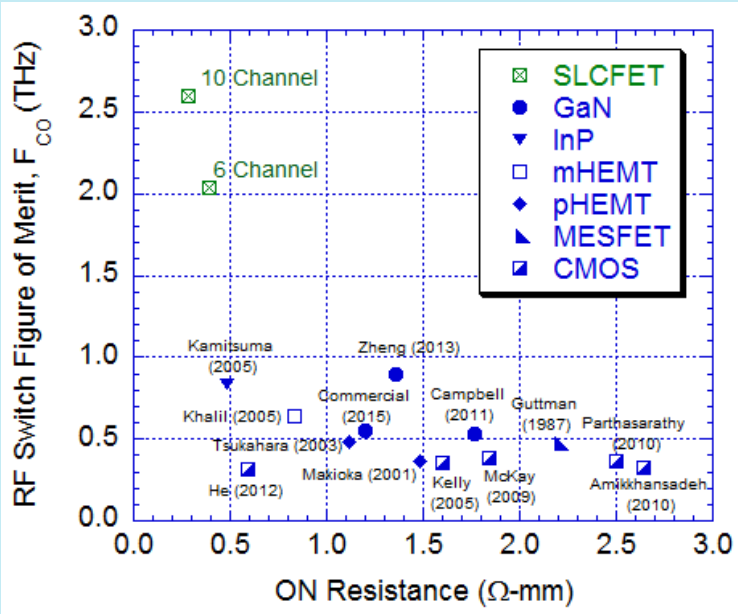
SLCFET = Superlattice Castellated Field Effect Transistor, Demonstrated Superior Wideband RF Switch Performance

0.1-20 GHz Single Pole Double Throw Switch Technology Comparison





RF Switch FoM Comparison

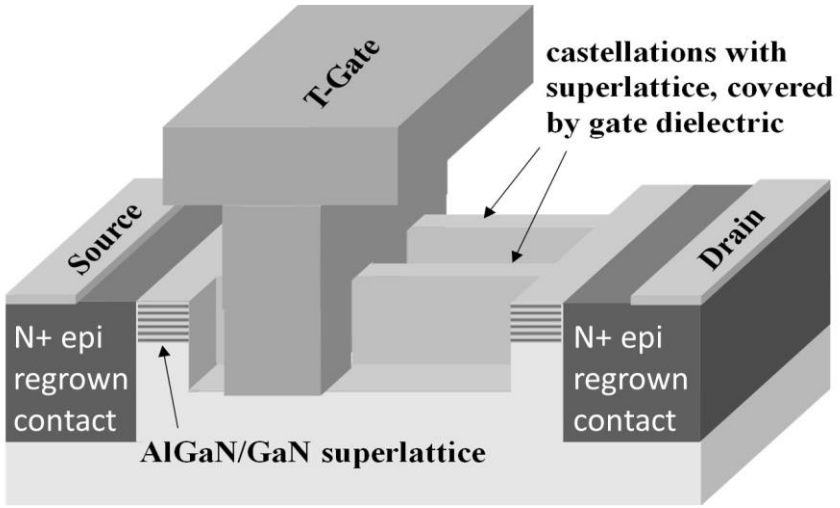


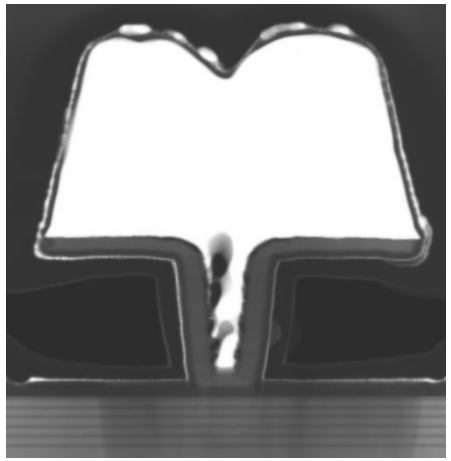
From ***[Howell, et. al. IMS 2016]***

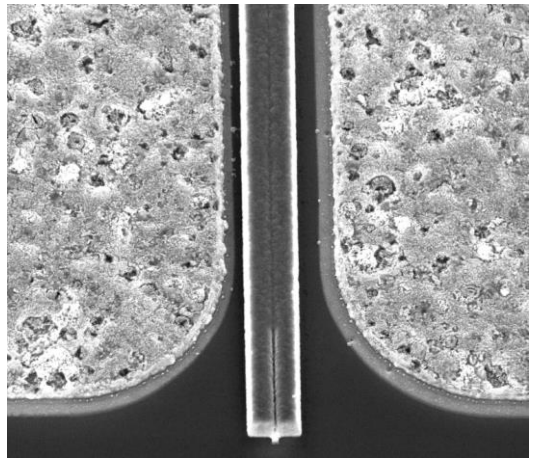
- Superlattice supports multiple stacked 2DEG channels between source and drain
- 3D castellated gate provides electrostatic control of stacked channels
- Structure decouples OFF capacitance from ON resistance, giving superior RF switch performance
- Structure provides method for efficiently scaling current density to support high output power densities in amplifiers

Original SLCFET RF Switch Process Leveraged to Create a Highly Capable RF Amplifier Process

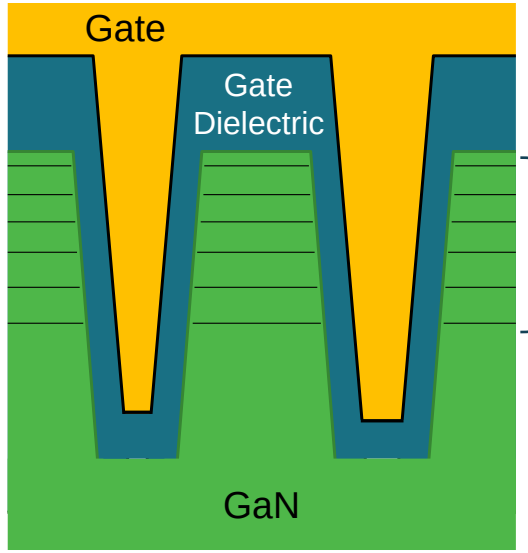
- 3D T-gate process has been developed that is compatible with the narrow aspect ratios of the SLCFET castellations
- SLCFET amplifier remains a fully sidewall gate actuated device, as is the SLCFET RF switch device
- Nanoribbon dimensions, castellation duty cycle and gate dielectric each optimized for SLCFET amplifier





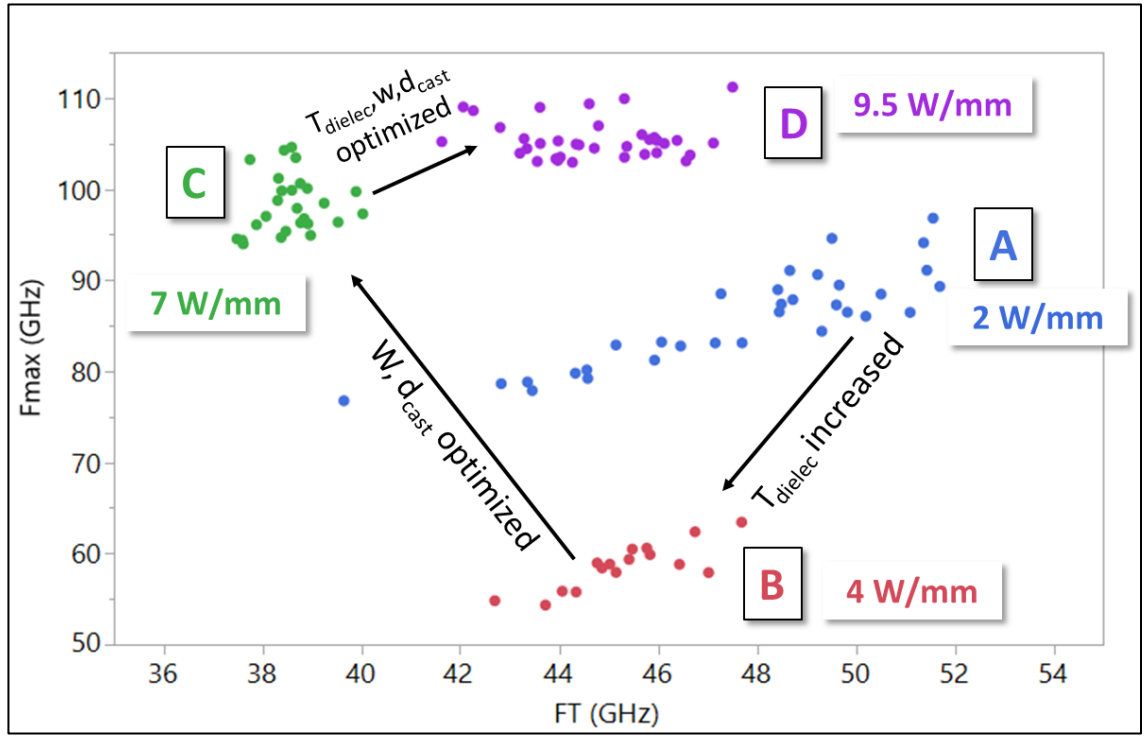


Cross-sectional view



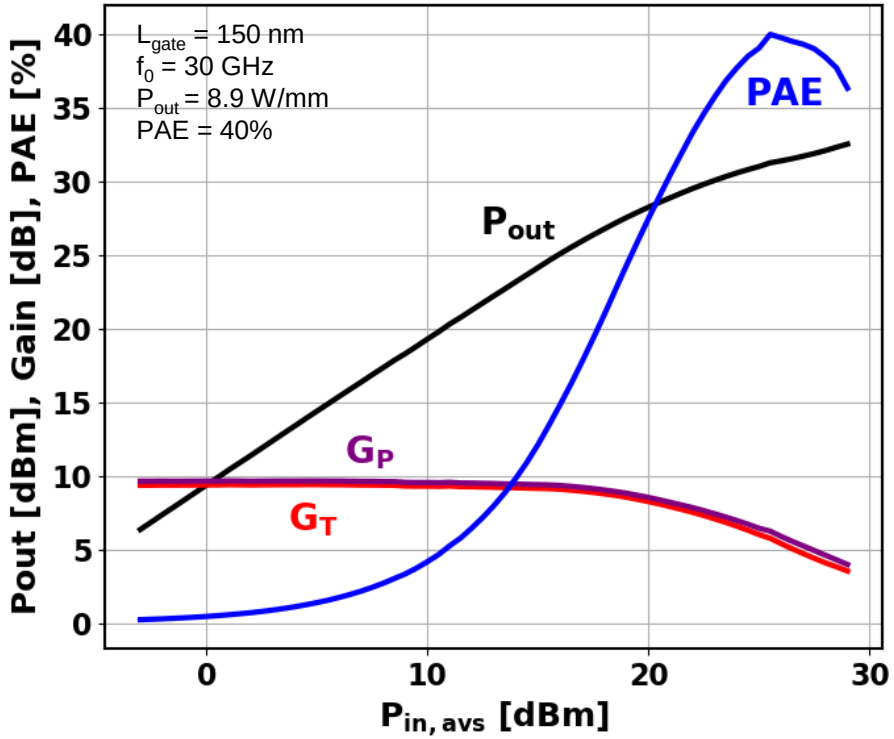
AlGaN/GaN Superlattice

SLCFET Previously Demonstrated it's Capabilities for Efficient, High Power Density Amplification at 30 GHz



SLCFET device structure was re-optimized from its original RF switch function to be a high power density mmW amplifier

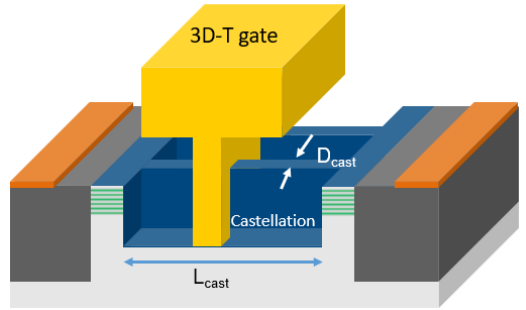
Phase 1 DREaM Program Result

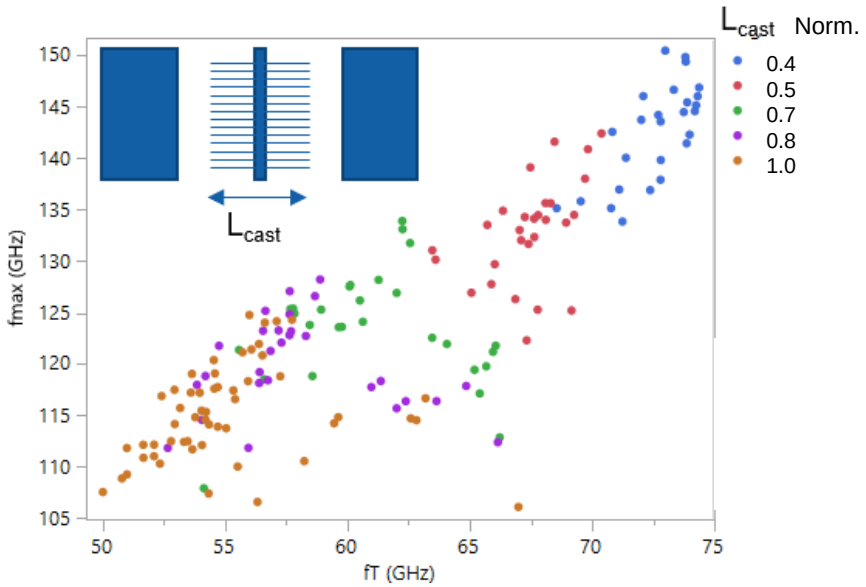


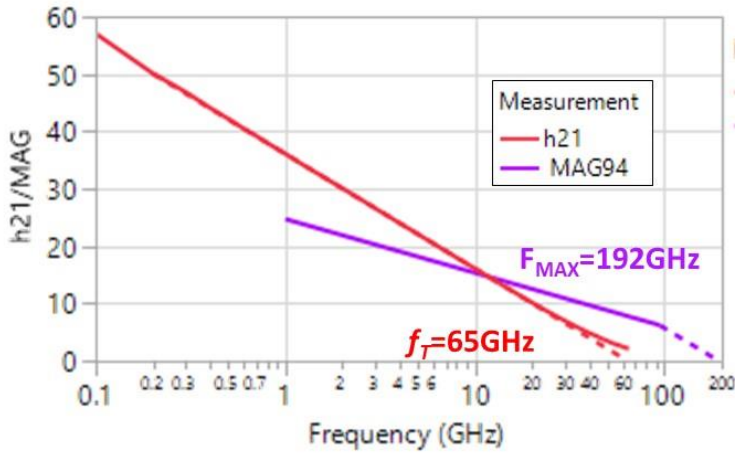
From ***[Chang, et. al. IMS 2020]***

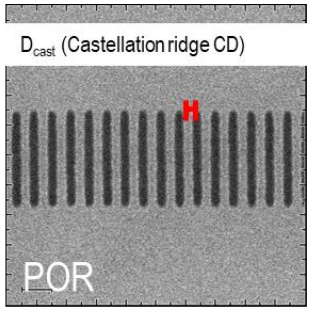
SLCFET Castellation Structures Now Optimized to Maximize Power Density and Gain at W-band

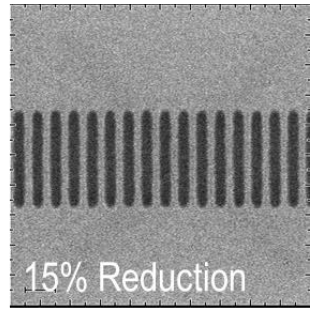
- Phase 2 DREaM program increased frequency target from 30 GHz to 94 GHz
- Electrostatics maintained for smaller gate lengths by reducing castellation widths
- Source resistance reduced by scaling of castellation length
- Improves device f_T/F_{MAX} performance to 65/192GHz

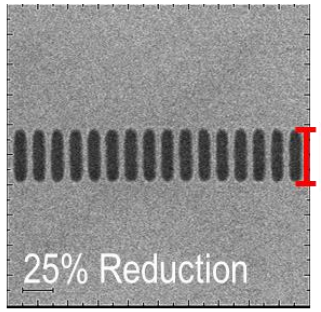






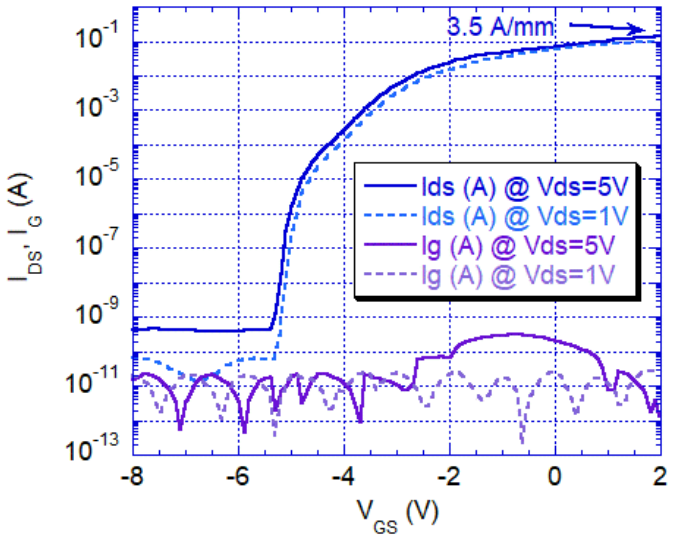


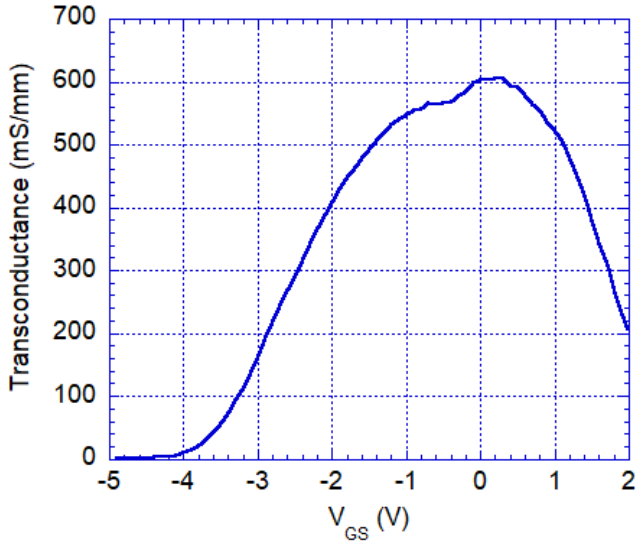




L_{cast} (Castellation length CD)

SLCFET Structure Facilitates Extremely High Device Charge Densities, from 2DEGs and Sidewall Accumulation

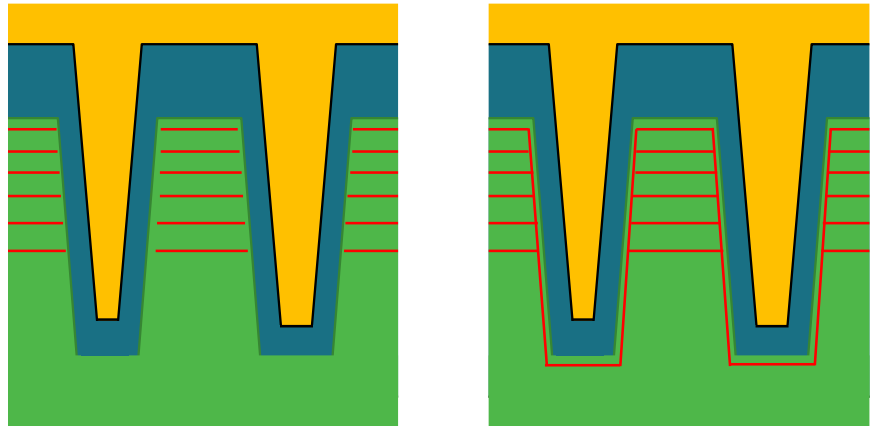


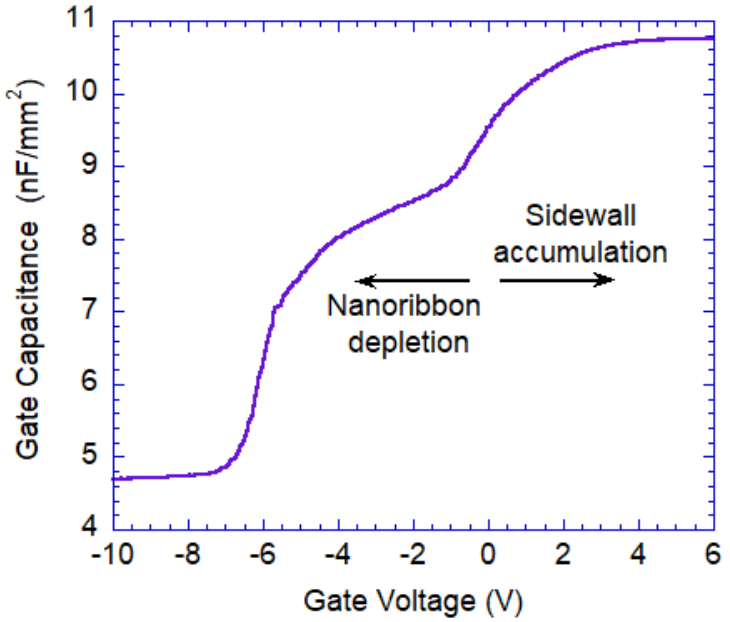


- Superlattice with stacked 2DEG provides ~1.3e13 cm^{-2} carriers per heterojunction, for a total depletion charge density ~8e13cm^{-2}
- Sidewall accumulation under small forward bias increases total charge density further ~40%
- Depletion (2DEG) and accumulation (sidewall) charges form distinct humps in both transconductance and gate capacitance vs gate bias

2DEG depletion mode charge

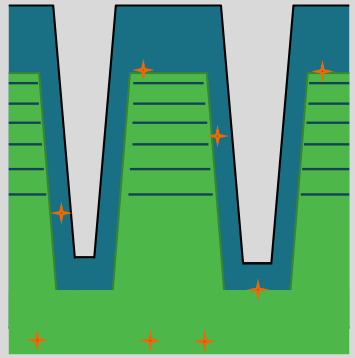
Sidewall accumulation and 2DEG enhancement mode charge





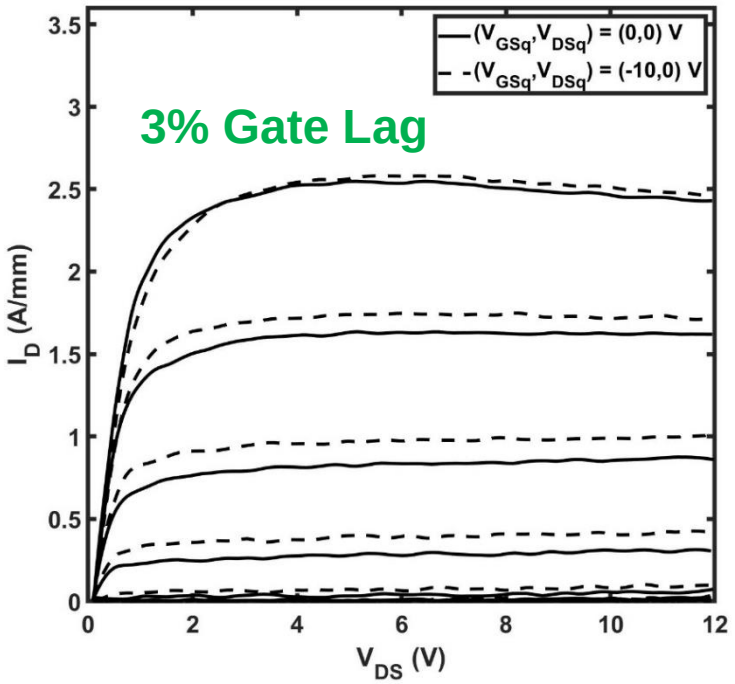
SLCFET's Intrinsically Low Dispersive Property Enables High Power Performance

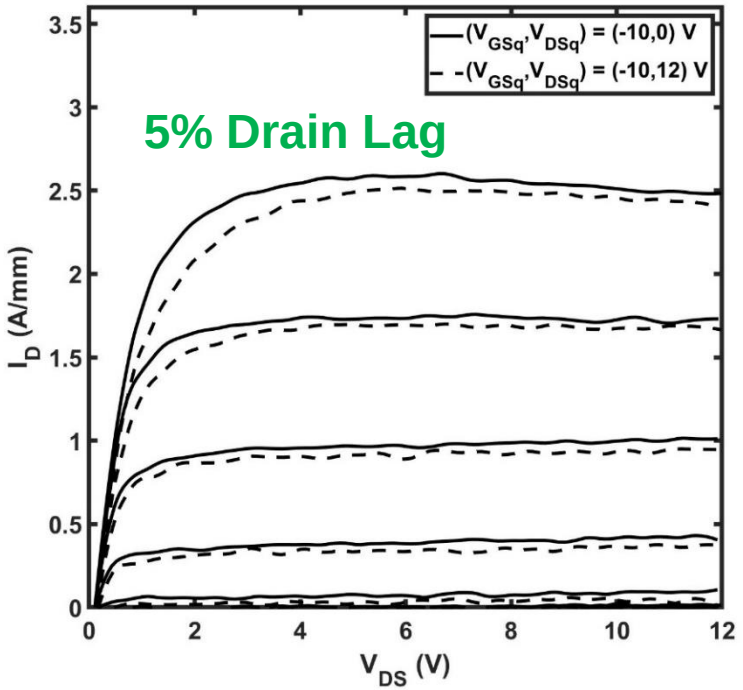
- 3D stacked heterojunctions act to screen surface, interface and/or buffer traps from the majority of the current carrying channels
- Applied surface passivation further minimized current dispersion effects
- Extremely low gate and drain lag enable RF swing to fully utilize the high current density provided by the SLCFET structure

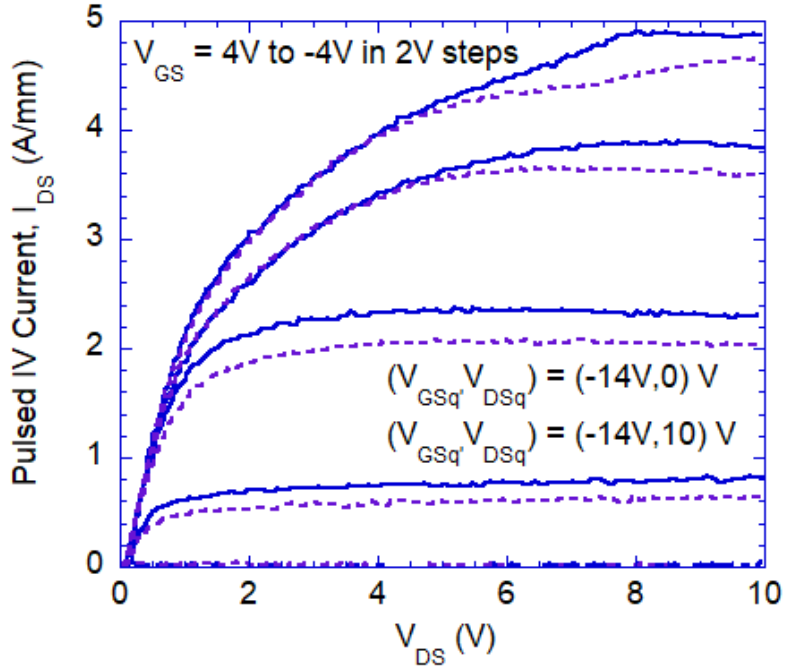


Tightly stacked 2DEG self-shield channel charge from the parasitic gating effect of traps that cause dispersion and RF current collapse

Interface, Surface, or Buffer trap



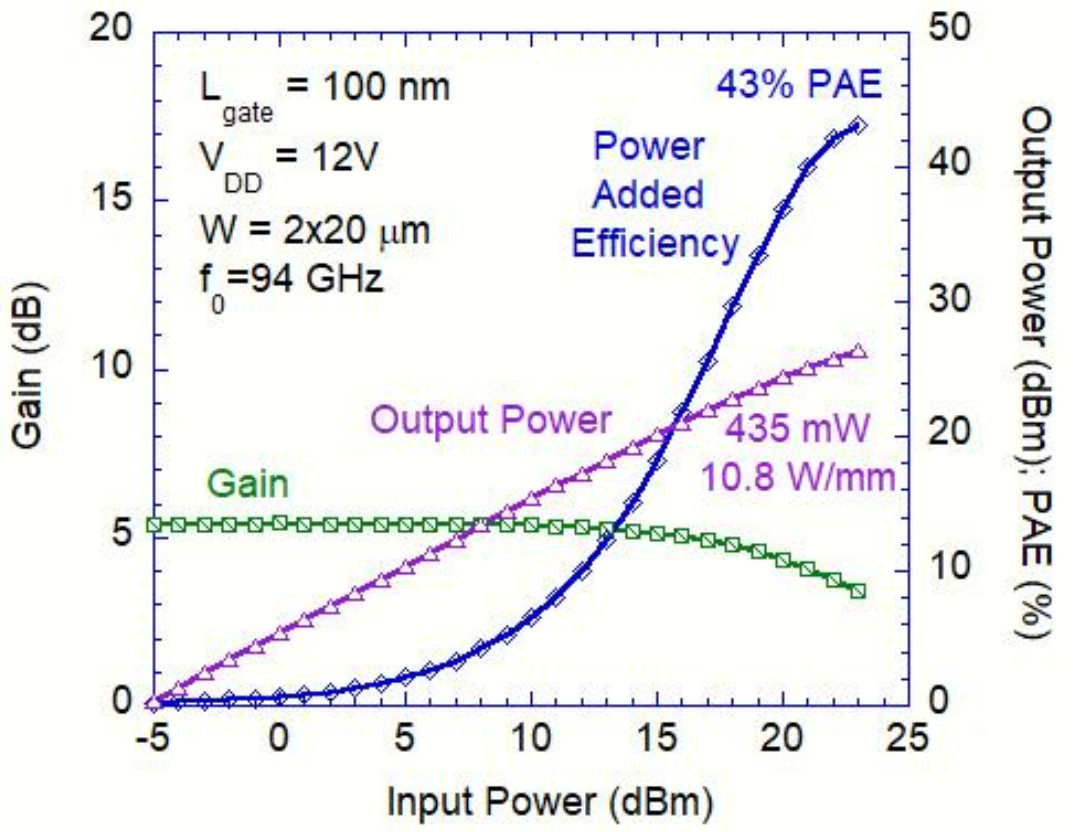




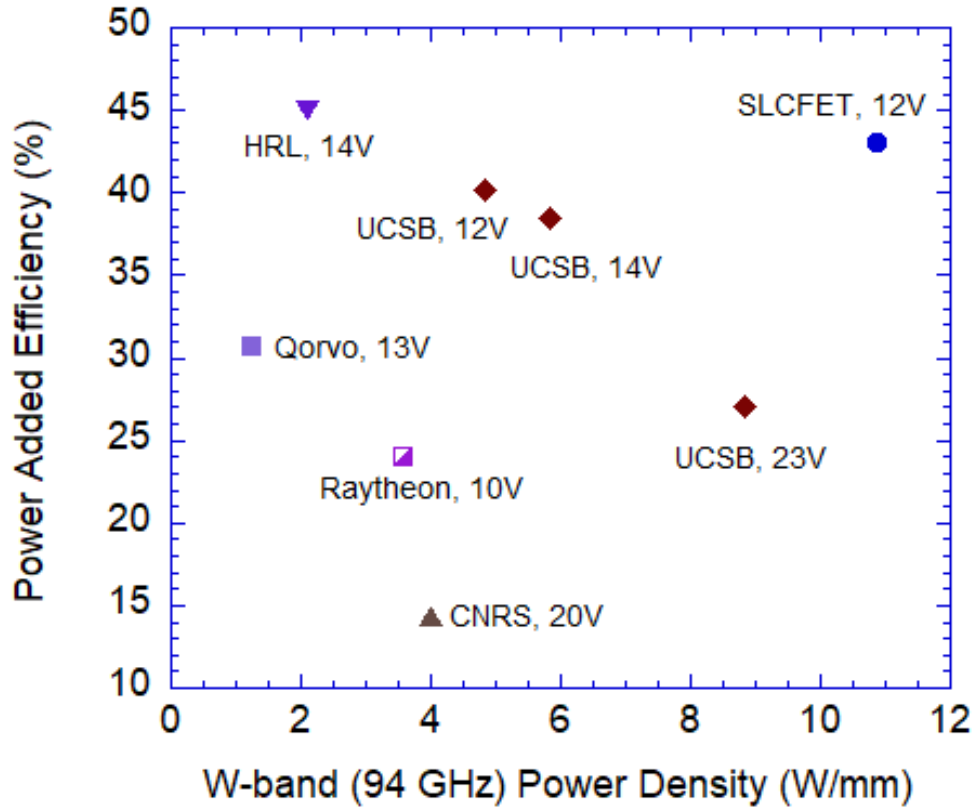
SLCFET Amplifier Demonstrates Record 10.875 W/mm and 43% PAE at 94 GHz under Load Pull

Unique SLCFET geometry and process improvements enables high performing W-band amplifier

Load-pull measurement of SLCFET at W-band



Comparison of reported GaN W-band load-pull power densities vs. PAE



Summary

- A GaN SLCFET based amplifier was optimized for output power density and efficiency at mmW frequencies
- The superlattice structure and 3D device geometry provides
  - Extremely high current densities
  - Minimal dispersion/current collapse
  - Excellent electrostatic control (high output impedance)
  - Low parasitic source and contact resistances (low knee voltage)
- Load pull measurements at 94 GHz on a 2x20 µm test cell with a 100 nm T-gate demonstrated **10.875 W/mm (435 mW)** with a simultaneous **PAE of 43%**
- SLCFET technology offers new capabilities to achieve high efficiency, high power density mmW amplification monolithically with low loss RF switching
  - New possibilities now exist to realize high performance, agile, wideband, reconfigurable RF/mmW front ends

Acknowledgements

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  - Work performed in the DARPA-MTO DREaM program under contract # FA8650-18-C-7805
  - The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government
- Dr. Matthew Guidry and Christopher Clymore at UCSB for taking load pull measurements
- Dr. Nicholas Miller and Ryan Gilbert at AFRL for taking load pull measurements