A Low Power V-Band LNA with Wide Supply Voltage Range Exploiting Complementary Current Reuse and Power Efficient Bias Point

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Power Constrained Small Sat.

- Emerging IoS apps. leverage cube-sat and other small devices
  - <10cm² solar cells on a 1U device
  - Typically operate between 5-10W
- F.S.P.L \( \propto 1/f^2 \) for a fixed Tx and Rx antenna aperture
  - High frequencies -> mmW communications
- If \( T_{on}(Rx) >> T_{on}(Tx) \) Rx power consumption can easily dominate
Power and Sensitivity in Arrays

- Array performance scales w.r.t the number of elements
  - EIS $\propto N_{\text{Elements}} + NF_{\text{Element}}$
- Power increases as $N_{\text{elements}}$ is increased
  - Linearly for digital phased arrays
  - Sub-Linearly for RF beamformers
- For a fixed EIS a $3\,\text{dB}$ $NF_{\text{Element}}$ increase doubles the required $N_{\text{Elements}}$

“Digital Phased Arrays: Challenges and Opportunities” Fulton et. al
Power Efficient Bias in mmW

- Typical mmW bias point
  - 150µA/µm for minimum NF$_{\text{Min}}$ @VDD=1V
    - IC=7 and gm/ID=7.8
  - 250µA/µm for maximum F$_{\text{max}}$ @VDD=1V

- Modern CMOS have very high F$_{\text{max}}$ even at low current densities
  - @IC=2 (43µA/µm) F$_{\text{max}}$$\sim$250GHz w/ gm/ID=11.8

- High linearity Systems
- Low power constraints
- Very high frequencies

- Power constrained systems
- Moderate RF Frequencies
Voltage and Current Scaling

- Power gain norm. to $P_{DC}$ defines amplifier efficiency
- Traditional bias of 250uA/µm and $V_{DD}=1V$ Eff=6
- Heavily scaled bias Eff=250
- 40X power reduction compared to standard bias point
Current scaling on S.S parameters

- **NF<sub>min</sub>** and **Gmax** both rapidly degrade as ID/W scales down
  - Lowering IC **increases** g<sub>m</sub>/I<sub>D</sub>
  - Lowering IC **decreases** g<sub>m</sub>/W
  - Lowering IC **decreases** (g<sub>m</sub>/C)
- Higher capacitance means higher Q-factor interfaces
  - High Q-factor interfaces means BW degrades (bode-fano)
Voltage scaling on S.S parameters

- Scaling supply voltage has weak impact on small signal
  - $G_{\text{max}}$ drops 0.4dB vs >5dB for ID/W scaling
  - $NF_{\text{min}}$ drops 0.3dB vs >2dB
  - IO impedances have very low variation w.r.t supply

\[
G_{\text{Max}} = \text{real}(Y_{22})
\]
\[
B_{\text{Out}} = \text{imag}(Y_{22})
\]

\[
G_{\text{max}} \approx 0.4\text{dB Variation}
\]
\[
NF_{\text{Min}} \approx 0.3\text{dB Variation}
\]
\[
G_{\text{out}} < 15\% \text{ Variation}
\]
\[
B_{\text{out}} < 5\% \text{ Variation}
\]
Current scaling on linearity

- $I_D/W$ scaling doesn’t inherently degrade TOI
  - IIP3 sweet spot occurs at much lower current densities than optimum $F_{max}$
- For high Z interfaces voltage bias dominates P1dB
- Current scaling has a weak impact on linearity
Bias scaling on linearity

- $I_D/W$ scaling doesn’t inherently degrade TOI
- $G_{gd}$ nonlinearity generates TOI at low $V_{DS}$ even if $V_{DS}>V_{DSAT}$ due to voltage gain
- Large signal compression (P1dB) is weakly effected by current scaling for high Z interfaces
- Voltage scaling however strongly degrades compression point
Voltage scaling and current reuse

• Adding additional regulation to enable voltage scaling decreases power efficiency and increases area

• Voltage levels are typically set by logic levels, IO or PA requirements
  • Current reuse implements voltage scaling which reduces power consumption

• Current reuse splits a single voltage domain into multiple subdomains sharing the same current
LNA Design

- Three stage differential LNA utilizing complementary current reuse, transformer based interstage coupling networks and capacitive neutralization
- Leverages integrated CMFB loops to track VDD/2 at output for maximum linearity
Complementary current reuse

- For many modern CMOS nodes NMOS and PMOS are nearly symmetric
  - $F_{\text{Max}} \approx 10\%$; $N_{\text{FMin}} < 0.2\,\text{dB}$
- Utilize both NMOS and PMOS for GM
- Inherent 2\textsuperscript{nd} order nonlinearity cancellation
- Ease of DC coupling, identical signals on all devices improves linearity compared to cascaded current reuse
LNA Input stage and bias

- Inductively degenerated common source input stage
  - Enabled use of lower coupling factor transformer on input
  - Lowered NF but drastically reduced input imbalance
- Dual neutralization $C_{GD}$ and $C_{DS}$ stabilize input
  - Additional path introduced by $L_s$
- Stage 1 uses 100uA/um bias for low noise, stage 2 and 3 use 45uA/um for low power
  - All stages biased at 100uA or below

<table>
<thead>
<tr>
<th>Stage</th>
<th>$G_{max}$</th>
<th>$NF_{min}$</th>
<th>$G_{max}/I_D$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stg. 1</td>
<td>16dB</td>
<td>2.3dB</td>
<td>2.2</td>
</tr>
<tr>
<td>Stg. 2/3</td>
<td>14dB</td>
<td>3dB</td>
<td>5.0</td>
</tr>
</tbody>
</table>

Typical Bias
- $G_{max}=16.4$dB
- $NF_{min}=2.2$dB
- $G_{max}/I_D=1.7$
Small signal measurements

13.6GHz BW across wide VDD range
8.6 to 13.3mW DC power consumption
<5dB NF
Performance comparison

Performance @ 60GHz

Power Gain
BW=13.6-13.7GHz
NF= 4.85-5.0 dB

2.7dBm
OP1dB @ 13.3mW

This work @1.3V 13.3 23.4 13.6 63 4.85 -19.7 0.6 40.1 0.138
This work @1.0V 10.8 21.9 13.7 63 4.9 -20.2 -5 39 0.138
This work @0.8V 8.6 20.4 13.6 63 5 -23.6 -9 38.1 0.138
Qui IMS 22 3.6 13.5 6.6 72 4.6 -16.3 -5.8 26.8 0.88
Shin RFIC 18 10.8 20 10.4 74 4 -22.8 -9.5 36.1 0.155
TMTT 20 9 20 12 76 4.6 -27.4 -17.8 37 0.35
Li MWCL 22 5.7 16.8 17 58 7 -26 -21 31 0.6
Kong MWCL16 6 31.4 4.1 64 4.7 -32.4 -11.1 53.7 0.59

Reference

Cui IMS 22
Shin RFIC 18
This work @1.3V
This work @1.0V
This work @0.8V
Kong MWCL16
TMTT 20
Li MWCL 22

0.1 to 0.3 dBm
OP1dB @ 13.3mW

16
Conclusions

• Bias point optimization is a powerful tool for block level power optimization
• Current density scaling strongly influences small signal parameters, with moderate linearity impact (for high Z)
• Voltage scaling weakly influences small signal parameters, but strongly impacts linearity
• Many modern CMOS technologies can support complimentary current reuse in mmW
• Presented a state of the art LNA with highest linear and nonlinear FOM in the literature
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