Tu3B-1

A 450W GaN-Based Limiter for S-Band Application

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Outline

- Introduction
- UMS GH15 technology
- Design consideration
- Measurement results
- State of the art
- Conclusion
- Acknowledgment

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Introduction

- New receivers require SWaP (Size Weight and Power) components in order to become more and more integrated
  - RF Power Limiters are key components for receiver, they must ensure :
    - High power handling
    - Low insertion losses
    - Low flat Power Leakage
    - Integrability
- Usually Limiter are made of Silicon or GaAs PIN Diodes

➔ Alternative proposed here is to use GaN technology to realize integrated high power limiter

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UMS GH15-1x technology

- **Applications up to Ka Band (35 GHz)**
- **Technology Features**
  - 4 Inch AlGaN/GaN on 70µm SiC substrate
  - Thin an thick metal Layers
  - Air bridges
  - Vias interconnects
  - Mechanical BCB protection
- **Components**
  - GaN HEMT with Lg = 150 nm
    - Source terminated field plate topology
    - Switch type devices
    - 20 years life time @ Tj ROR = 200°C
  - Diodes
  - Inductors
  - 175 pF/mm² MIM capacitors (DLD)
  - 350 pF/mm²MIM Capacitors (DHD)
  - TaN / TiWSi thin film resistors

UMS GH15-1x technology

- **Technology Features (What's News)**
  - Over Via capacitor (DLD and DHD)
  - Moisture Protection
  - Optimized transistor layout for low-noise applications
  - Extended frequency capabitlity

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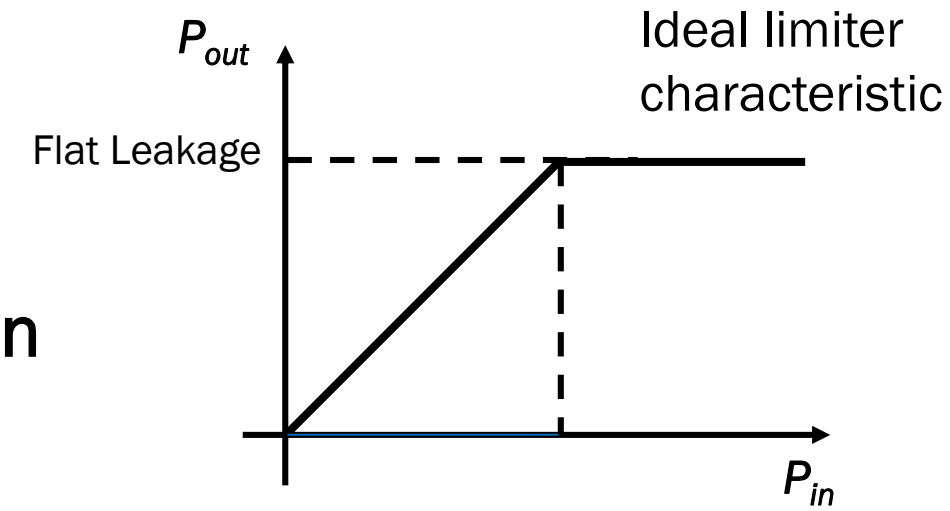
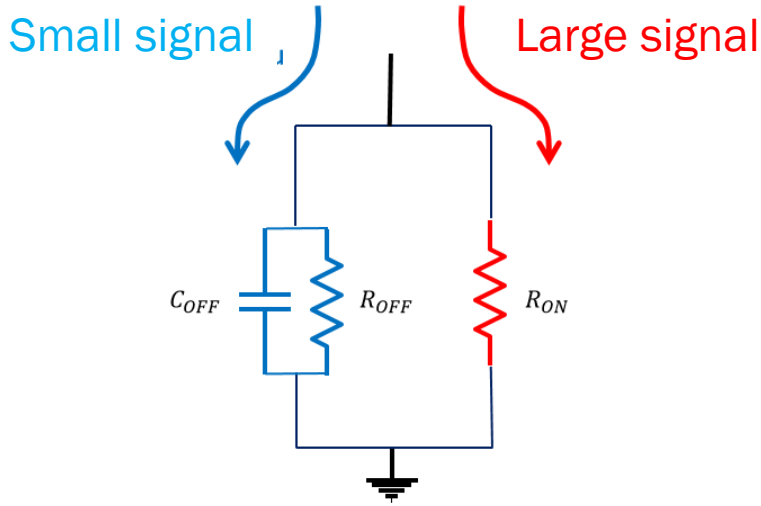
Design consideration

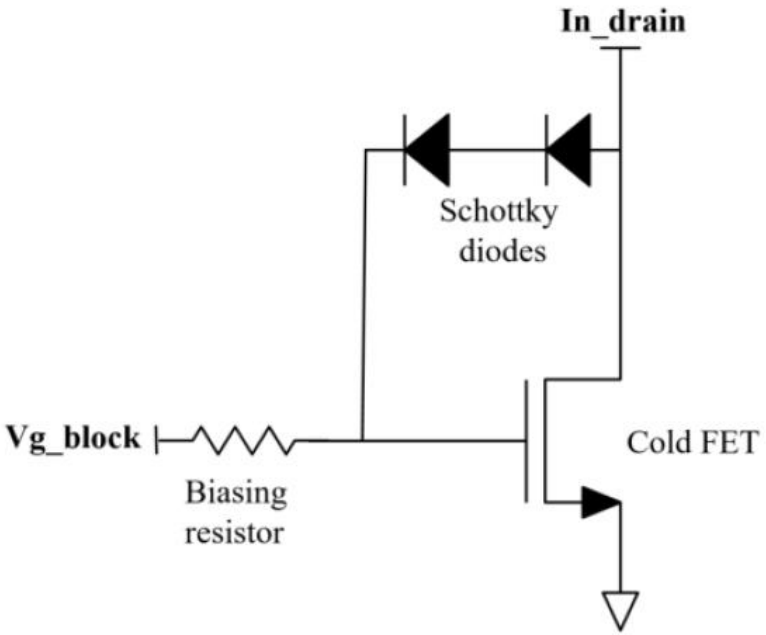
- RF Power Limiter key parameters
  - Bandwith ➔ Low Coff
  - Insertion losses ➔ High Roff / Low Coff
  - Power handling / Flat leakage ➔Low Ron
  - Maximum peak current

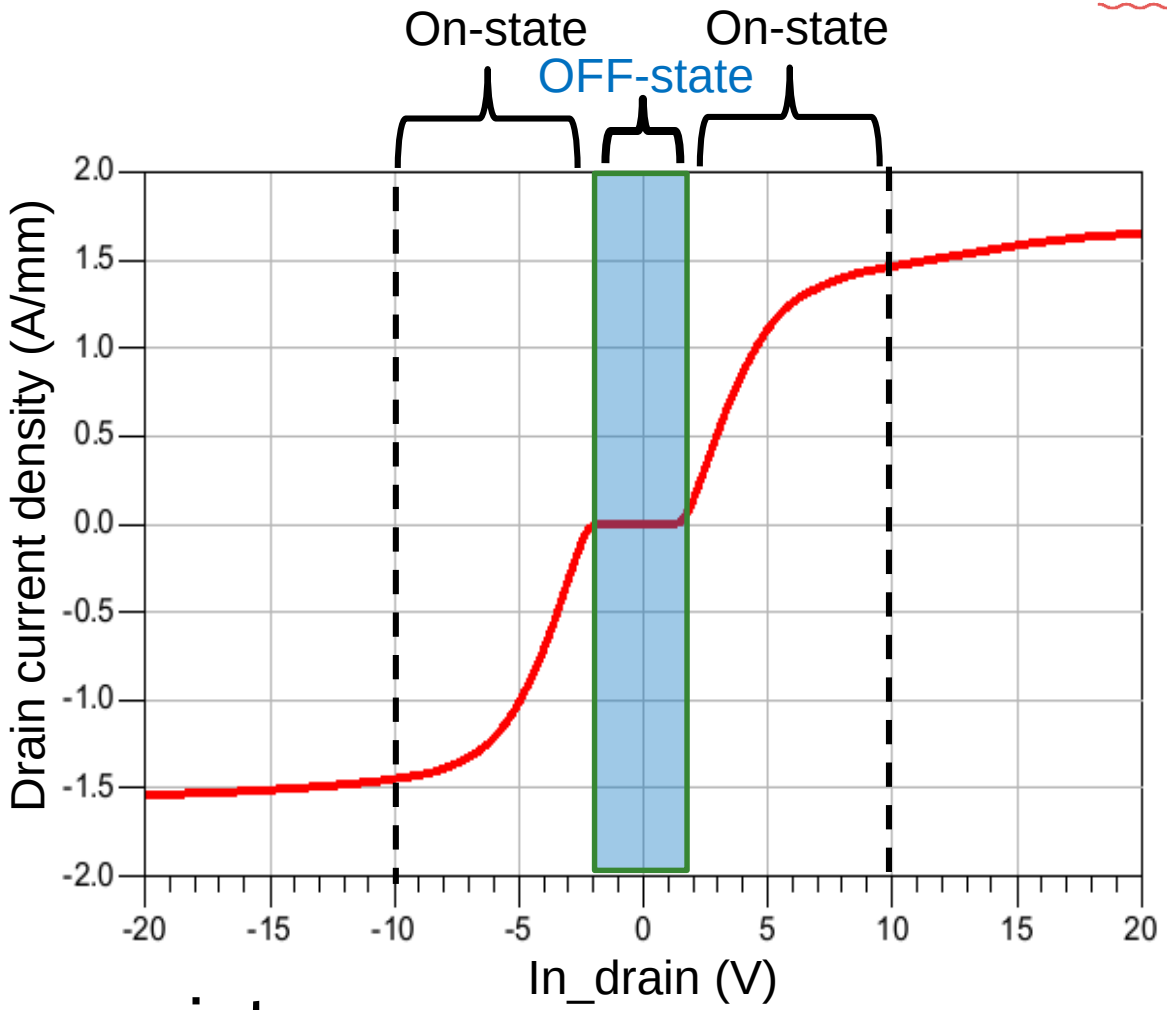




Design consideration

- GaN Limiter power cell

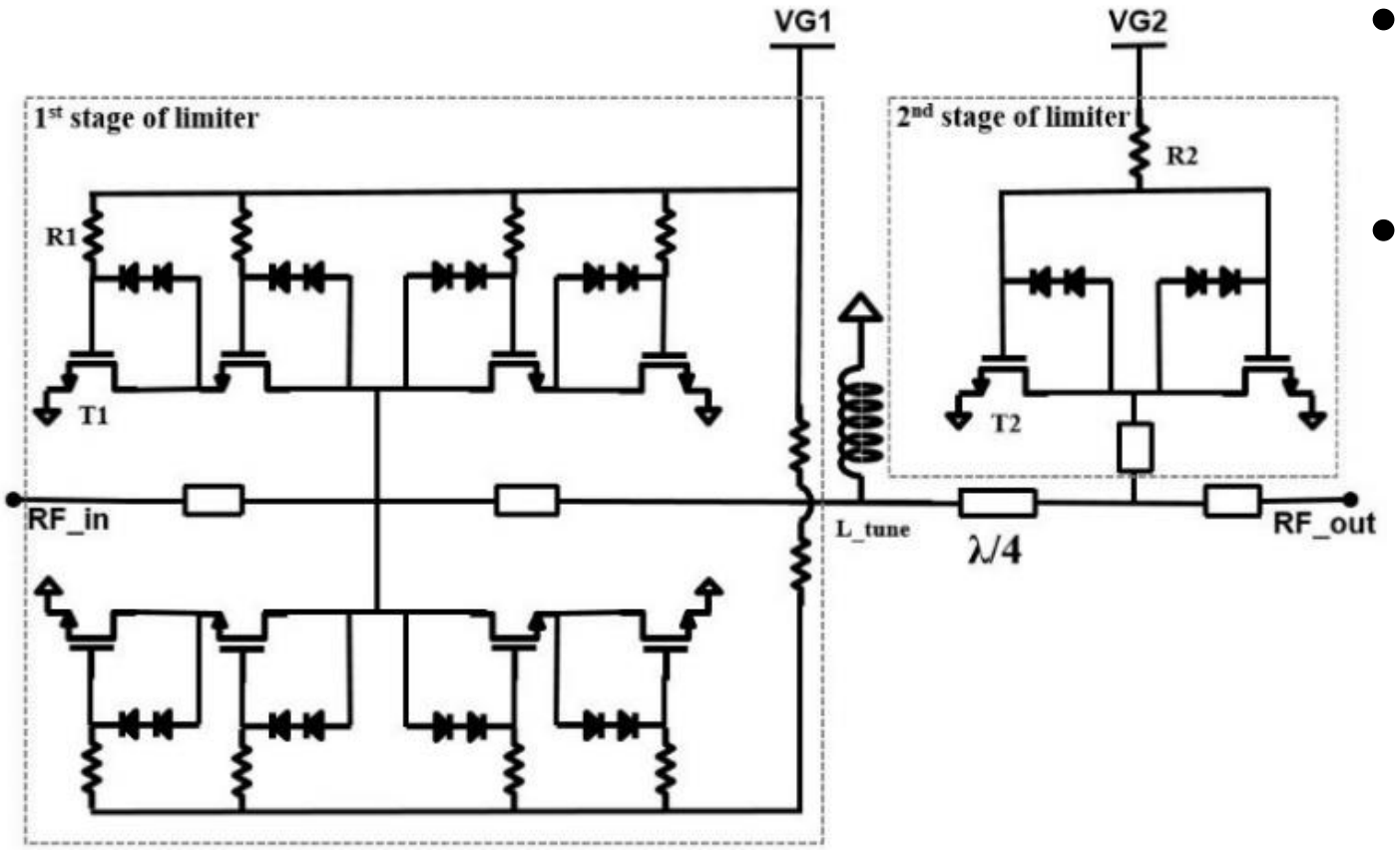




➔ Diodes are used to reduce Ron resistance

➔ Limiter triggering level is set by Gate voltage (Vg_block)

Design consideration

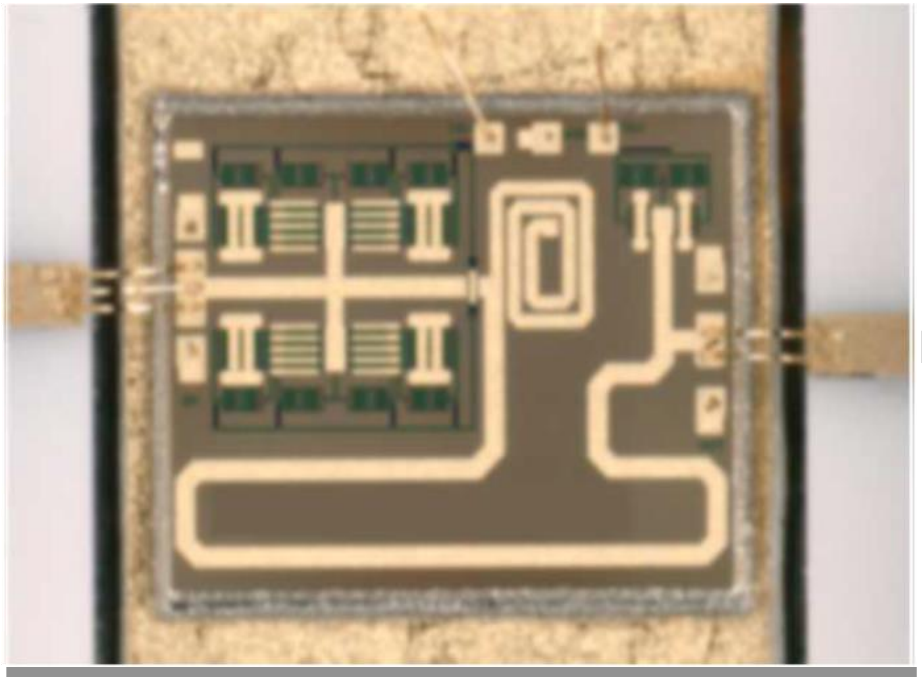


$$I_{peak} = 2\sqrt{\frac{2\,P_{RF\_in}}{R_0}} \sim 6A$$

- 2 Stage / quarter-wave structure
- 1st stage sizing
  - Sustain 250W (~6A)
    - Limited 1.4 A/mm saturation current per transistor
  - L_tune is used to accord Coff
  - Quarter-wave length to maximize second stage performances (isolation and flat leakage)
- 2nd stage sized to minimize flat power leakage

Design consideration

- Manufactured MMIC
  - Die size : 2,5 mm x 2 mm



- 1st stage sizing
  - W = 2x4x8x150 um
- 2nd stage
  - W = 2x6x40 um
- Diodes
  - Sized to handle until 8mA of RMS current during hard limitation of the limiter

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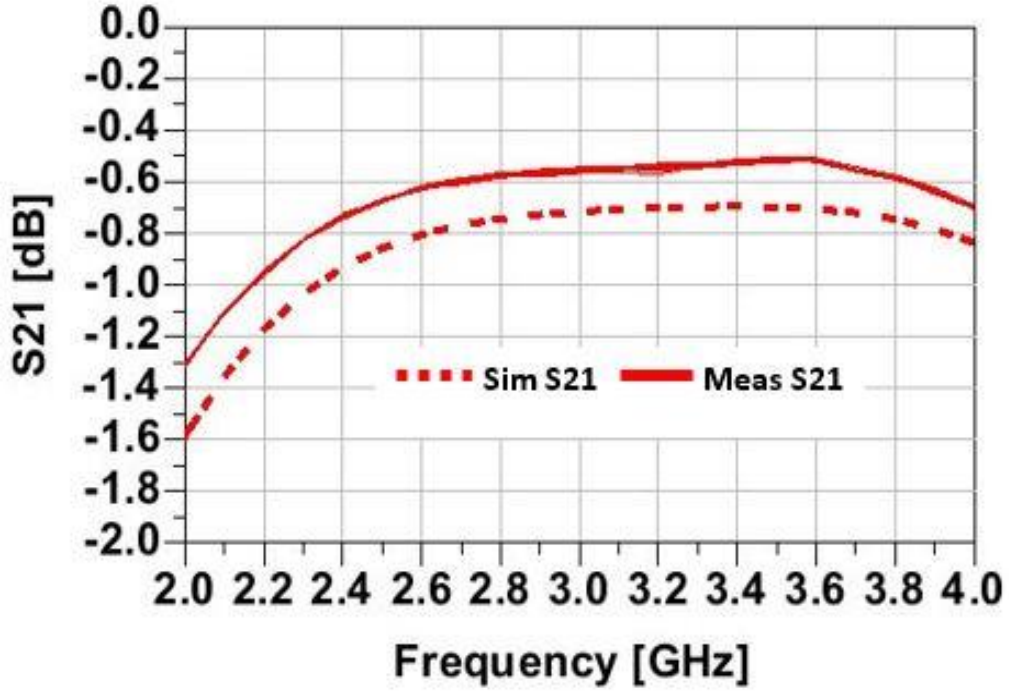
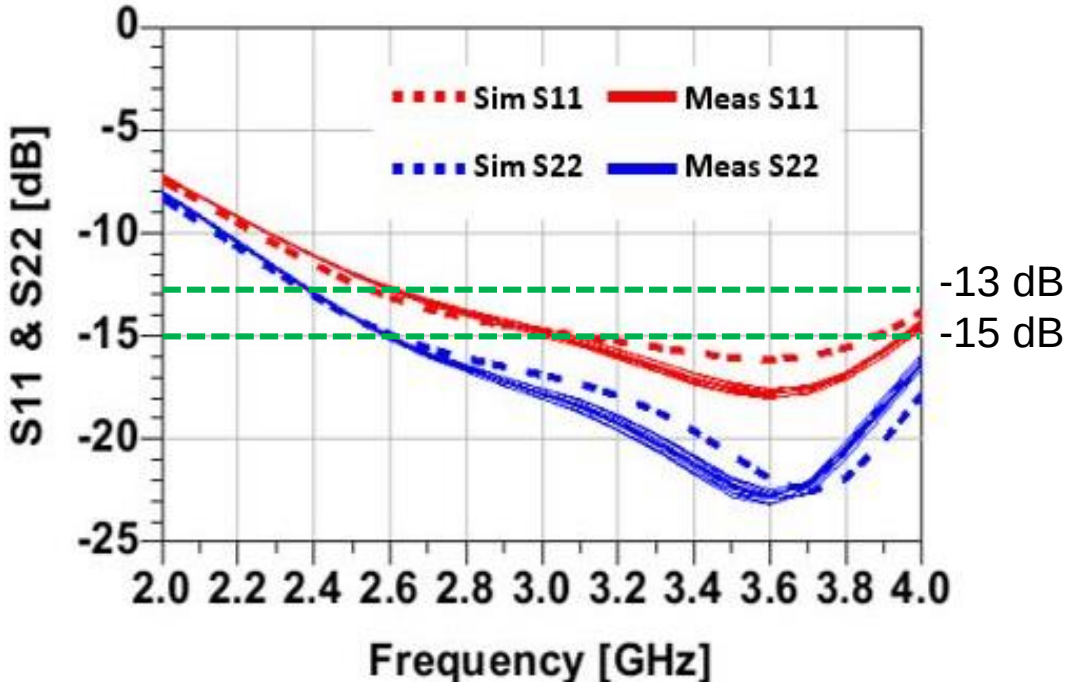
Measurement results

- On wafer measurements / Small signal (10 dies)

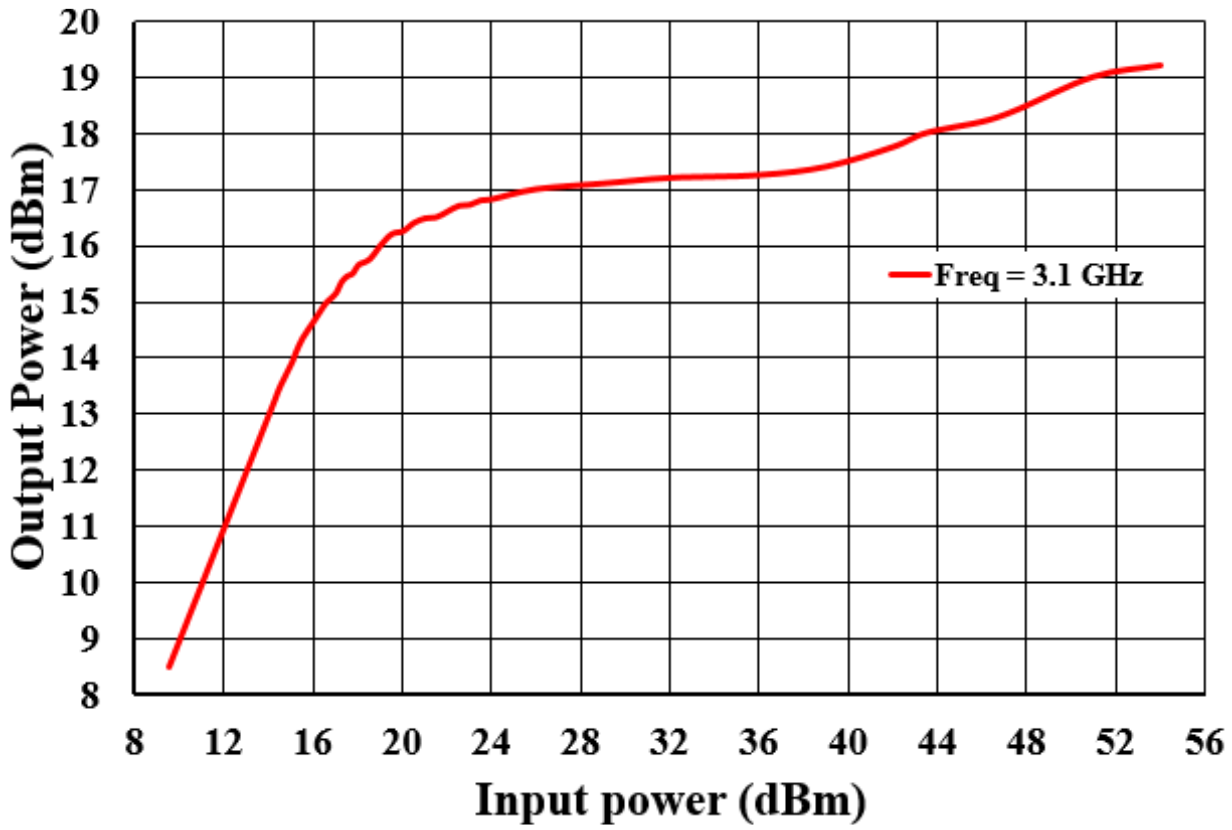




- Insertion Losses < 0.6 dB on [2.6 – 3.8] GHz
- Input reflexion coefficient < -13 dB
- Output reflexion coefficient < -15 dB

Measurement results

- Text fixture / High power measurements

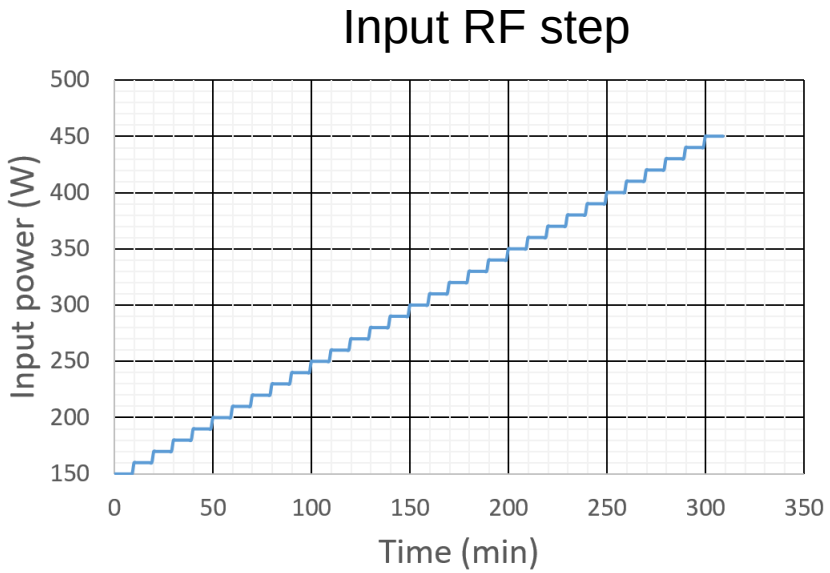


- Test conditions
  - Temp = 25°C
  - Pulsed input power
    - Duty cycle 15%
    - <10ms

- Flat power leakage < 20 dBm
- Triggering level : P_{in1dB} = 16 dBm

Measurement results

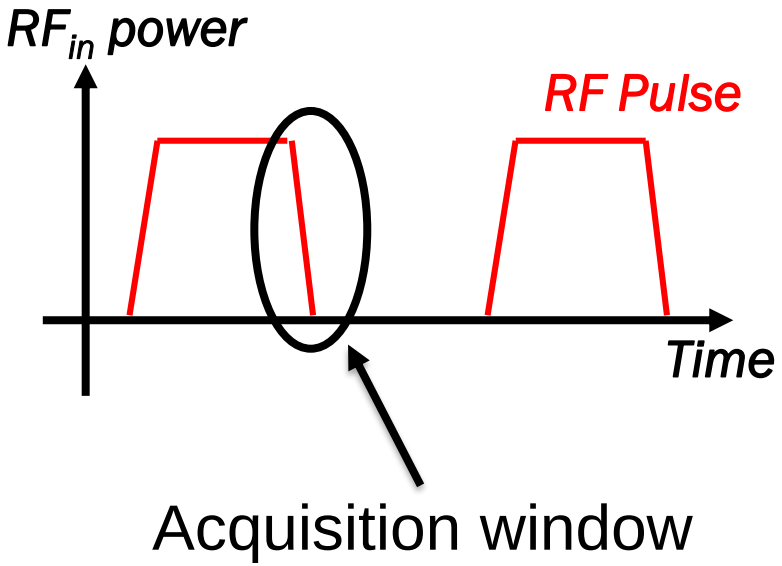
- RF step stress test
- Test conditions (4 Devices)
  - Tcase =75°C
  - Freq = 3.1 GHz
  - Pulsed input power
    - Duty cycle 15%
    - <10ms
    - From 150W to 450W by 10W step
    - 10 min between each step

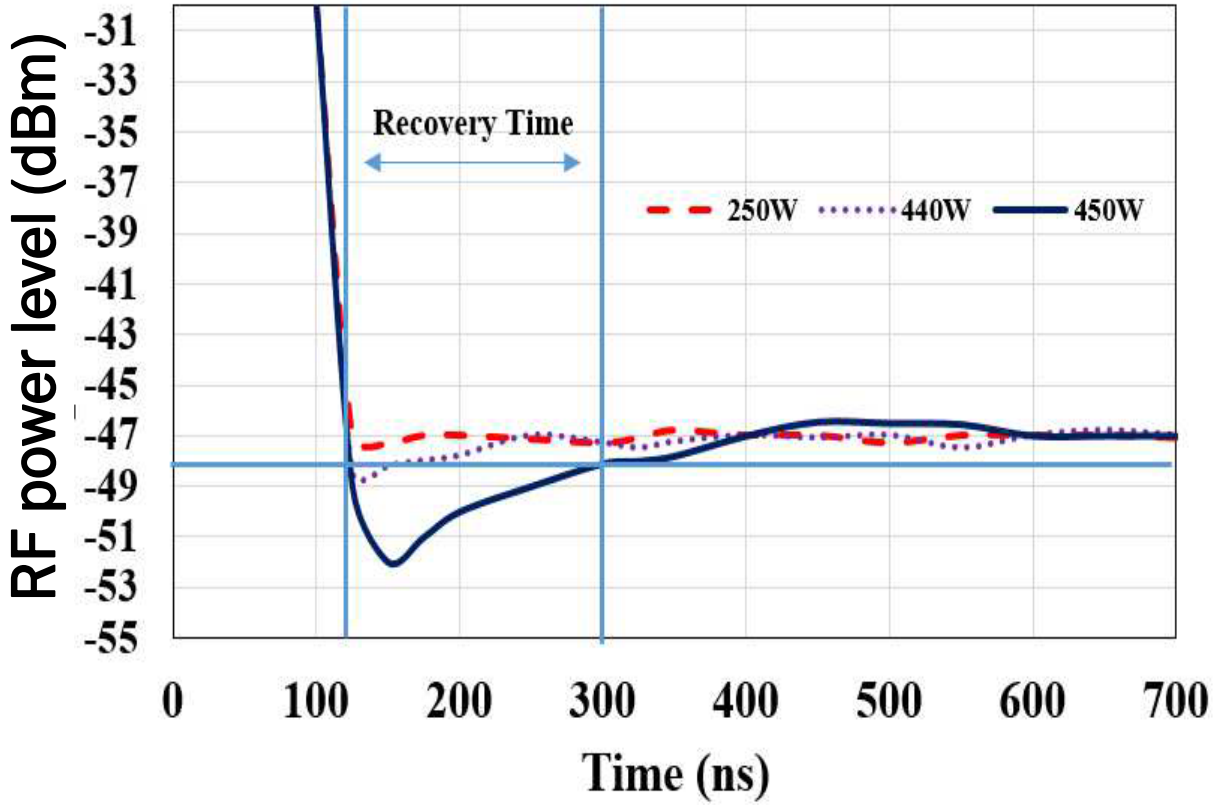


- No performance or structural degradation observed. Small signal measurement performed to confirm.
- Power Handling of 450W (pulsed) achieved

Measurement results

- Amplitude recovery time measurement

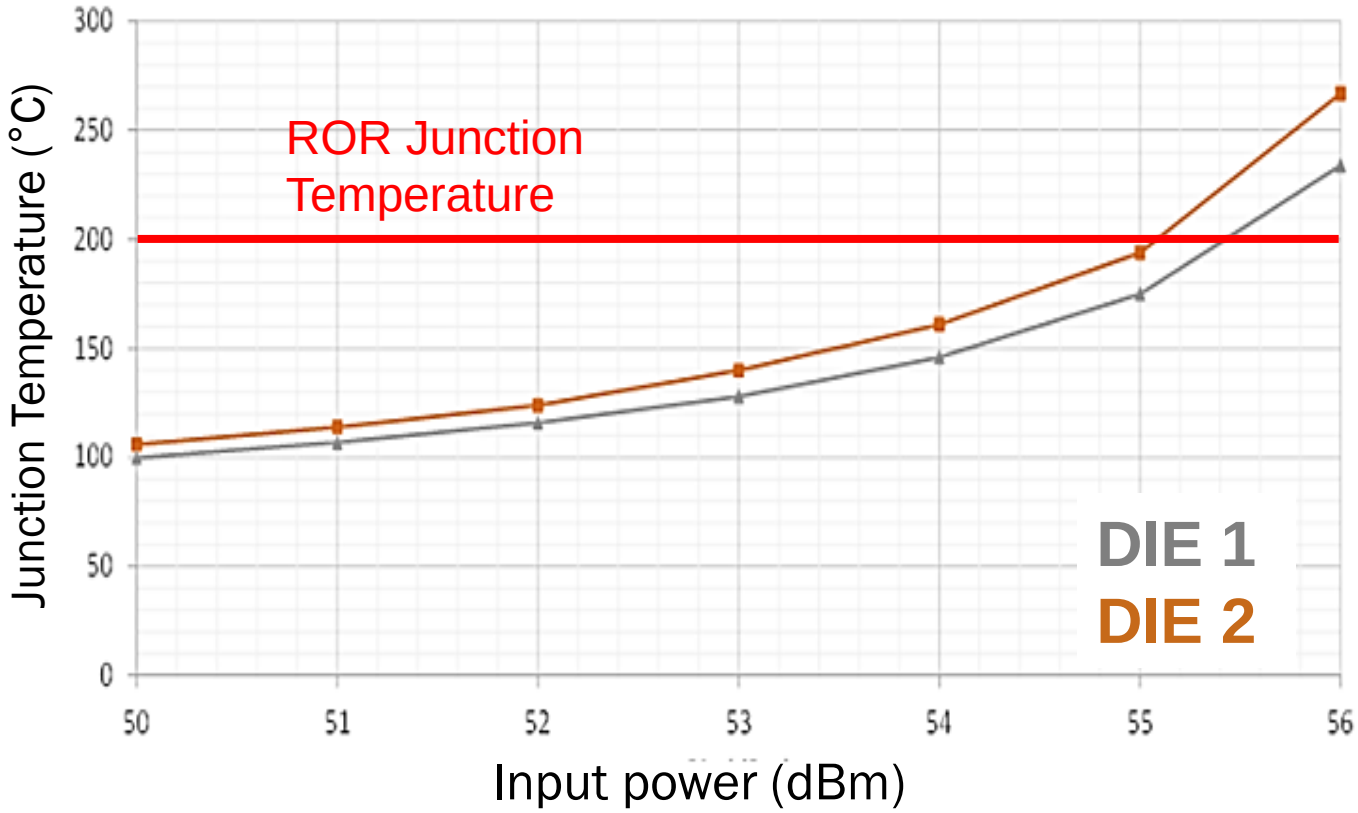




- Low amplitude recovery time < 200 ns @450W pulsed

Measurement results

- First stage limiter temperature measurement



- Test conditions
  - Temp = 75°C
  - Pulsed input power
    - Duty cycle 15%
    - <10ms

- ROR junction temperature is reached after 55 dBm of pulsed input power

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State of the art

Ref.	Technology	Freq (GHz)	Limiting cell	Pmax (W)	Insertion Loss (dB)	Leakage (dBm)
[3]	GaAs	2-5	VPIN diodes	100 (CW)	0.5	16
[4]	BiCMOS	3	PIN diodes	63 (P)	0.5	20
[5]	GaAs	3-28	VPIN diodes	4 (CW)	0.39	17
[6]	GaN	1-6	FET	50 (CW)	0.6	22
This work	**GaN**	**2.6-3.6**	**Cold FET + Schottky diodes**	**450 (P)**	**0.5**	**<20**

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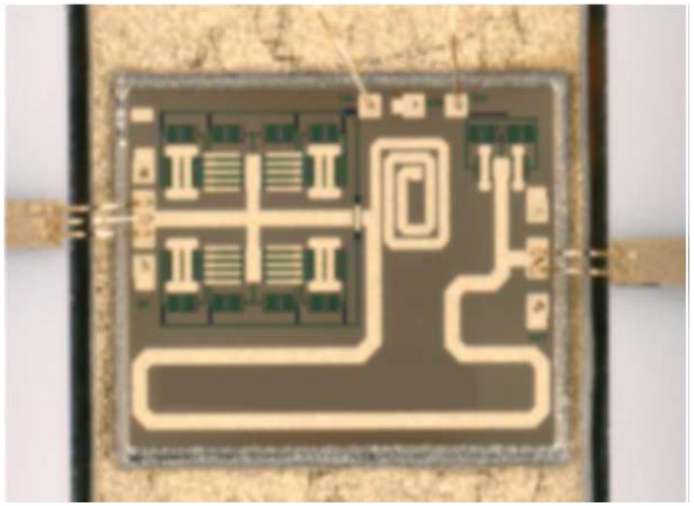
Conclusion

- Robust High power 2 stages GaN limiter
  - Low insertion losses < 0.6 dB
  - State of the art power handling
    - >450 W pulsed input power
    - Tj < 200 °C @ 55 dBm
  - Low Recovery time limiter
    - <200 ns at 450Wc



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