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A 26-32GHz Differential Attenuator with 0.23dB RMS Attenuation Error and 11.2dBm IP1dB in 40nm CMOS Process

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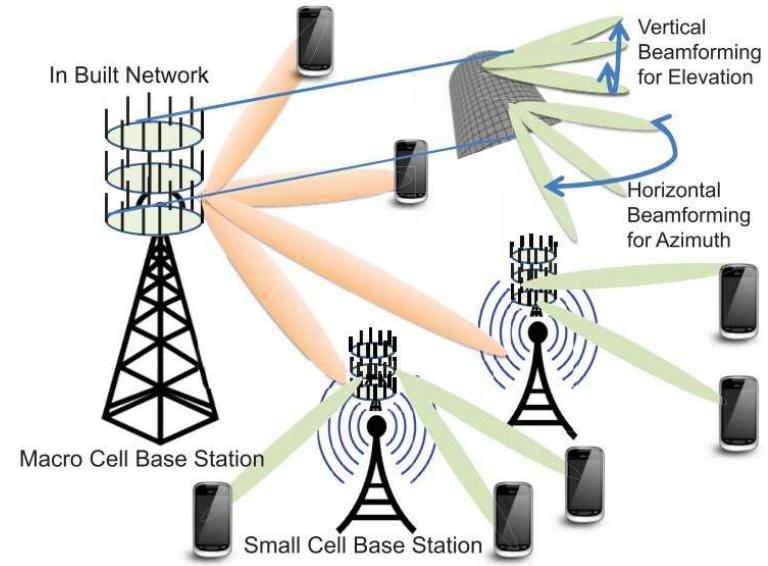
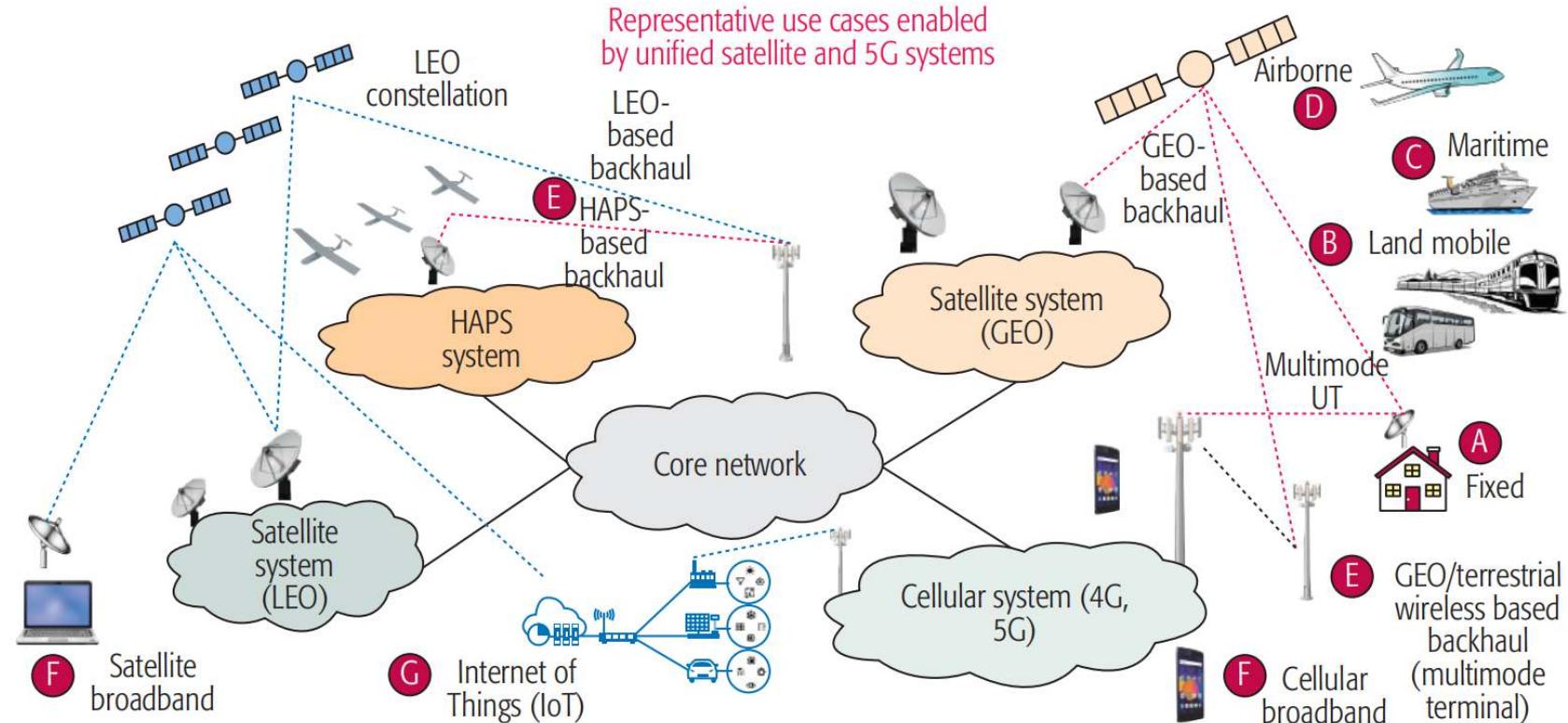
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- Introduction
- Circuit Design
 - Architecture Overview
 - Phase variation suppression
 - (1) Capacitive Compensation (C_p)
 - (2) Further Optimization of Phase Error (K_p)
 - Cascading Order for Linearity Improvement
- Measurement Results
- Performance Comparison
- Conclusion

Application Background

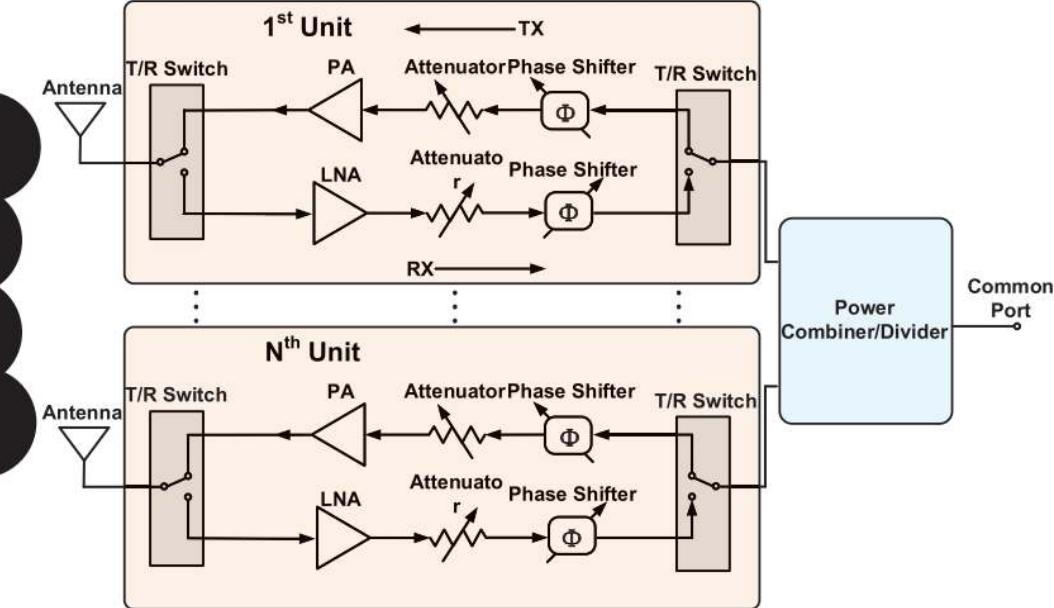
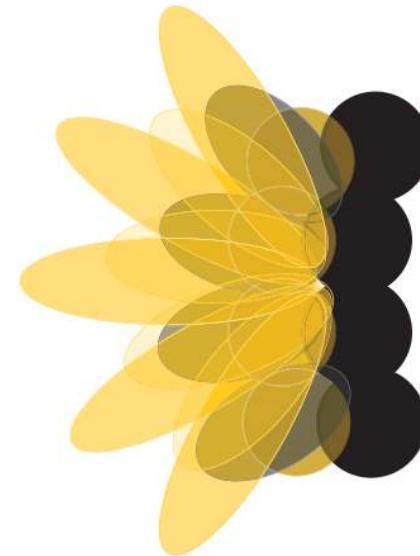


- [1] IEEE COMMUNICATIONS SURVEYS & TUTORIALS, M. Agiwal, 2016
- [2] IEEE Network, R. Gopal, 2018

- K/Ka/Ku band Phased Array in 5G Satellite Communication

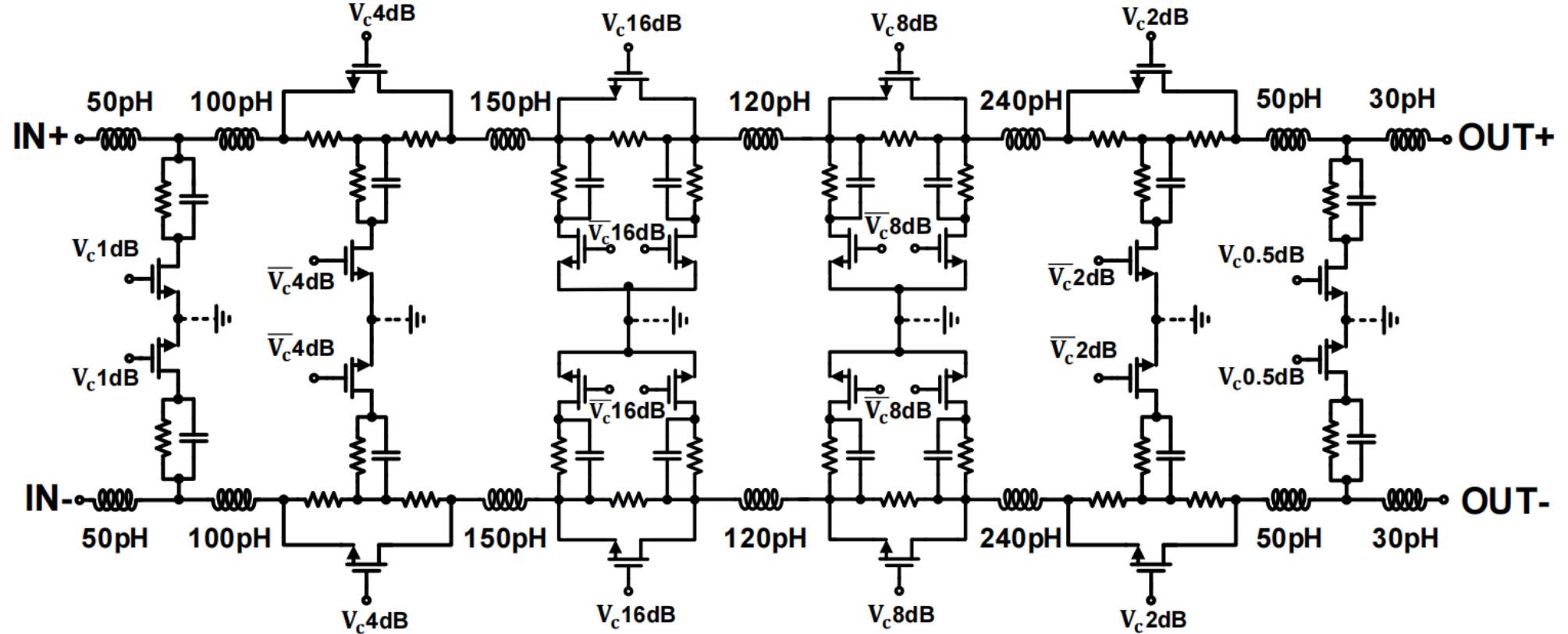
Application Background

- Attenuator
 - Phased Array Transceiver
 - Amplitude control
- Challenge of Attenuator
 - High Attenuation Accuracy
 - Low Phase Error
 - High Linearity



[4] TCAS-I, C. Zhao, 2020

Architecture Overview



- 6bit differential structure

- Capacitive Compensation technique

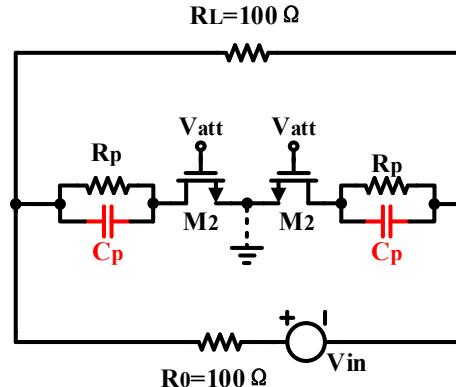
- Optimized cascading order for Linearity Improvement

Phase variation suppression

(1) Capacitive Compensation (C_p)

ST-type Attenuator:

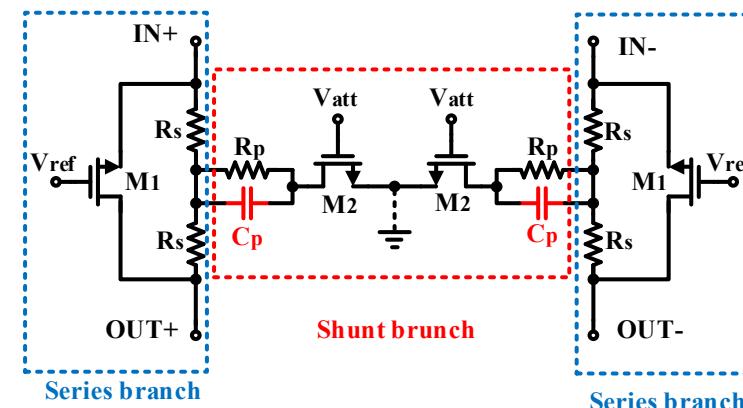
- Low insertion loss
- small attenuation(0.5/1dB)



Simplified T(ST)-type Attenuator with C_p

T-type Attenuator:

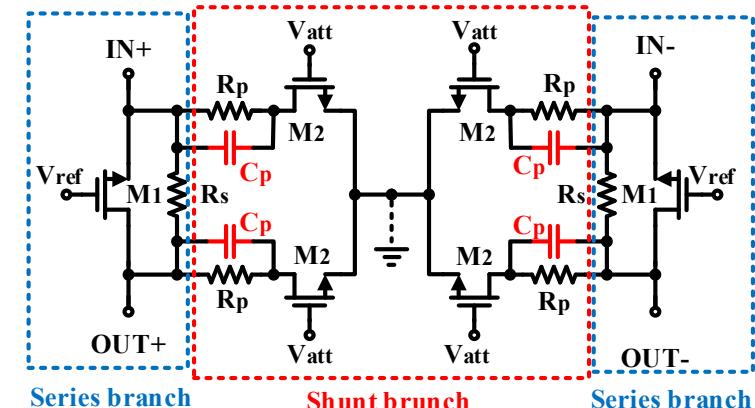
- Low insertion loss
- medium attenuation(2/4dB)



T-type Attenuator with C_p

Π -type Attenuator:

- large attenuation (8/16dB)



Π-type Attenuator with C_p

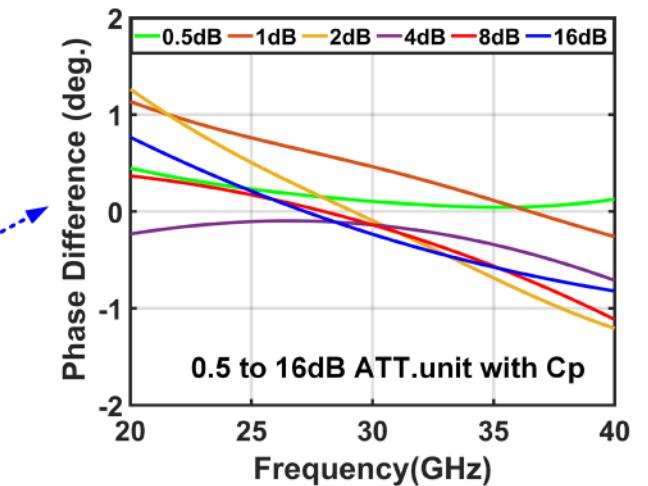
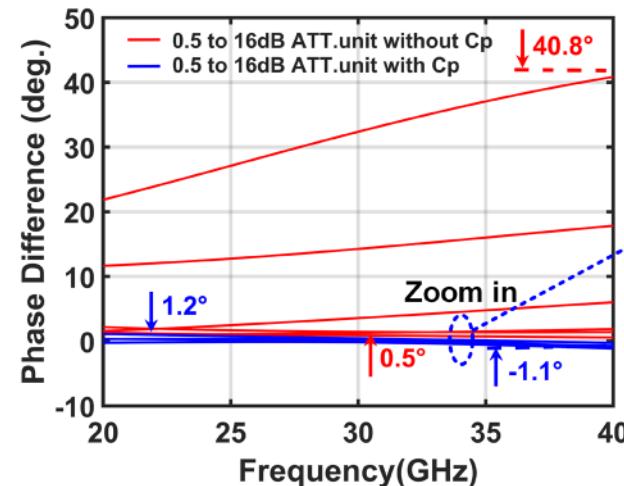
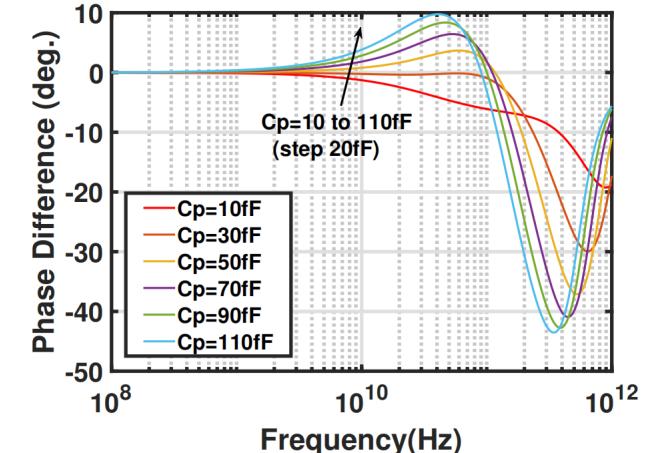
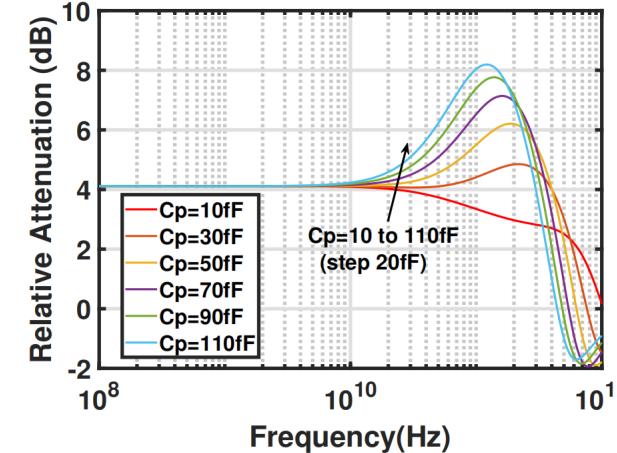
Phase variation suppression

(1) Capacitive Compensation (C_p)

Compensation Capacitor C_p :

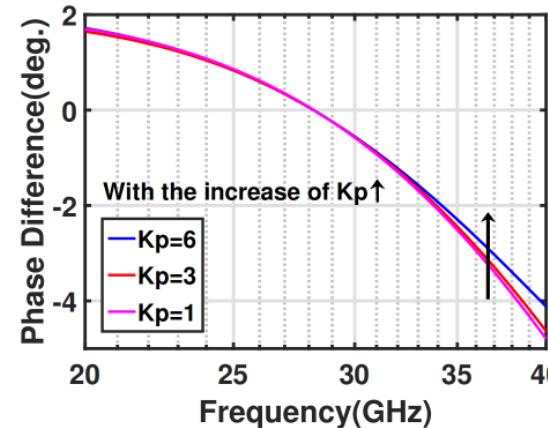
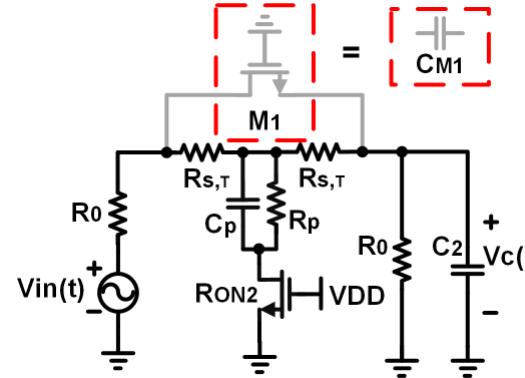
- Optimizing the value of C_p to obtain Low attenuation/phase error (T-type 4dB)

Capacitance compensation for each attenuator unit

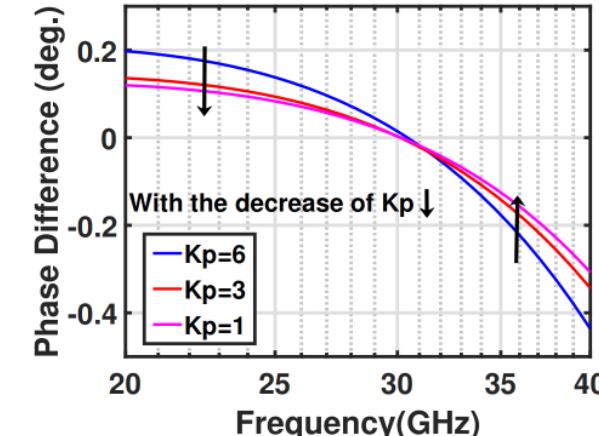
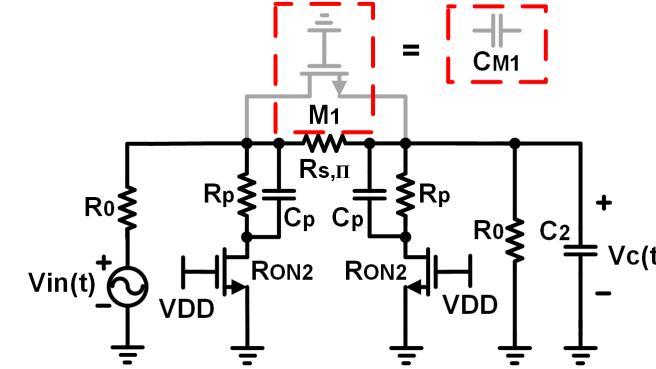


(2) Further Optimization of Phase Error (K_p)

Phase difference with different values of K_p



4dB T-type attenuator

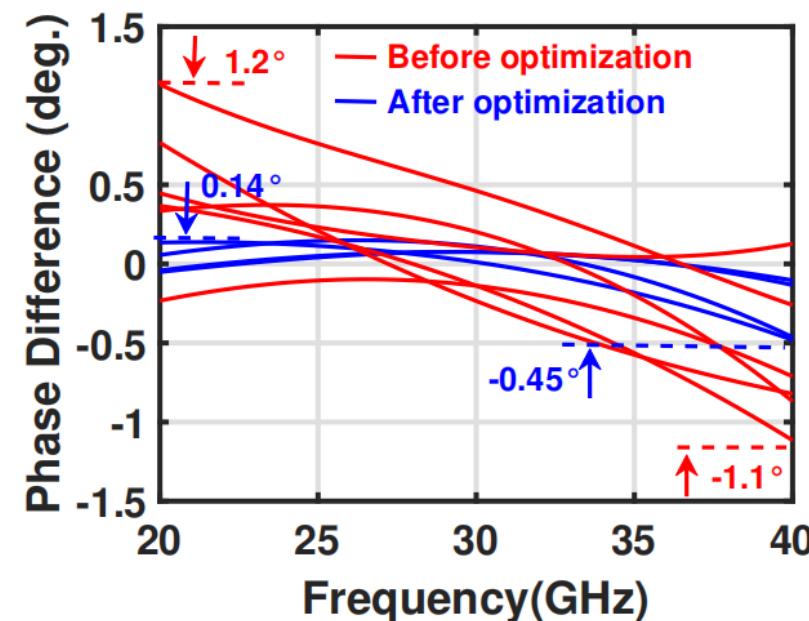


16dB Π -type attenuator unit

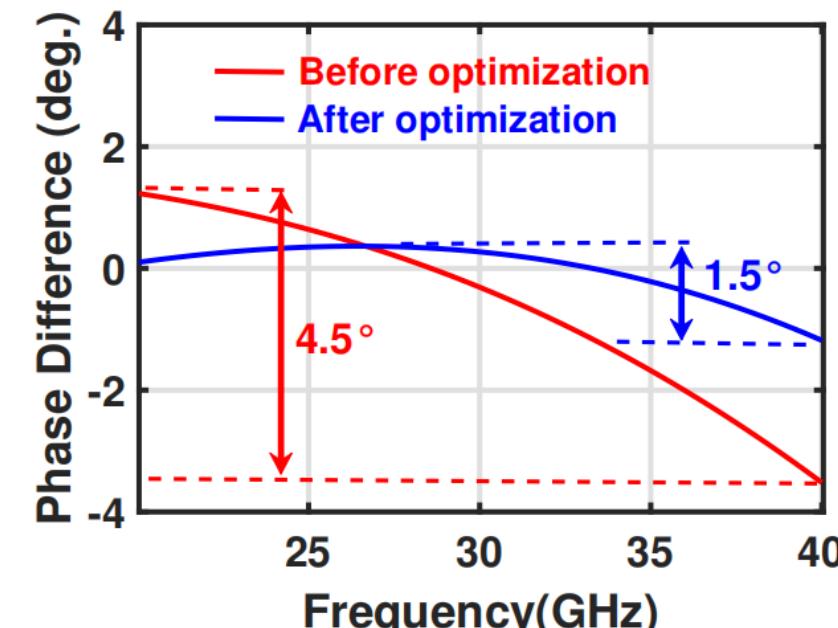
Define: $K_p = R_p / R_{ON2}$

(2) Further Optimization of Phase Error (K_p)

- (a) Simulated phase difference of attenuator units (0.5 to 16dB) before and after optimization (inductors and routings extracted by EM simulation tool)
- (b) Simulated phase difference of the overall attenuator before and after optimization



(a)

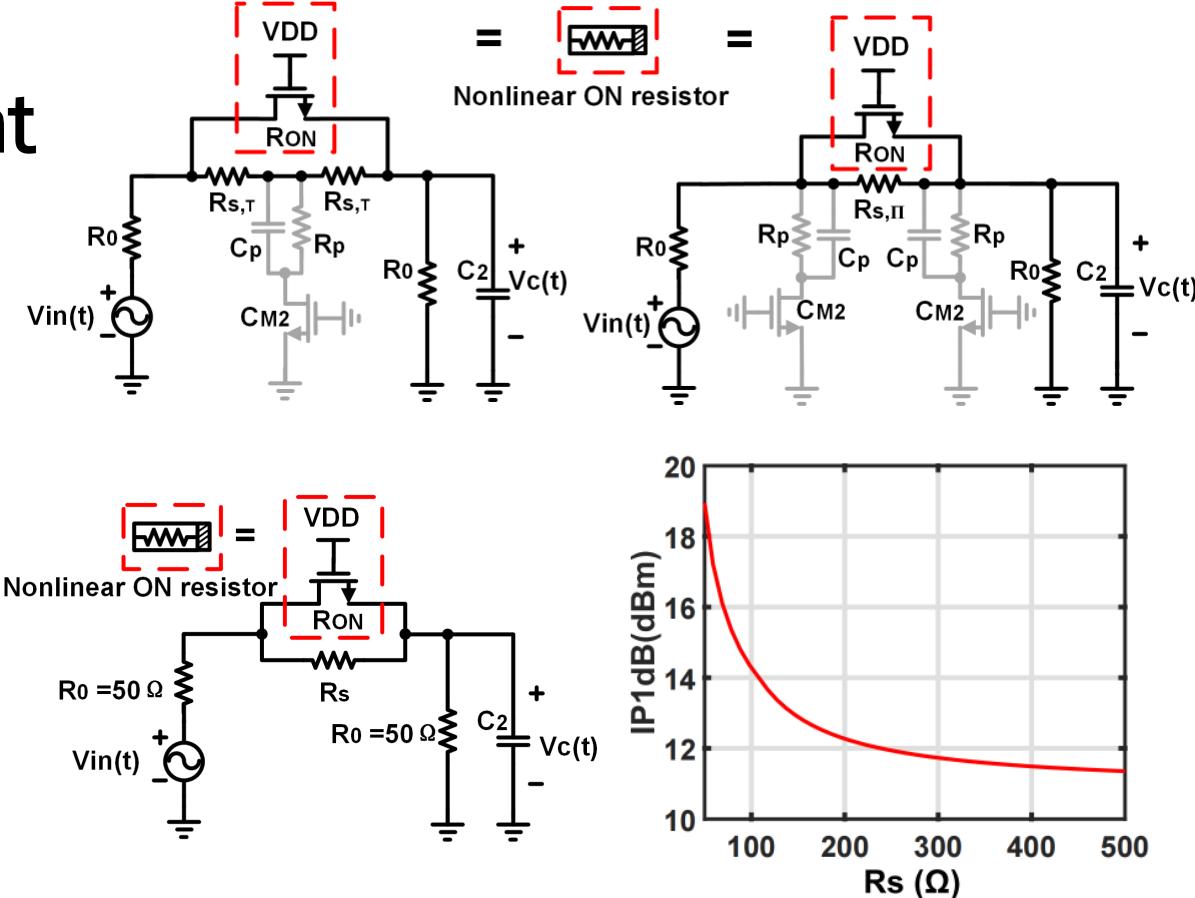


(b)

Cascading Order for Linearity Improvement

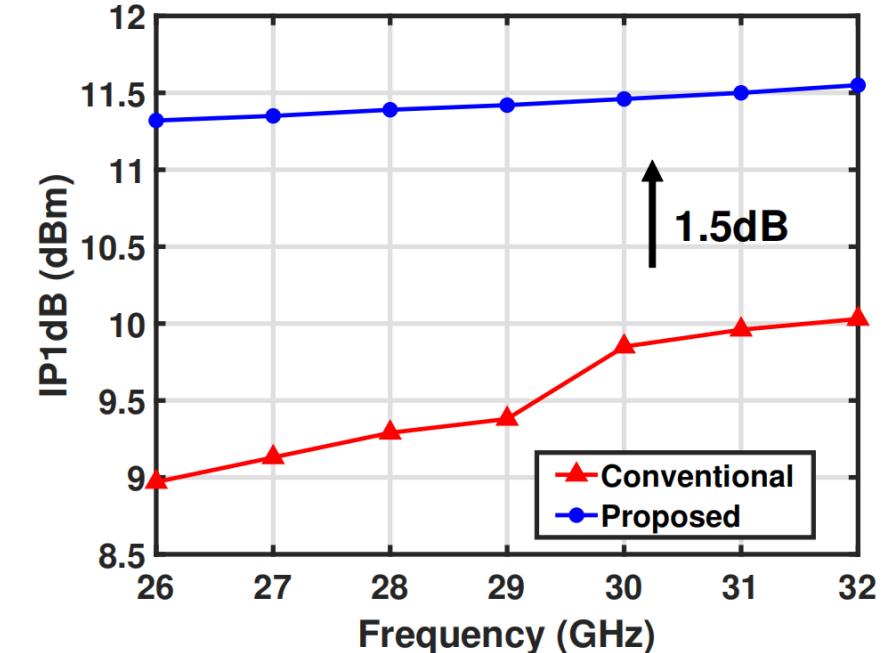
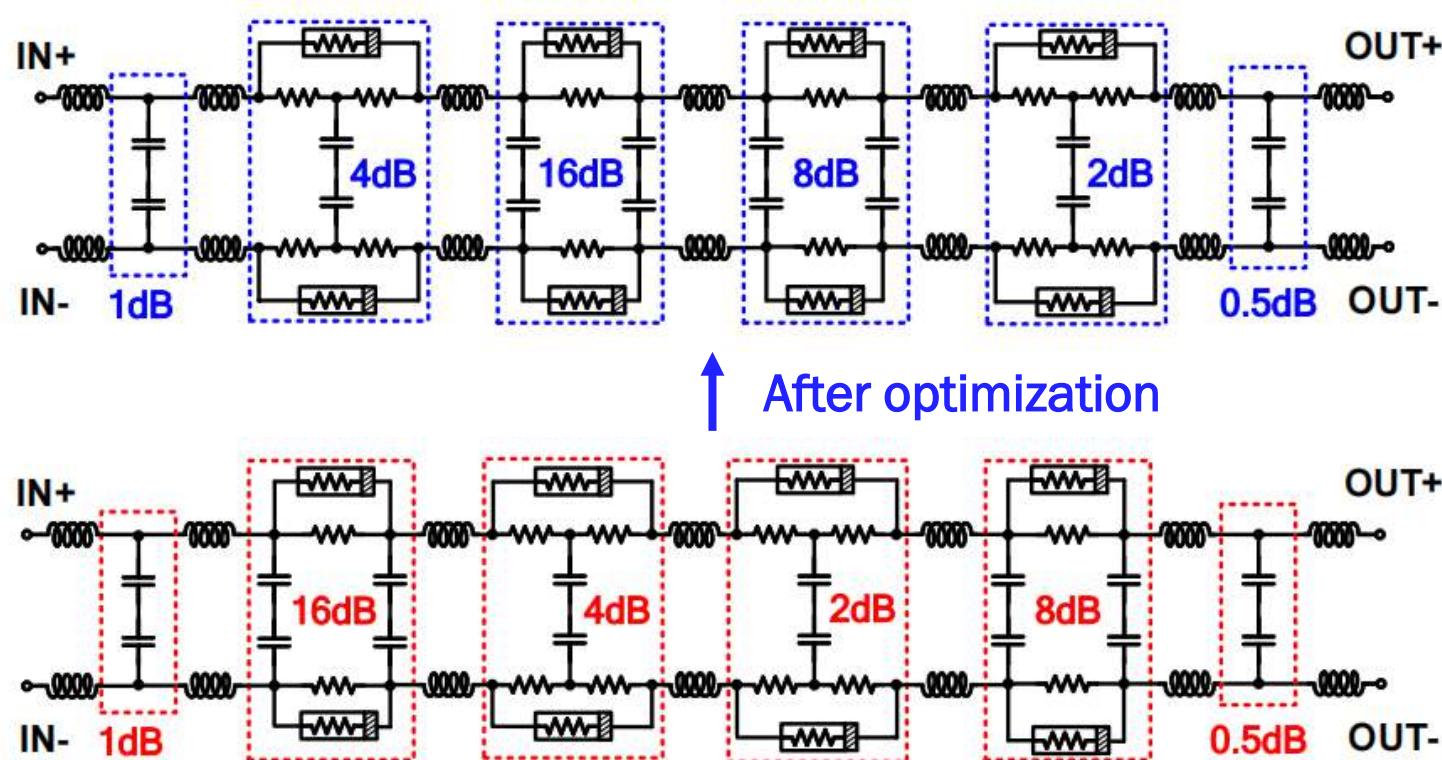
Distortion analysis of T/ Π -type Attenuator in reference state

- Series transistor can be equivalent to a nonlinear resistor
- The larger the attenuation, the larger the R_s ($R_{s,T}$ or $R_{s,\Pi}$), and the lower the IP_{1dB}



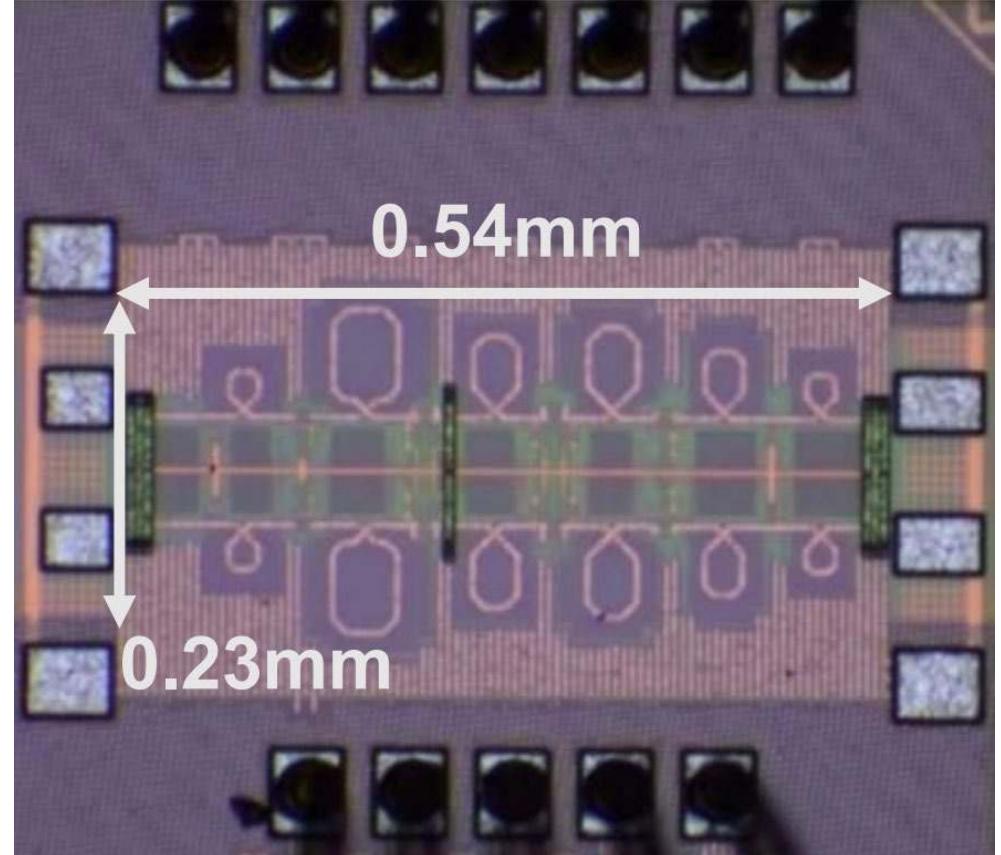
Cascading Order for Linearity Improvement

- 1.5dB IP1dB improvement by optimizing the order of attenuation units



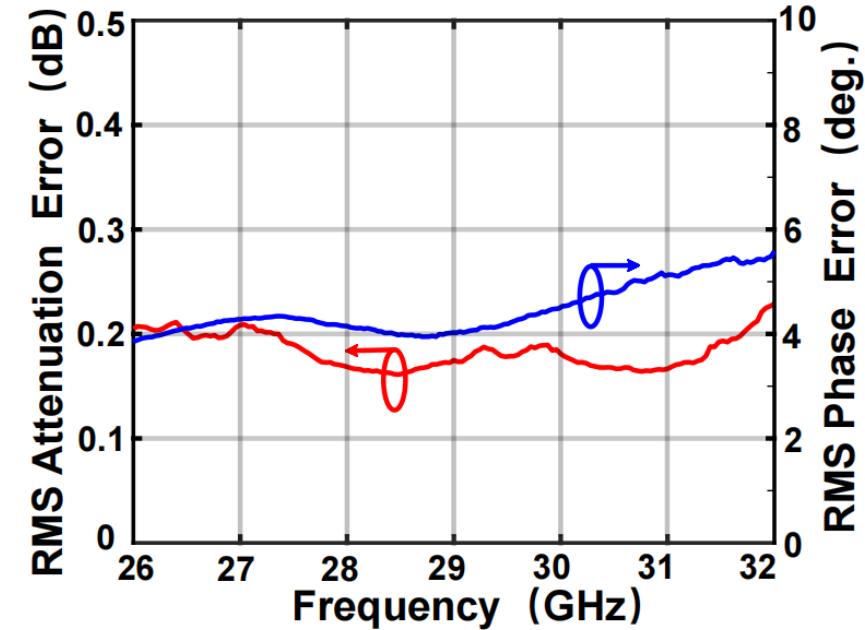
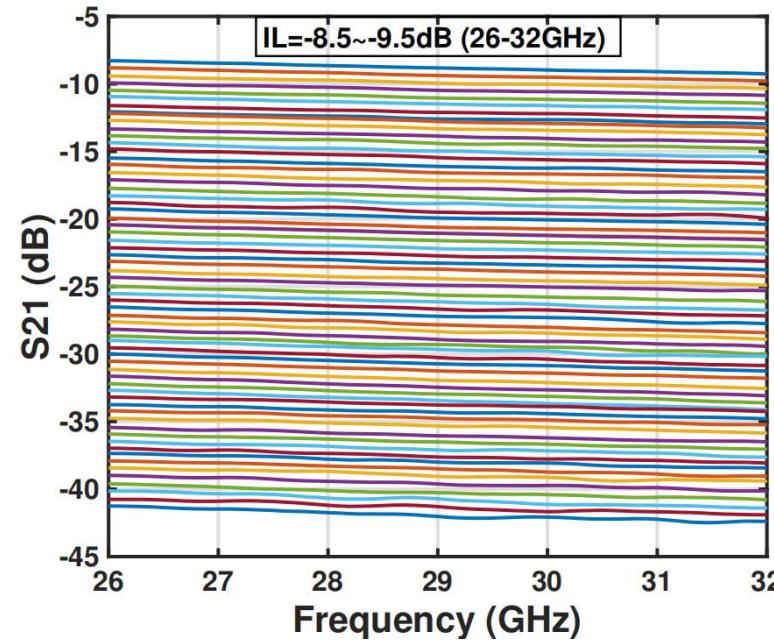
Chip Photo

- 40nm CMOS
- $0.54 \times 0.23 \text{ mm}^2$ (core)
- On wafer test using a probe station



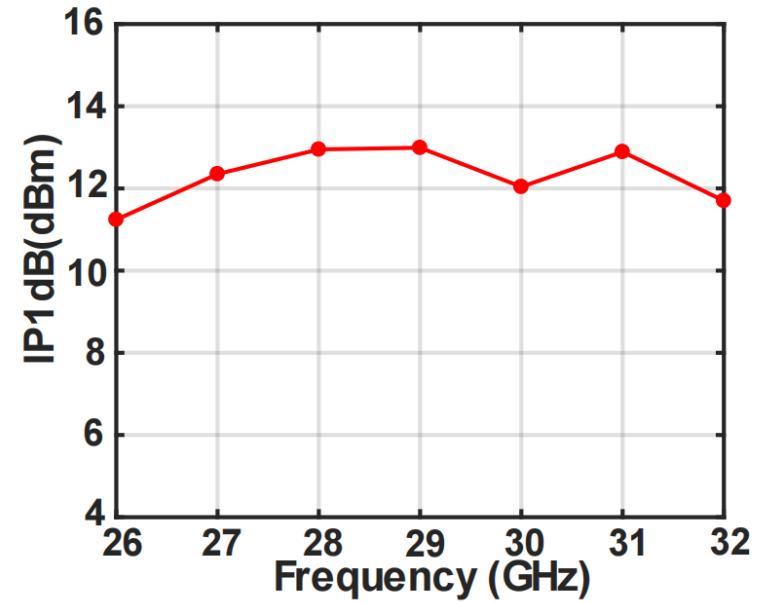
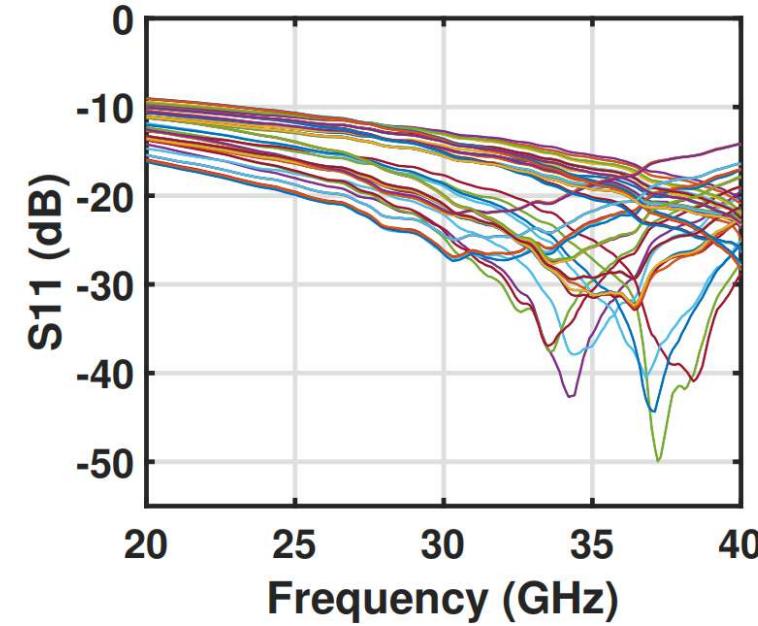
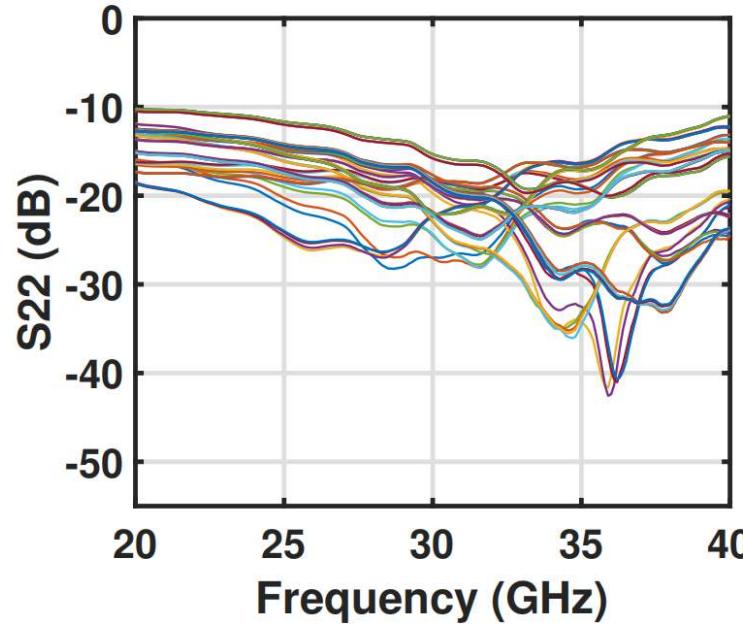
Measurement Results

- Insertion Loss: -8.5dB ~ -9.5dB
- RMS attenuation error <0.23dB RMS phase error <5.6°



Measurement Results

- Input/Output Return Loss: <-10dB
- IP1dB : >11.2dBm



Performance Comparison

	JSSC'18 [3]	TCAS-I'20 [4]	RFIC'17 [5]	IMS'20 [6]	This work
Process	0.13μm SiGe	65nm CMOS	65nm CMOS	55nm CMOS	40nm CMOS
Freq./GHz	DC-20	37-40	26-32	DC-32	26-32
Att.range/dB	31.5	31	31	32.4	31.5
LSB/dB	0.5	1	1	0.255	0.5
Insertion Loss/dB	1.7-7.2	7*	N/A	3.5-8.4	8.5-9.5
RMS ATT Error/dB	0.37	0.27	0.5	0.32	0.23
RMS Phase Error/deg.	4	3.7	5	5.33	5.58
Return Loss/dB	<-12	<-12	N/A	<-9.6	<-11.1
IP1dB/dBm	10	12*	N/A	9.1@30G	11.2-13
core area(mm ²)	0.14	0.21	N/A	0.054	0.124

Conclusion

- In this paper, a 26-32GHz 6-bit differential attenuator is proposed.
- The employment of the capacitive compensation and optimization of the shunt branches lead to low RMS phase errors among different attenuation states.
- Linearity improvement of the overall attenuator by optimizing the Cascading order of attenuator units

Acknowledge

This work was supported by the National Key Research and Development Program of China (No. 2020YFB1806300).

- Contact Information for the speaker is provided below for any follow-up questions:

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- [1] M. Agiwal, A. Roy and N. Saxena, "Next Generation 5G Wireless Networks: A Comprehensive Survey," in IEEE Communications Surveys & Tutorials, vol. 18, no. 3, pp. 1617-1655, thirdquarter 2016, doi: 10.1109/COMST.2016.2532458.
- [2] R. Gopal and N. BenAmmar, "Framework for Unifying 5G and Next Generation Satellite Communications," in IEEE Network, vol. 32, no. 5, pp. 16-24, September/October 2018, doi: 10.1109/MNET.2018.1800045.
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- [4] C. Zhao, X. Zeng, L. Zhang, H. Liu, Y. Yu, Y. Wu, and K. Kang, "A 37–40 GHz Low Phase Imbalance CMOS Attenuator with Tail-Capacitor Compensation Technique," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 10, pp. 3400–3409, 2020.
- [5] J. Han, J. Kim, J. Park, and J. Kim, "A Ka-band 4-CH Bi-directional CMOS T/R Chipset for 5G beamforming system," in 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2017, pp. 41–44.
- [6] Z. Zhang, N. Li, H. Gao, M. Li, S. Wang, Y.-C. Kuan, X. Yu, and Z. Xu, "A DC-32GHz 7-Bit Passive Attenuator with Capacitive Compensation Bandwidth Extension Technique in 55nm CMOS," in 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020, pp. 1303–1306.