Millimeter wave circuits for Phased Array communication systems in 28nm CMOS technology

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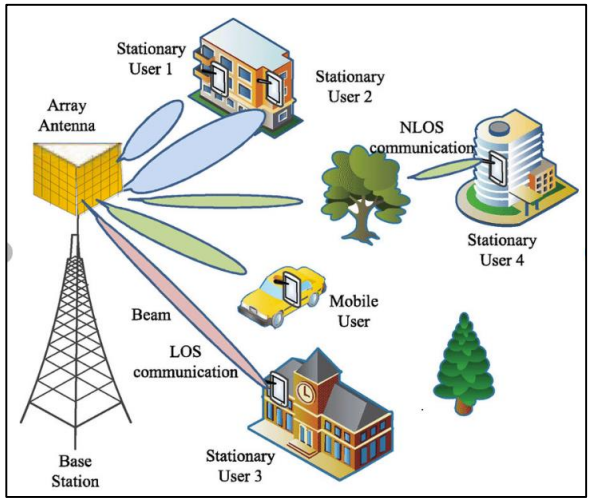
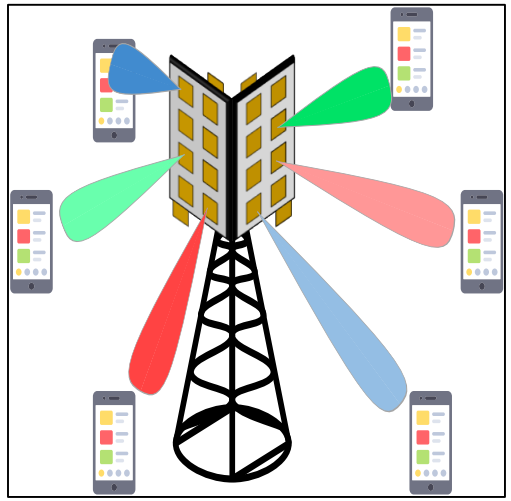
Outline

- Introduction
- Phased Array System
- Frequency Synthesizers for Phased Array System
- Up-Down conversion
- Conclusion

Digital transformation

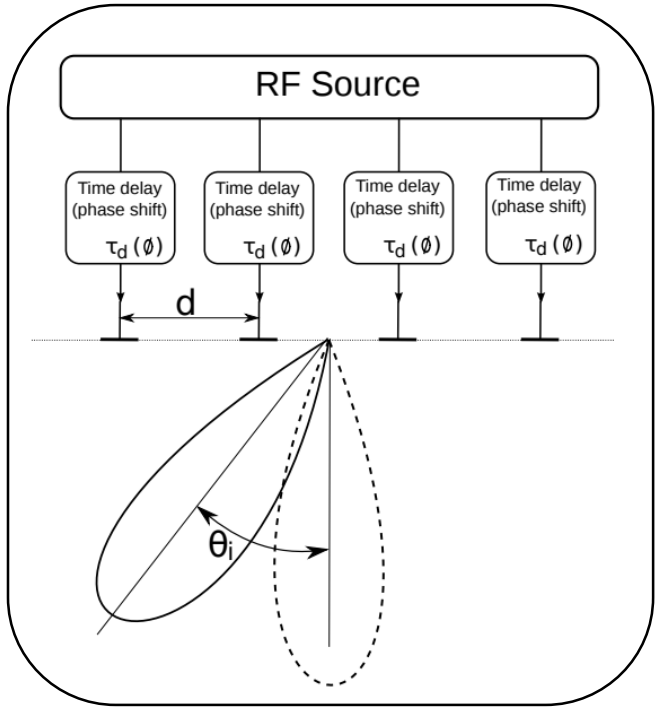
- Society and economy are seeing a strong transformation ➔ digital technology and digital business innovation
- All information are transformed into Digital Data and the number of communication links and data storage clouds are exploding
- Need of improved nano-scaled technologies, high data rate communication systems
- Phased array systems allow to increase efficiency of the communication network

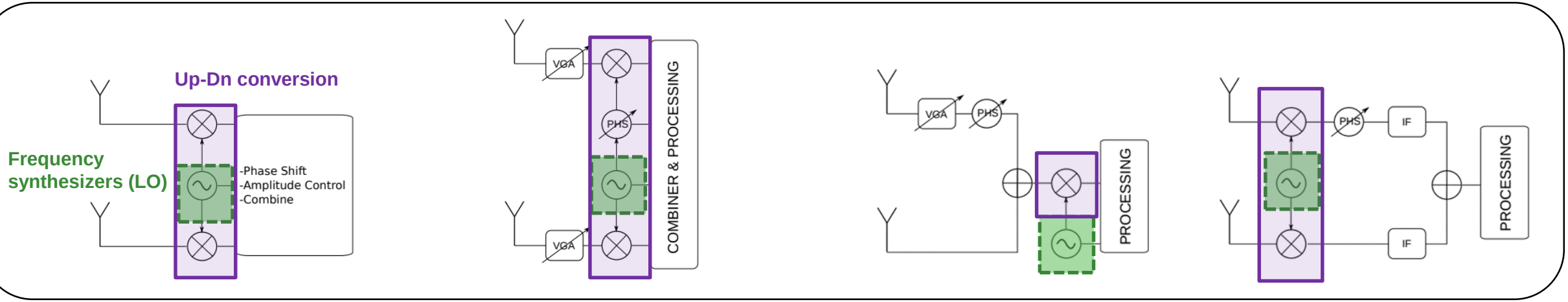




Phased Array System

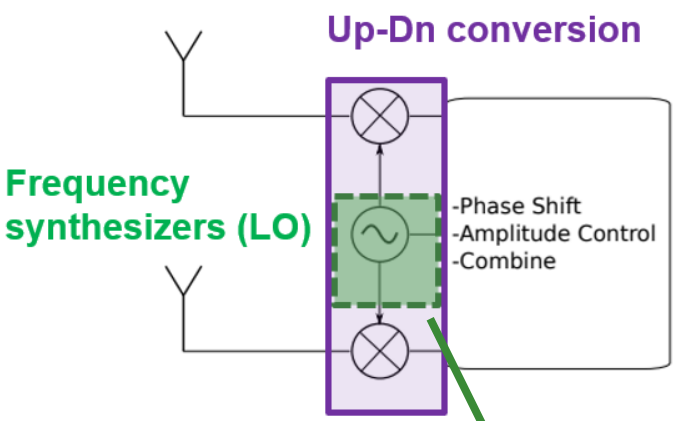
- Phased array systems exploit the use of multiple antennas to increase the directivity of the equivalent antenna resulting in a greater resilience to the spatial interference, an improvement of the signal-to-noise ratio and higher power
- Different architectures possible depending on target frequency and performance/flexibility demand
- Challenging RF-mmWave circuits of the phased array system are **Frequency Synthesizers** and **Up-Down Converter**

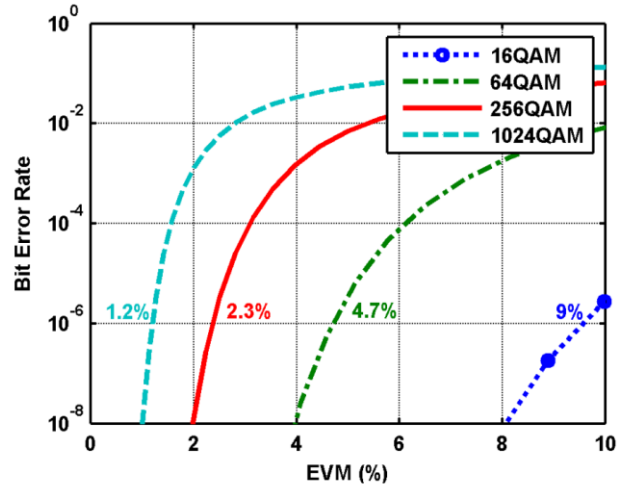


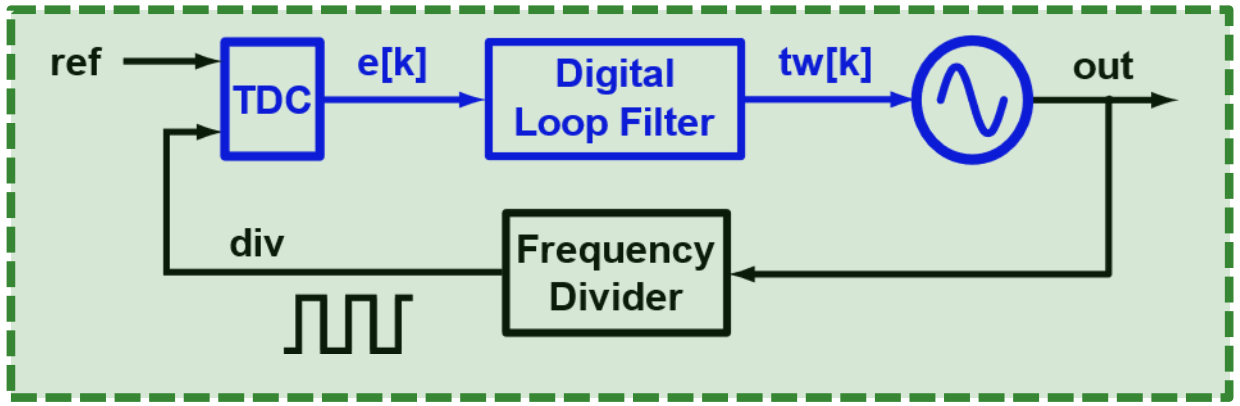


Frequency Synthesizers

- Frequency synthesizers provide the LO signal to the system
- Jitter requirement is proportional the modulation complexity, 1024QAM require <50fs PLL jitter (6G perspective)
- Digital PLL provide many advantages
  - Area optimization
  - Power optimization
  - Flexibility/configurability
  - Superior jitter performance



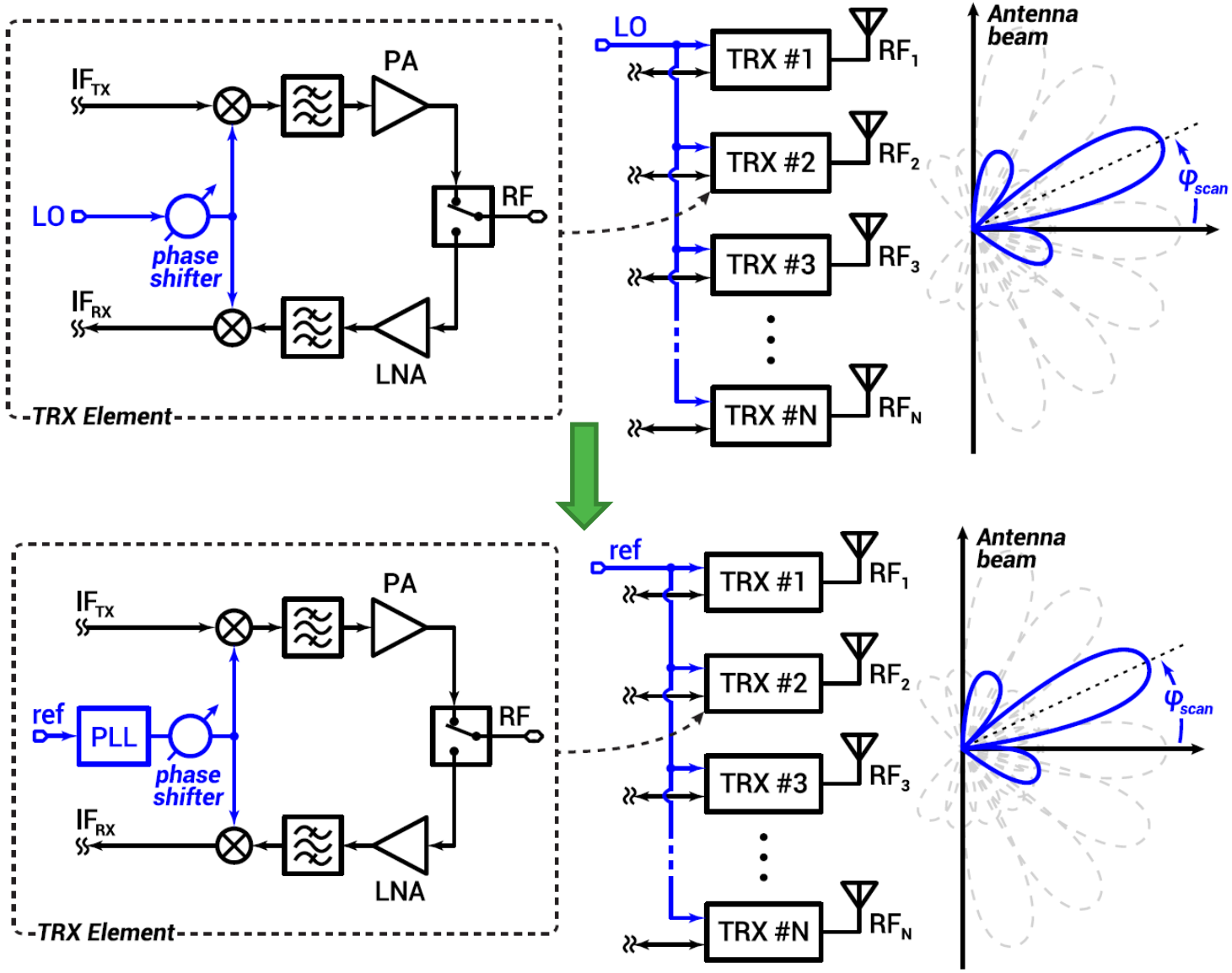




LO and Phased Array

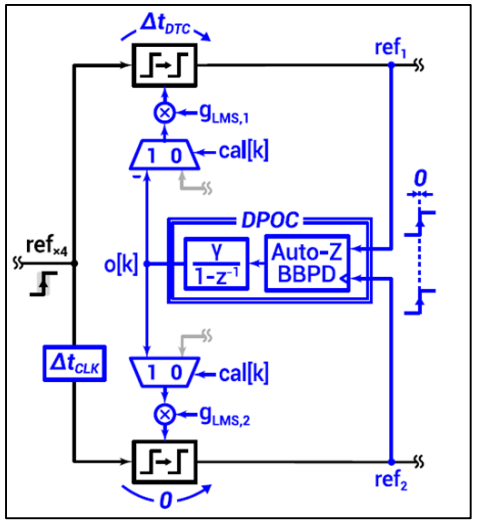
- The phase-shifter in the LO path enables higher beam steering accuracy than in the RF/IF phase-shifting cases

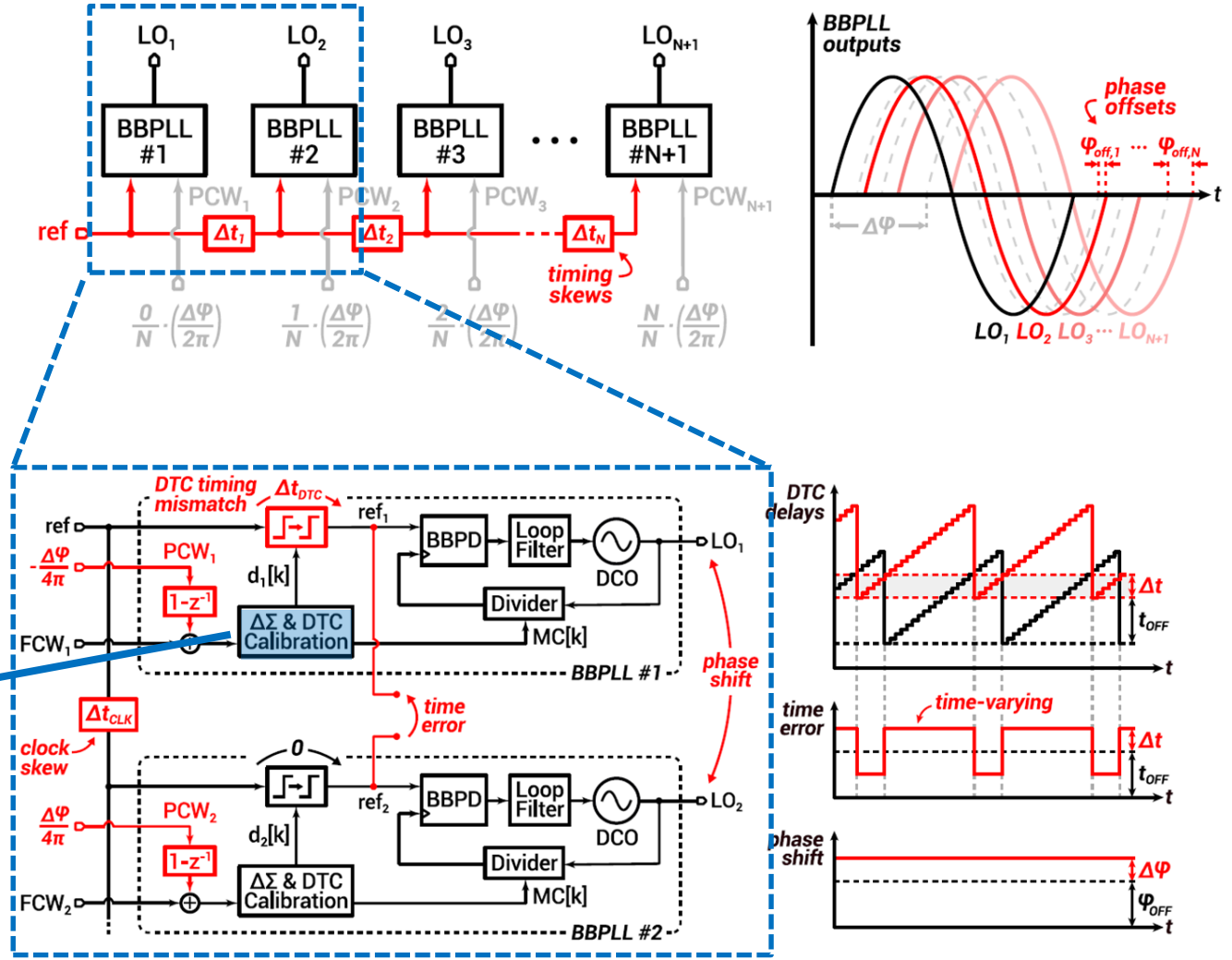
- Avoids routing of the mmW LO signal on the IC and allows 10·log(N) reduction in PLL PN from over-the-air coupling
- PLL can do phase shifting



DPLL in Phased Array System

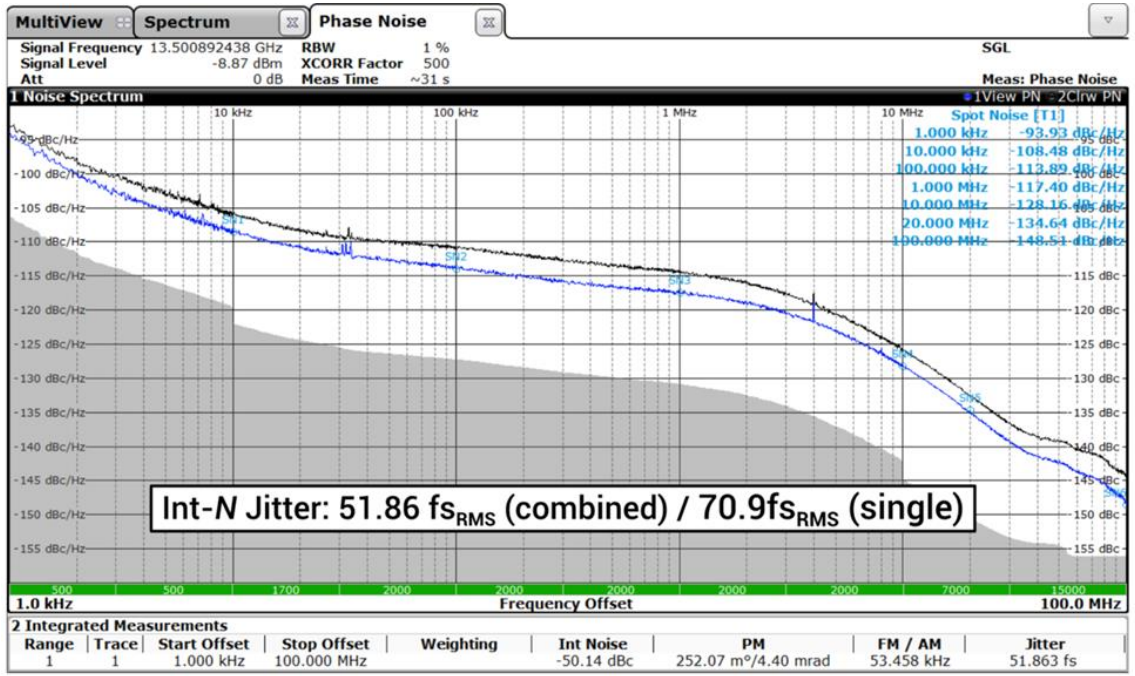
- Skew and mismatch on reference clock path introduces phase shift inaccuracies
- Digital Phase Offset Correction (DPCO) unit senses the offset and cancels it via DTC



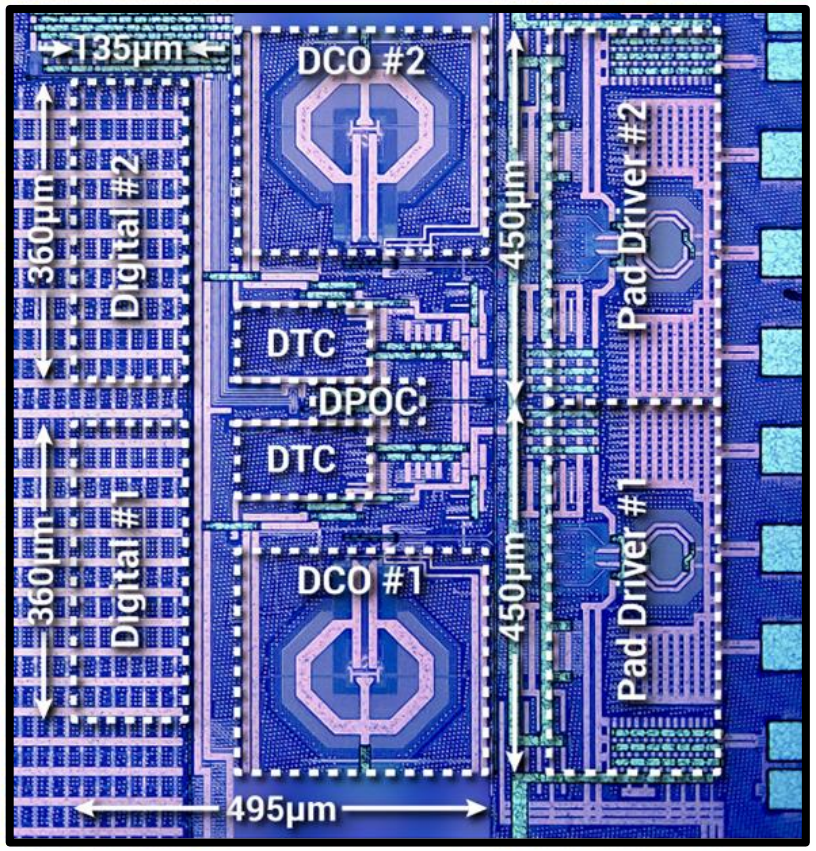


DPLL Measurements

- Implemented in 28nm CMOS Bulk, active area 0.21mm², Power 10.9mW
- F_{out} :12.9 to 15.1 GHz
- Jitter/Noise performance
  - 70,9fs (1k-100M) Single element ➔ PN @1 MHz= -114,6 dBc/Hz
  - 51,86fs (1k-100M) Combined ➔ PN @1 MHz= -117,4 dBc/Hz



Die Micrograph



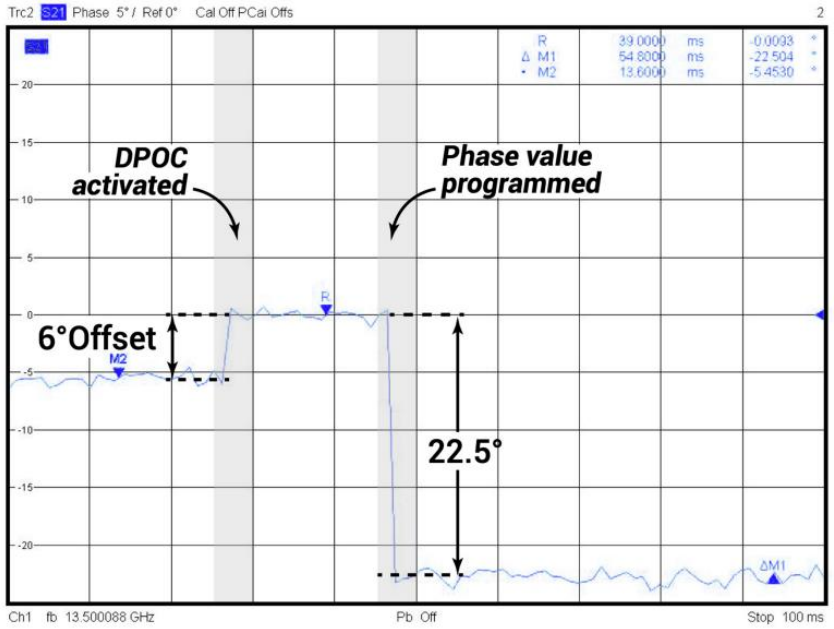
*ISSCC2021

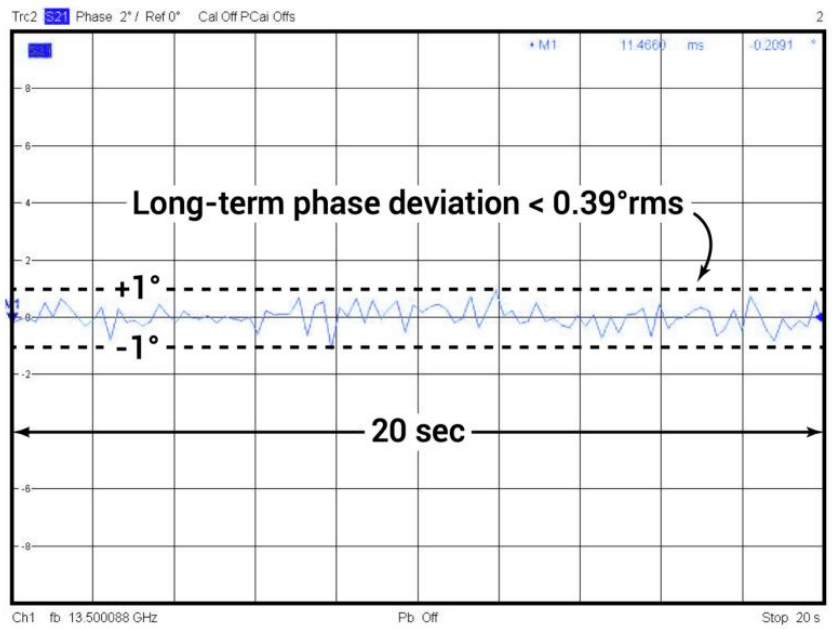
DPLL Phase-shifting measurements

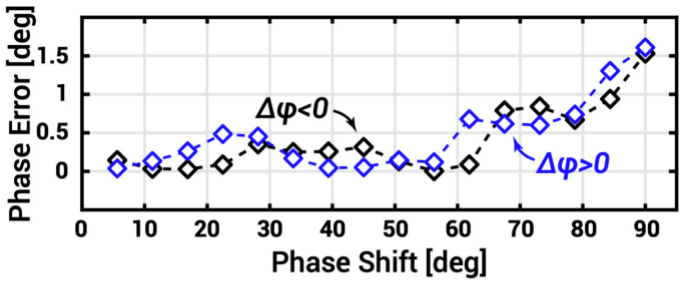
- Phase Resolution 0.7m° (19bit)
- Phase-Error 0.6°rms
- Settling-Time <1.05us
- Long –term phase deviation < 0.39°rms

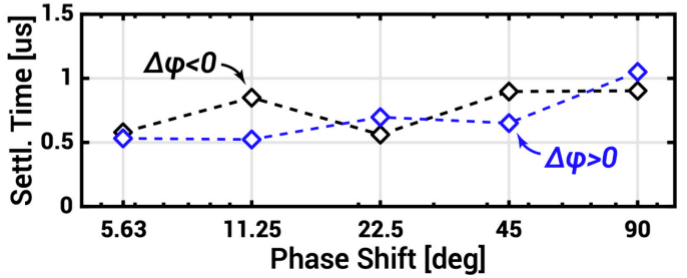
	This Work	J. Pang JSSC 2019	L. Wu JSSC 2013
Phase-Shifting Method	Digital PLL Mod.	Active Analog	IL-Oscillator
Frequency Range (GHz)	12.9-to-15.1	26.5-to-29.5	42.75-to-49.5
Resolution	0.7m° (19 bit)	11m° (15 bit)	22.5° (4 bit)
Phase-Error RMS/Peak	0.6°/1.6°	0.3°/5.1°	0.93°/1.5°
Max Settling Time (μs)	1.05	N/A	N/A
*Power (mW)	10.8	26.6**	21.25**
*Active Area (mm²)	0.21	0.39**	0.7**
Process	28nm CMOS	65nm CMOS	65nm CMOS

*Specified for one element **Not including LO generation



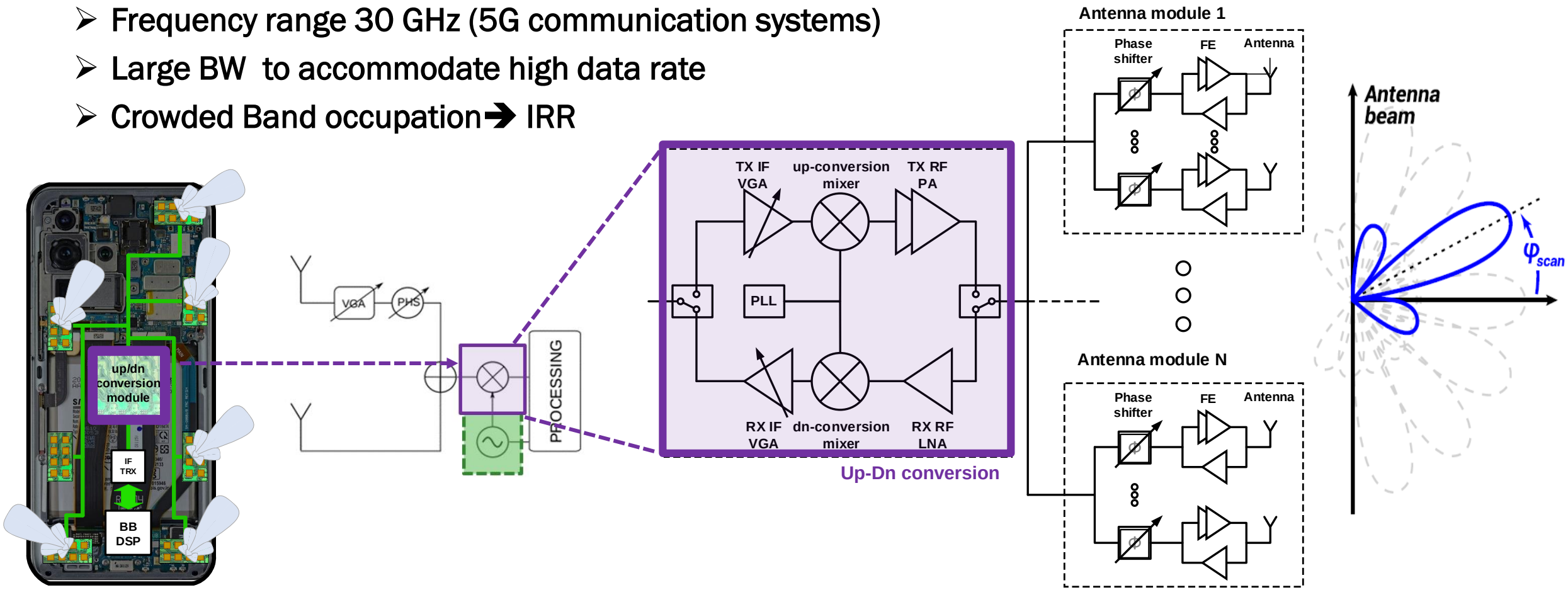






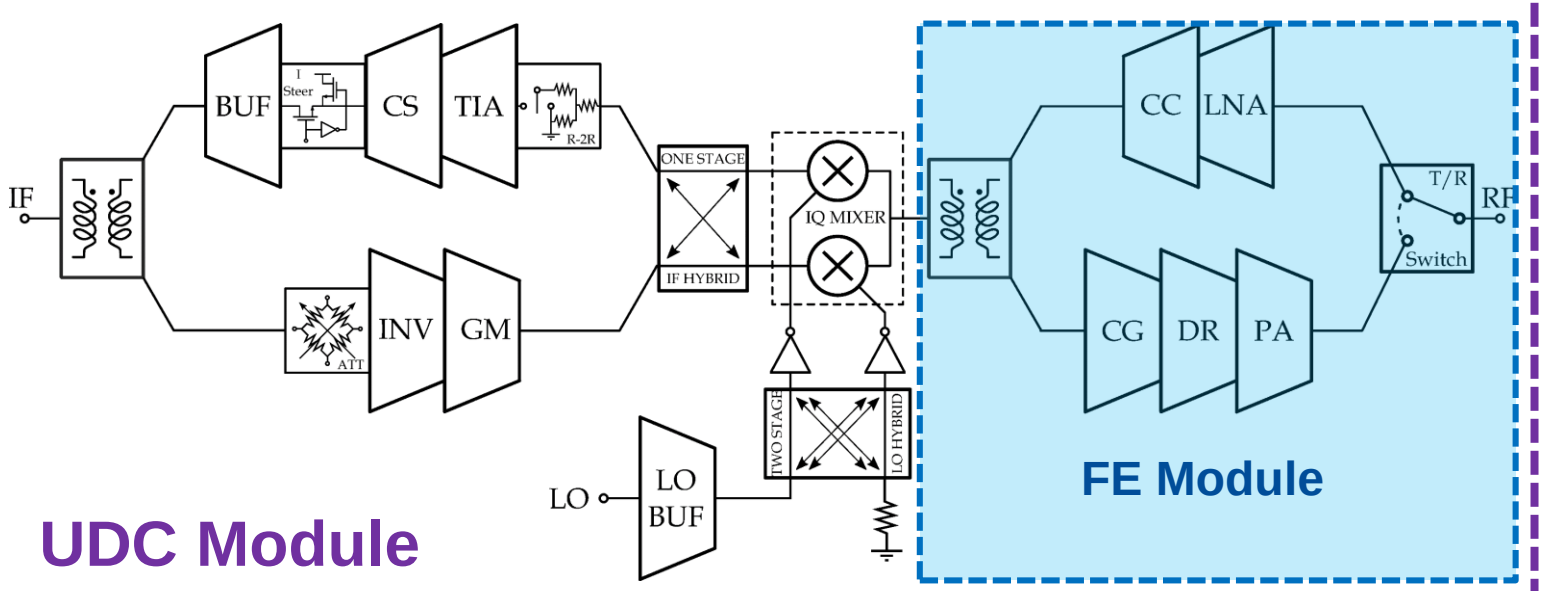
Up-Down Conversion

- Signal conversion from IF to RF in Phased array circuits is challenging
  - Area and Power optimization
  - Frequency range 30 GHz (5G communication systems)
  - Large BW to accommodate high data rate
  - Crowded Band occupation➔ IRR



UDC module overview

UDC Spec	Value
RF range	**24 … 31 GHz**
LO frequency range	**21 … 28 GHz**
IF frequency (fixed):	**3 GHz**
Target TX $P_{1dB,out}$	**13-15dBm**
Target RX $P_{1dB,out}$	**~0dBm**
TX conversion gain	**15 … 25 dB**
RX conversion gain	**10 … 30 dB**
TX/RX Image Rejection	**>35 dB**

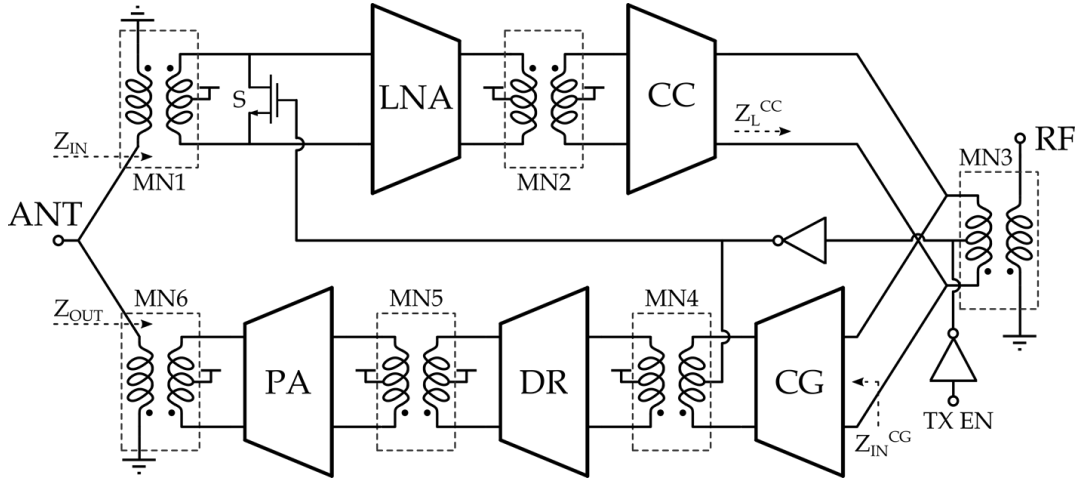


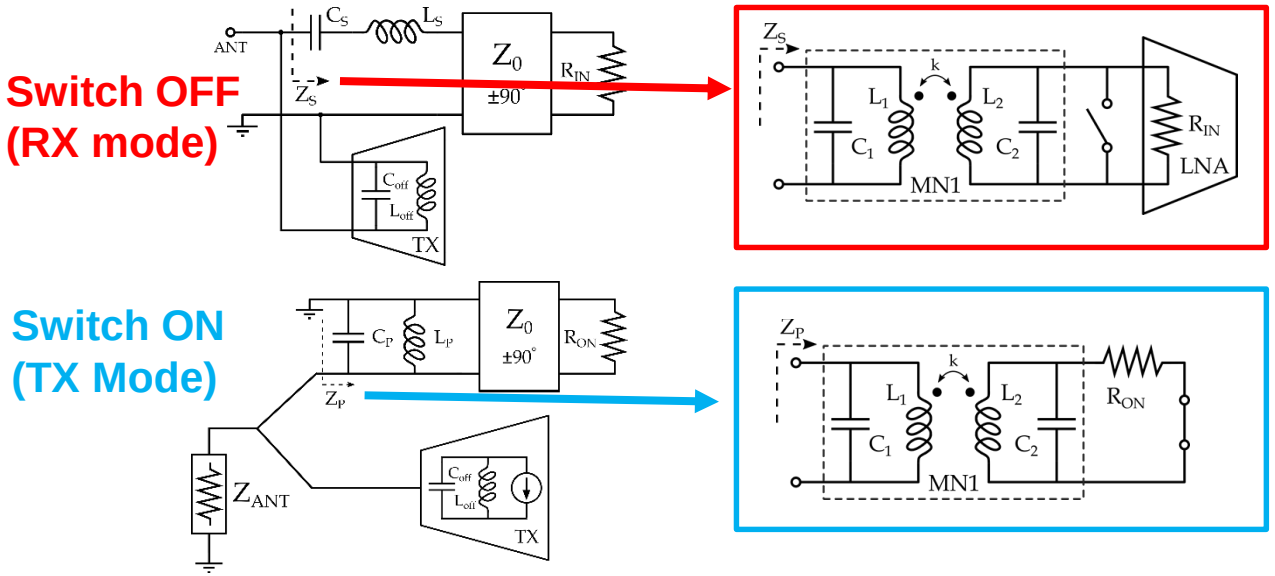
- UDC Architecture
  - Bidirectional to increase area efficiency of phased array
  - Low IF for better power consumption, RX linearity, need for Image-reject architecture
  - Bi-directional passive mixer with IQ generation

Front End Spec	Value
BW RX and TX	22 … 31 GHz
GT RX	17dB
GT TX	19dB
NF	<5dB
P_{1dB}	14dBm
PAE @ P_{1dB}	20%

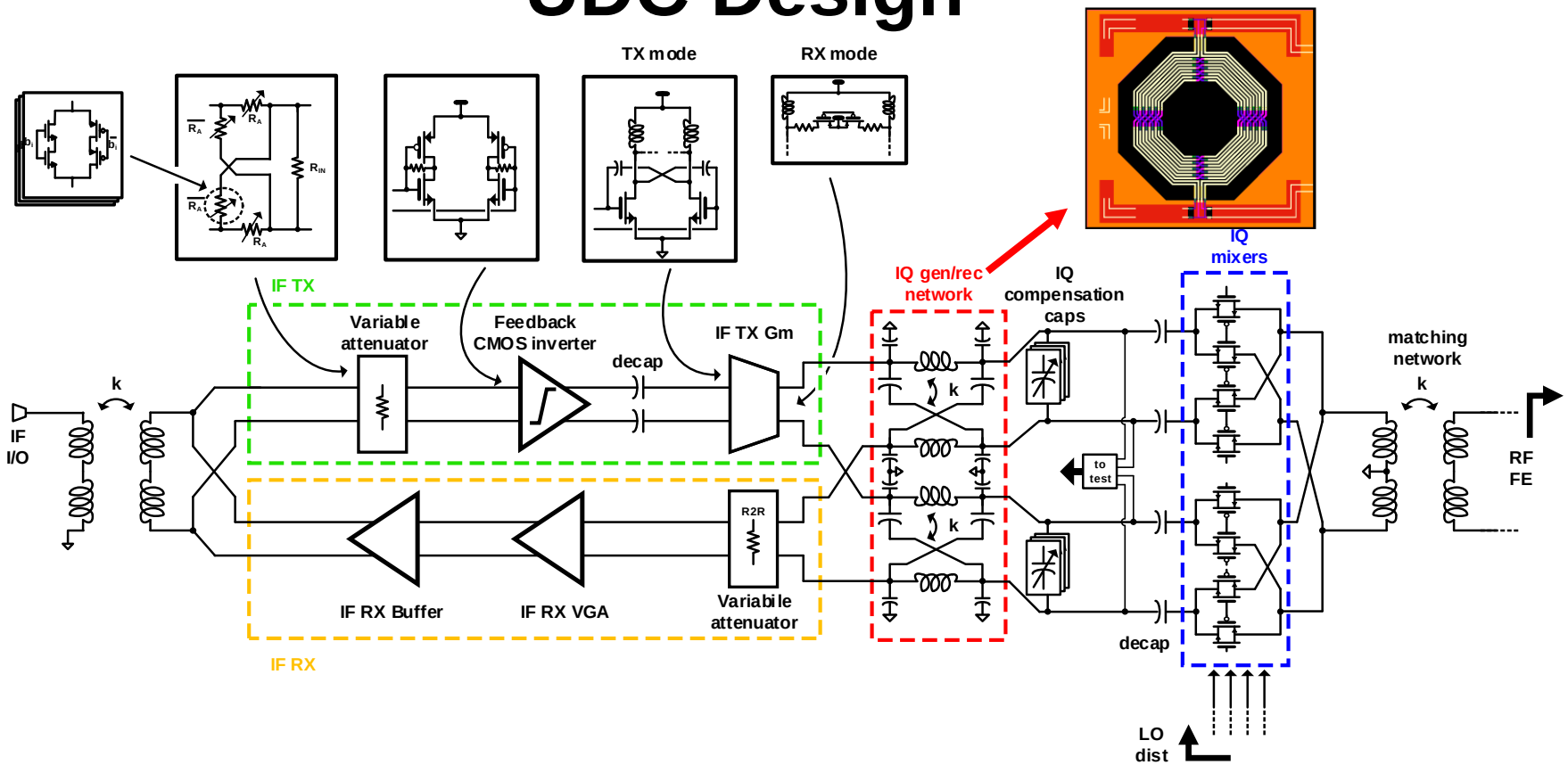
FE Module Design

- Front-End Architecture
  - TX-RX share same antenna
  - T/R switch based on transformer used as impedance inverter saving area respect to common λ/4 T-line
  - RX based on inductively degenerated LNA plus Cascode stage for better gain and isolation
  - PA stage and driver stage are using neutralized common source topology
  - Commong gate stage used as input for the matching
  - Design based on Broadband impedance trasformation featuring in-nand constant group delay





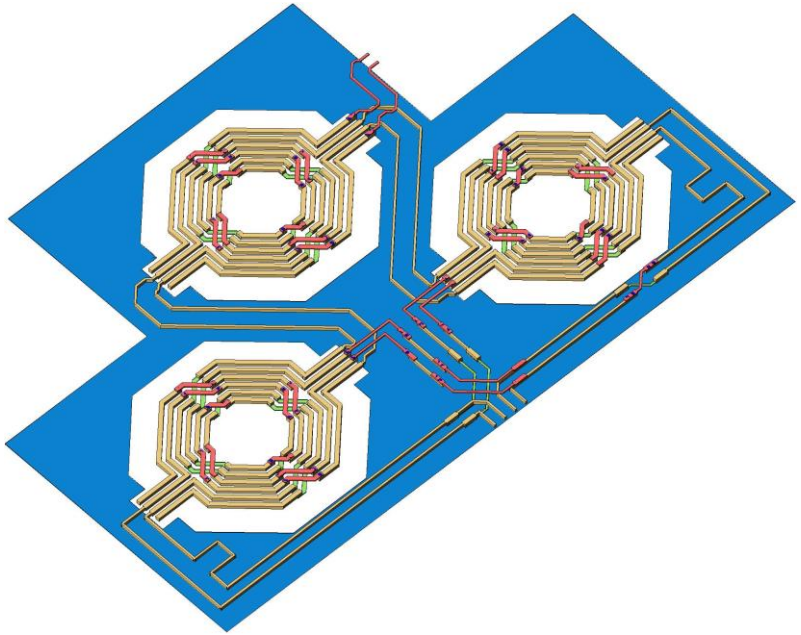
UDC Design

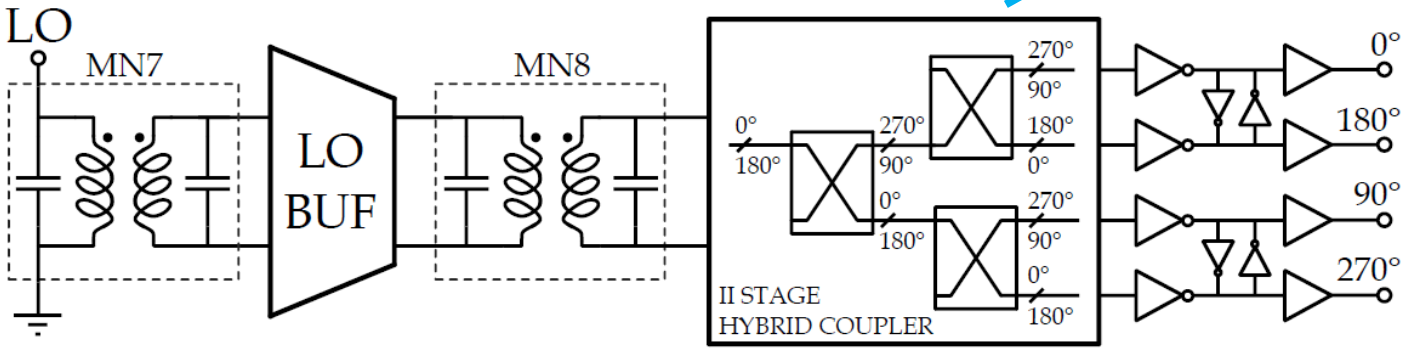


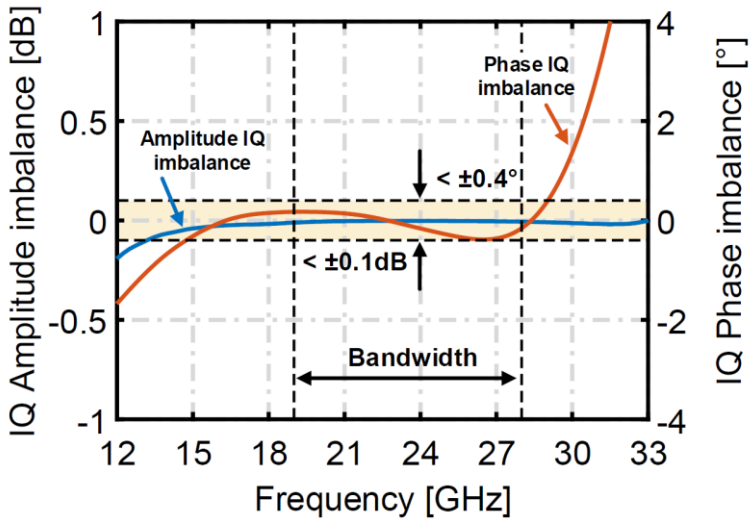
- UDC Design
  - IQ bidirectional network with calibration circuitry to balance IQ path in TX and RX
  - IQ passive mixer architecture based on transmission –gate to achieve high linearity and power
  - RX IF: three stage amplifier with TIA and R-2R for matching and having variable gain configurations
  - TX IF: two stage amplifier, resonant load for gain and linearity enhancement plus variable attenuator for gain control which set high impedance in RX mode

UDC –Wideband IQ generation

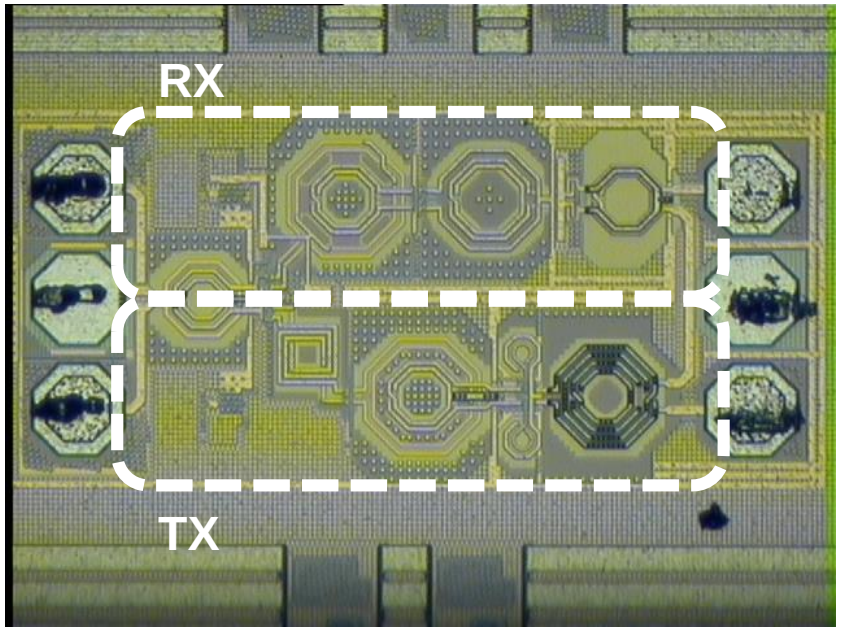
- IQ genaration based on hybrid coupler
- Multi-stage hybrid couplers can be levaraged to increase bandwidth and reduce quadrature error
- Saturated amplifiers reduce amplitude mismatch between I and Q path





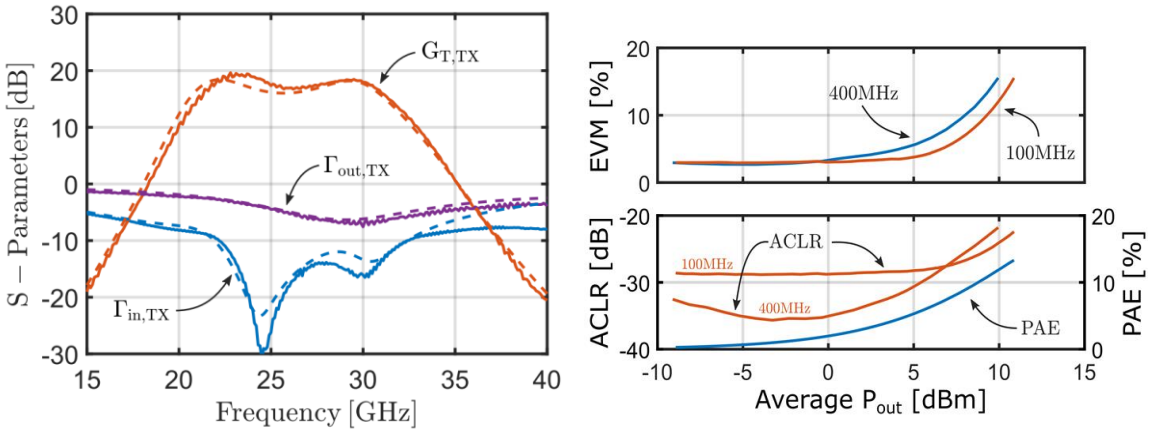


FE Module Measurements

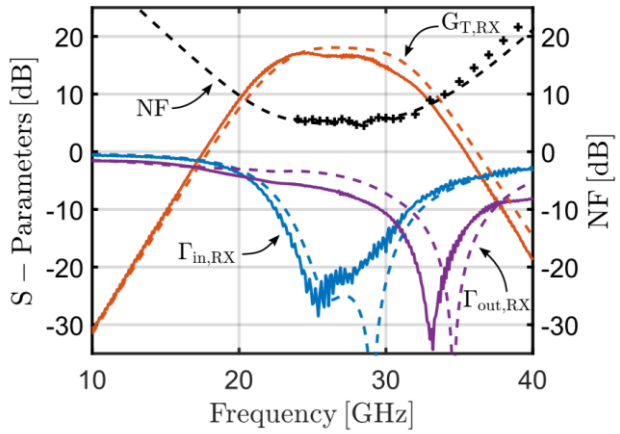


- Technology: 28nm bulk CMOS by TSMC
- Small area of 0.25mm² due too compact implementation of bi-directional transceiver with tansformer based T/R switch
- 5% EVM at $P_{out}^{avg} = 4.3dBm$ 64-QAM OFDM
- Wideband transformer design allows 9 GHz BW

Transmitter Path

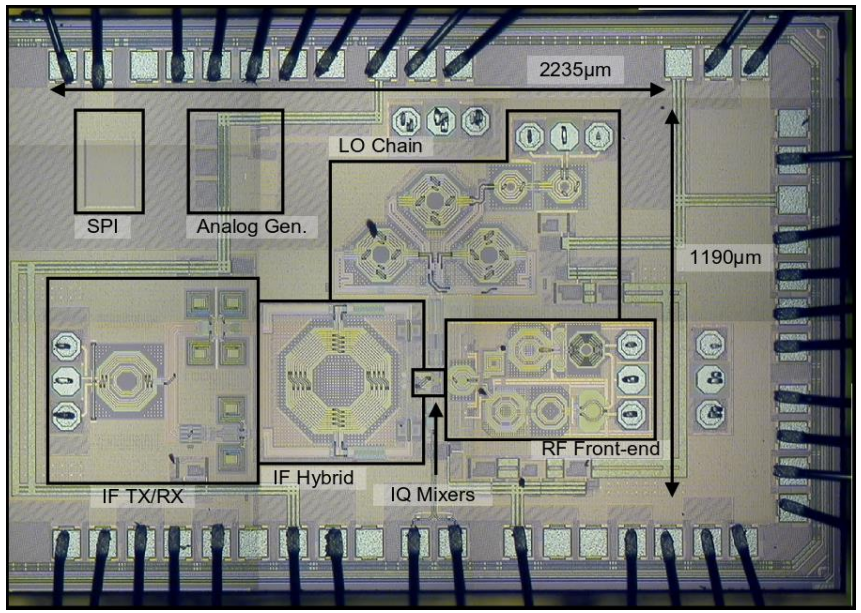


Receiver Path



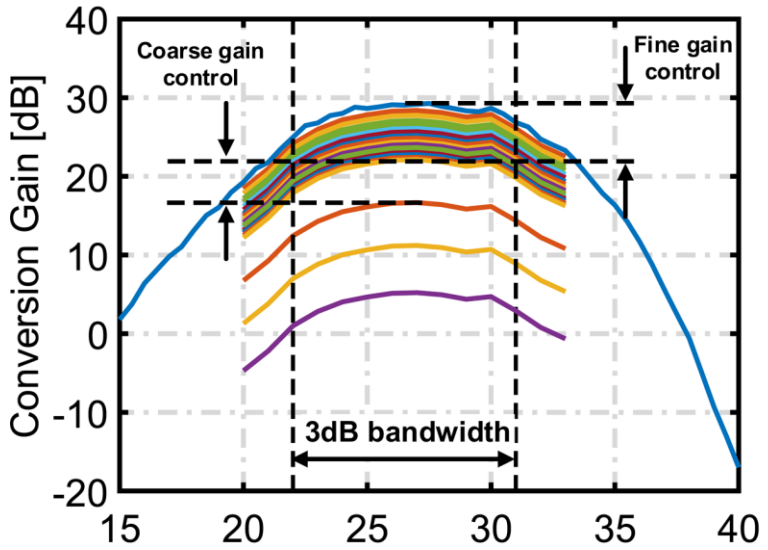
*ESSCIRC2021	This Work	[2]	[5]	[3]	[1]
CMOS Tech.	28 nm	65 nm	65 nm	28 nm	65 nm
Freq. [GHz]	22-31	27	26.5-29.5	28.5	24-28
Supply [V]	0.9	1	-	1.05	-
TX gain [dB]	19	35	20	35	27*
TX P_{1dB} [dBm]	14	14.4	11.3	9.5	16.1
TX PAE_{1dB} [%]	18.7	14.5	-	8.5	16.6
RX NF [dB]	4.9	5.9	4.2-5	5.6	4.4
RX gain [dB]	17	25.5	17	24	23.2
$P_{DC,RX}$ [mW]	35	50	112	50	40
Area [mm²]	0.25	0.26	0.58	0.52	0.94

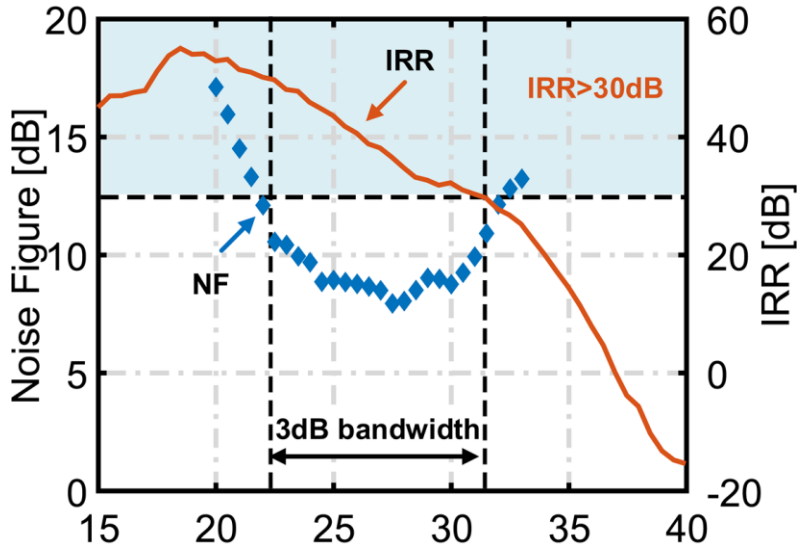
UDC Module Measuremens

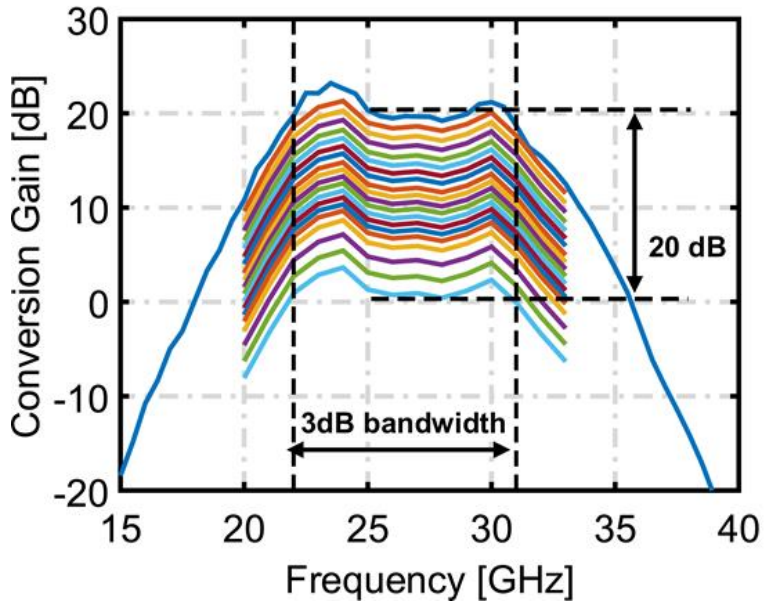


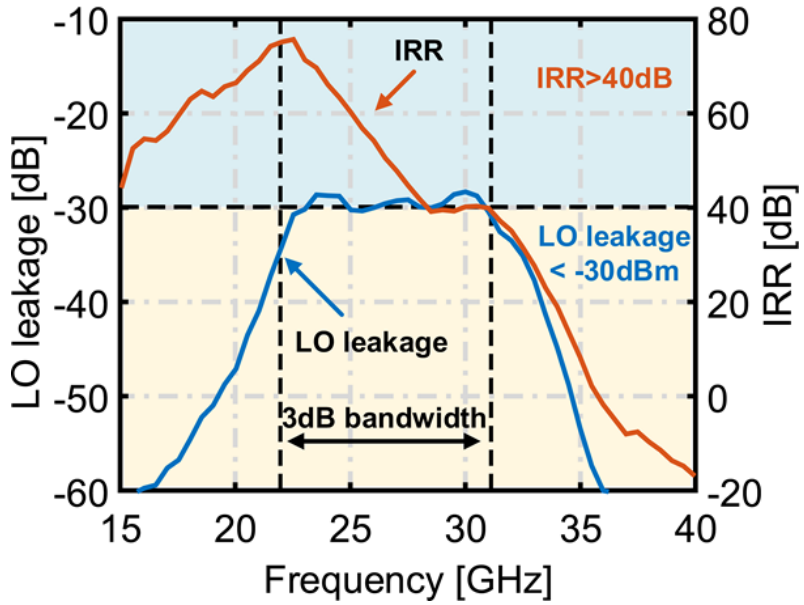
- Technology: 28nm bulk CMOS by TSMC
- RX P_{DC} 110 mW
- TX P_{DC} 220 mW @ P_{1dB}

Published in JSSC 2022

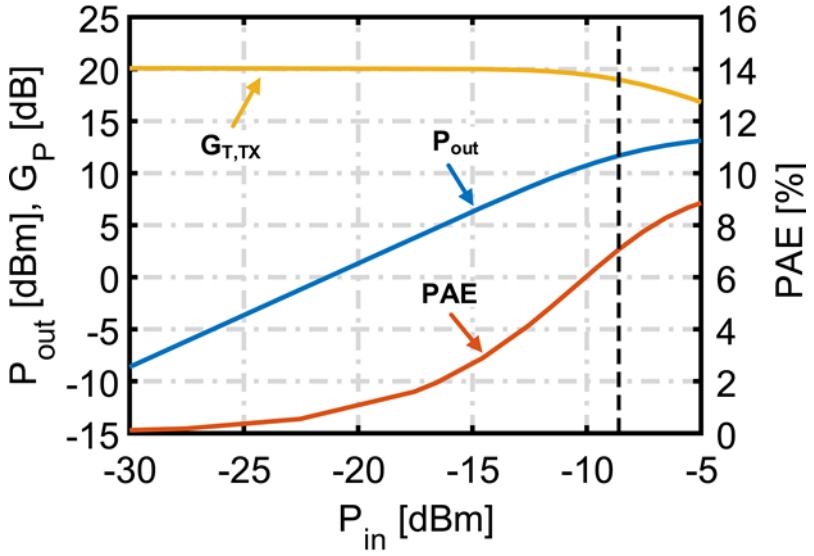


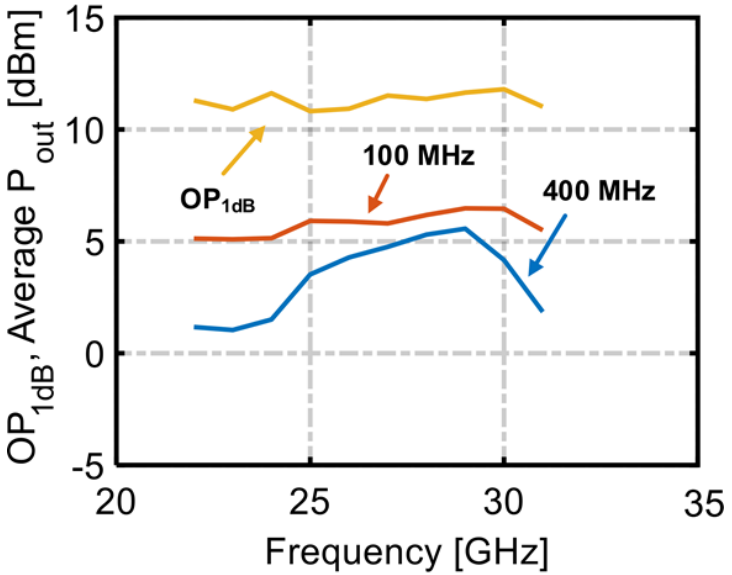




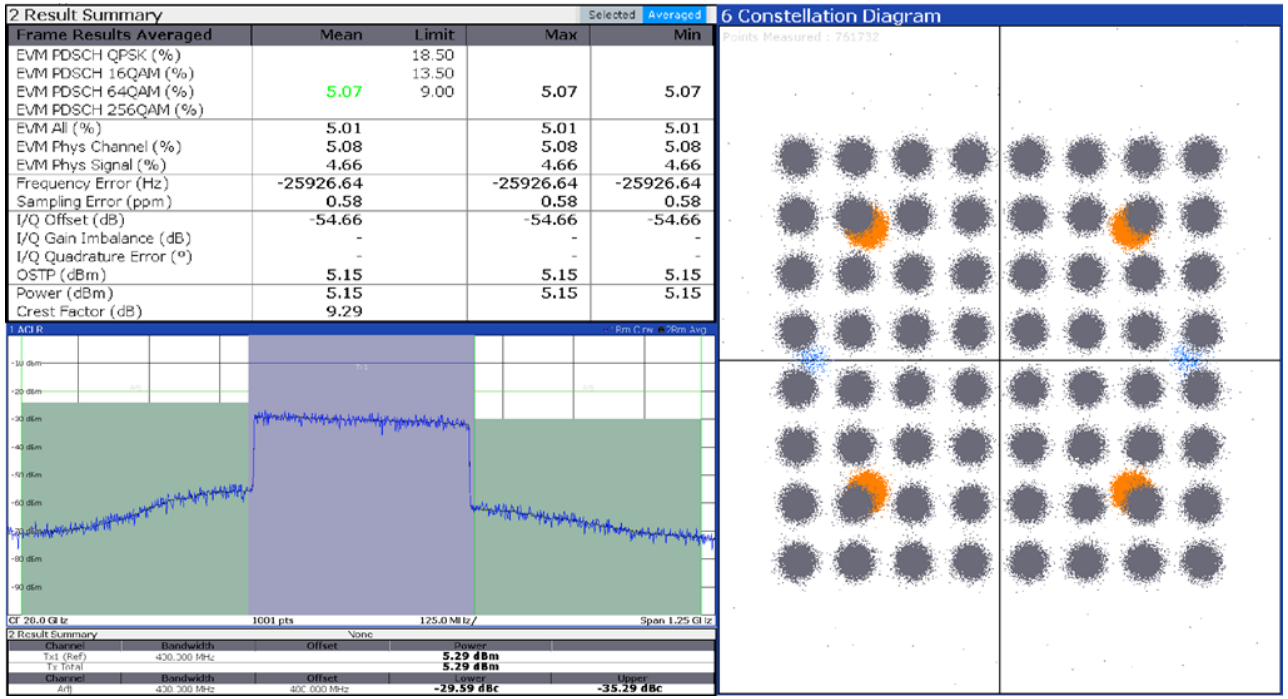


UDC Module – Large signal measurements





- Technology: 28nm bulk CMOS by TSMC
- P_{1dB} of 11.5 dBm
- 20 dB gain variation with 1-dB-fine-step control
- IRR > 40 dB, LO leakage < -30 dBm
- Tested with 64-QAM OFDM signals with PAPR = 10dB



2 Result Summary

Frame Results Averaged	Mean	Limit	Max	Min
EVM PDSCH QPSK (%)		18.50		
EVM PDSCH 16QAM (%)		13.50		
EVM PDSCH 64QAM (%)	5.07	9.00	5.07	5.07
EVM PDSCH 256QAM (%)				
EVM All (%)	5.01		5.01	5.01
EVM Phys Channel (%)	5.08		5.08	5.08
EVM Phys Signal (%)	4.66		4.66	4.66
Frequency Error (Hz)	-25926.64		-25926.64	-25926.64
Sampling Error (ppm)	0.58		0.58	0.58
I/Q Offset (dB)	-54.66		-54.66	-54.66
I/Q Gain Imbalance (dB)	-		-	-
I/Q Quadrature Error (°)	-		-	-
OSTP (dBm)	5.15		5.15	5.15
Power (dBm)	5.15		5.15	5.15
Crest Factor (dB)	9.29			

Conclusion

- RF-mmWave circuits for Phased Array communication system in 28nm CMOS has been presented
- A 12.9-15.1GHz BBPLL-based LP Phase-Shifting System with < 100fs_{RMS} jitter with
  - Direct phase-modulation to avoid mmWave phase shifters and LO distribution
  - DPOC technique to cancel phase mismatches in background achieving 0.7m° phase resolution
- Broad band (22-32 GHz) bidirectional transceiver plus up/down converter module in 28nm CMOS featuring compact area and suitable for TDD systems with IRR > 30 and 40 dB in RX and TX modes, respectively