

TU3C-4

A 26-32GHz 6-bit Bidirectional Passive Phase Shifter with 14dBm IP1dB and 2.6° RMS Phase Error for Phased Array System in 40nm CMOS

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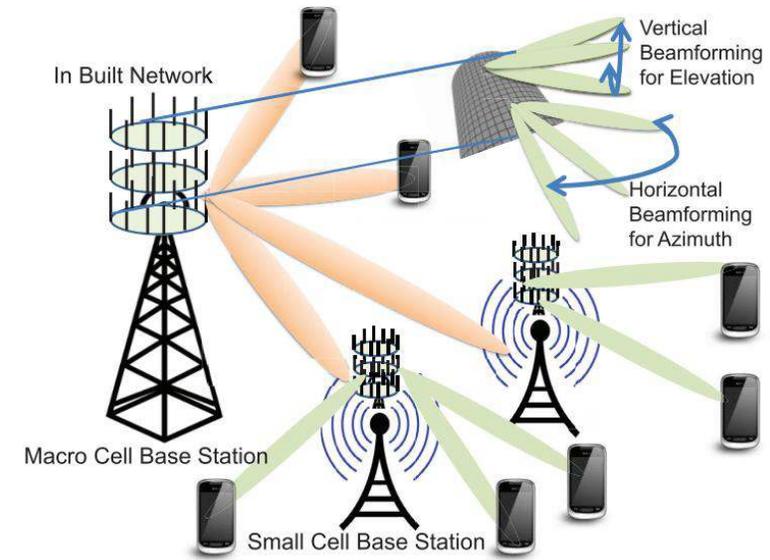
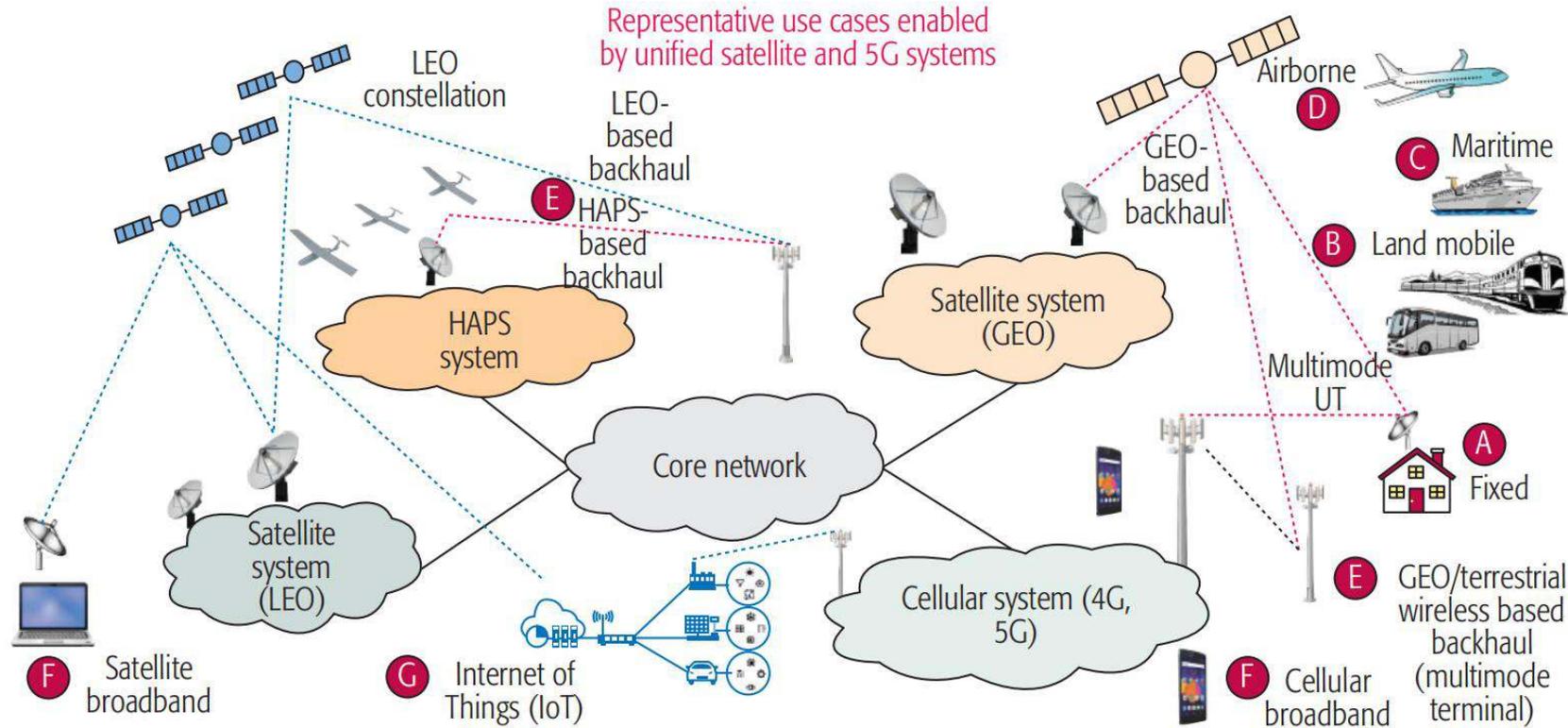
²East China Research Institute of Electronic Engineering, Anhui, China

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Outline

- **Introduction**
- **Circuit Design**
 - Architecture overview
 - Symmetric passive implementations
 - Passive Vector Modulator with linearity improvement technology
 - Multi-state inter-stage matching method
 - Bidirectional Phase-Shift Operation Principle
- **Measurement results**
- **Performance comparison**
- **Conclusion**

Application Background



[IEEE COMMUNICATIONS SURVEYS & TUTORIALS, M.Agiwal, 2016]
[IEEE Network, R. Gopa,I, 2018]

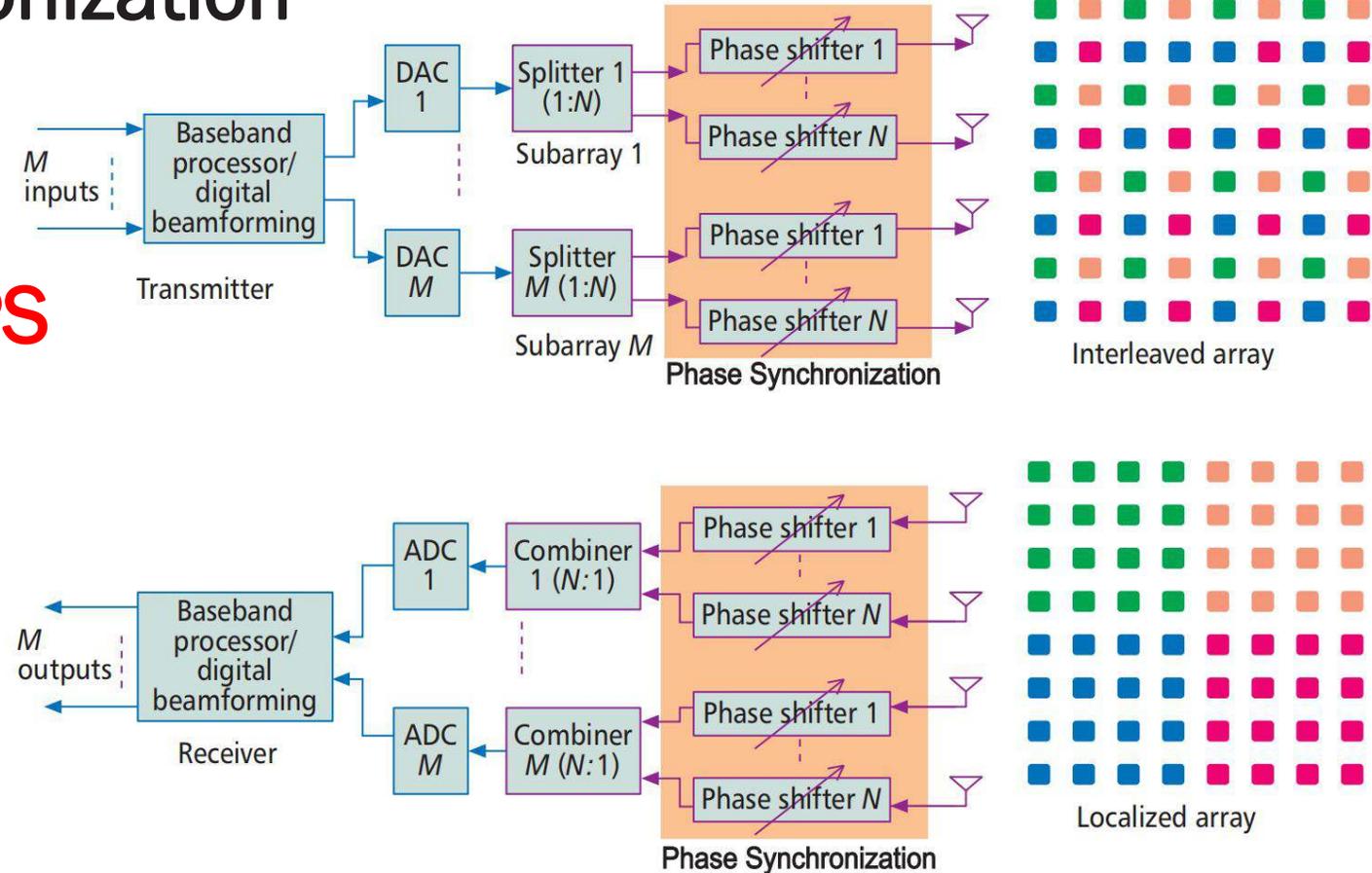
- K/Ka/Ku band Phased Array in 5G **Satellite Communication**
- Critical Technique : **Phase Synchronization** in beamforming

- Bidirectional Phase Synchronization

- Phase Shifter
- LO Clock Synchronization

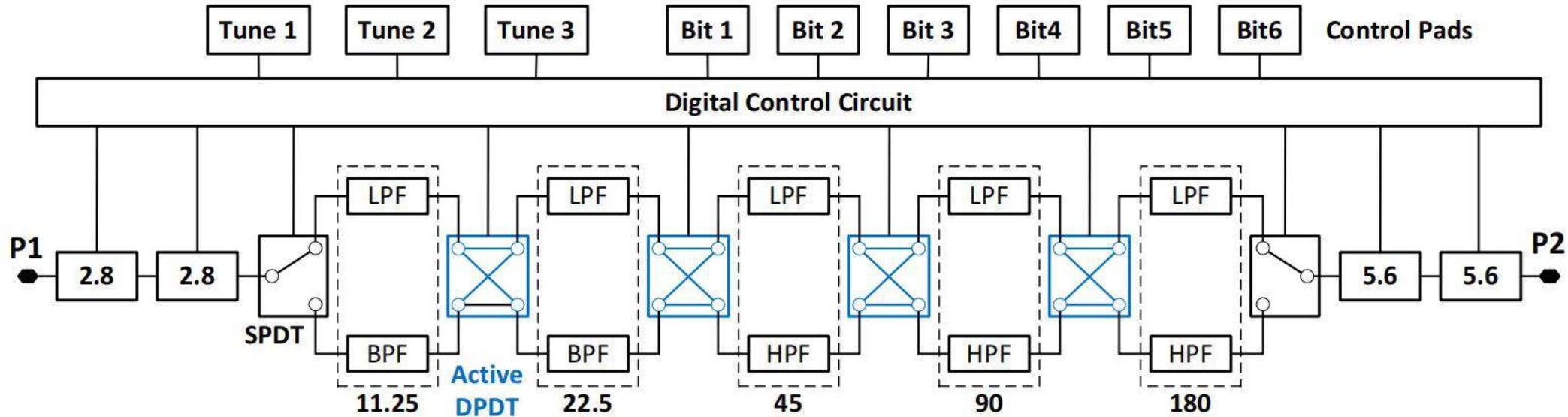
- Challenge of **Bidirectional PS**

- Design complexity
- Low power consumption
- Low imbalance
- High linearity
- High phase accuracy
- Moderate noise requirement



[IEEE Wireless Communication, Jian A. Zhang, 2015]

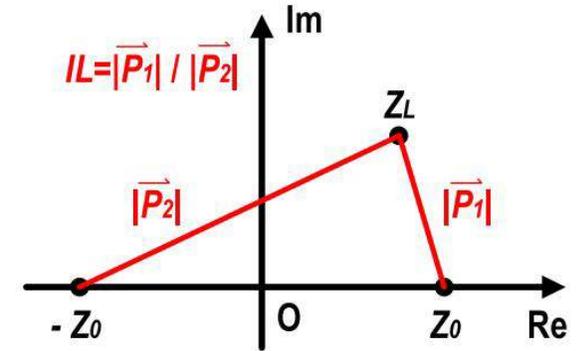
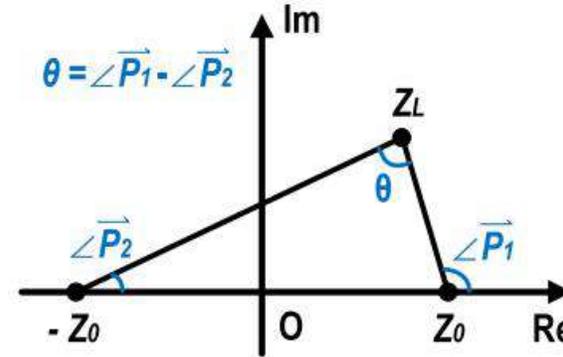
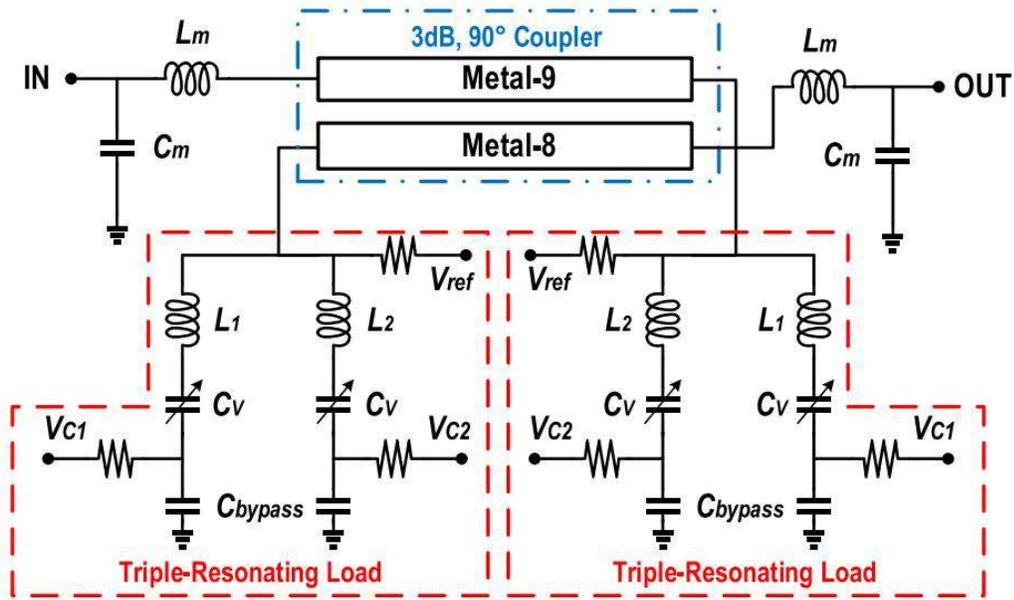
Switch-type Phase Shifter



- 😊 Simple structure
- ☹️ High power consumption
- 😊 Large nonlinearity
- ☹️ Large imbalance
- ☹️ Low phase accuracy

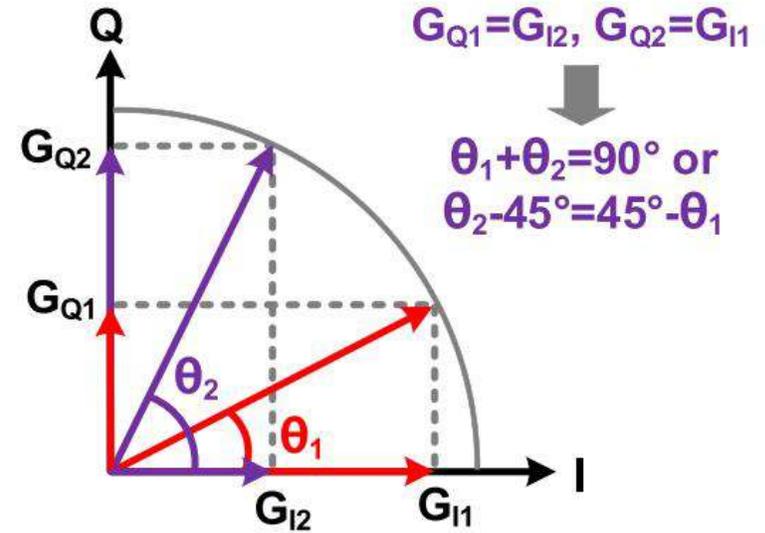
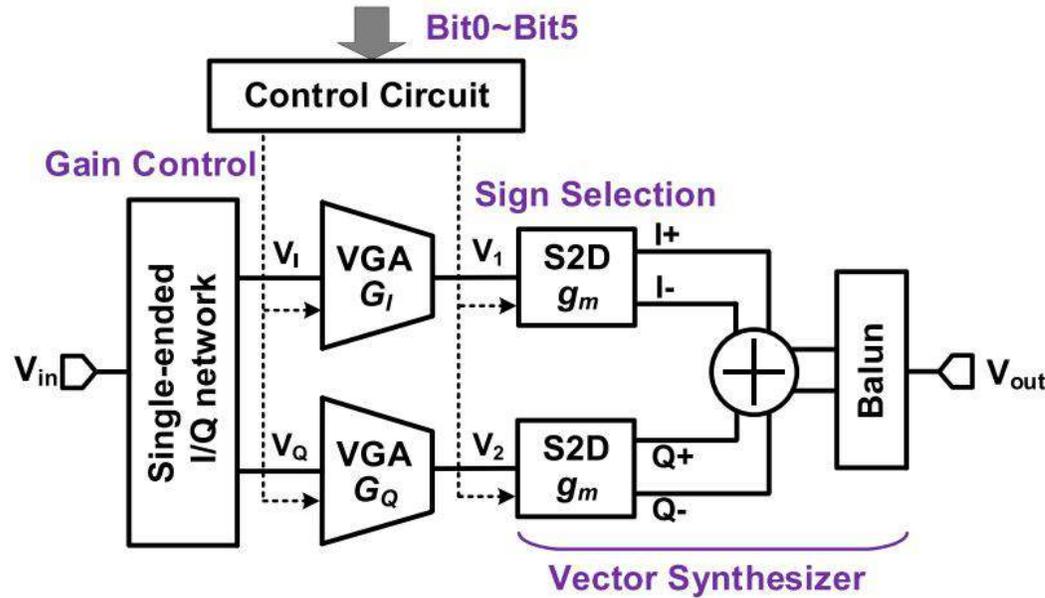
[ASSCC, Y.Gong, 2020]

Reflection-type Phase Shifter



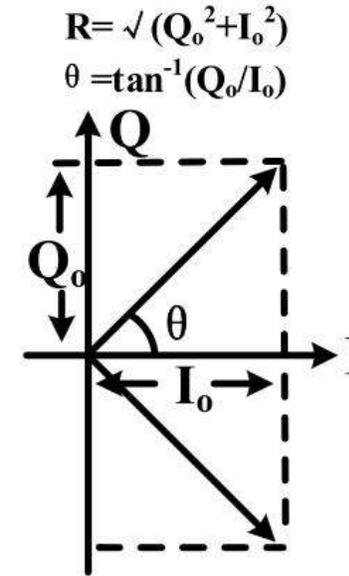
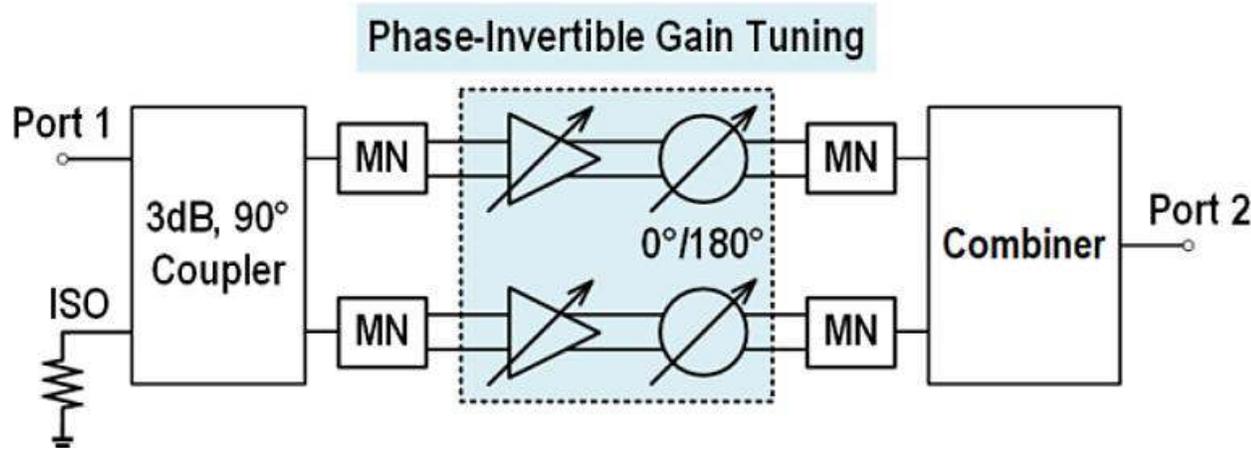
- ☹️ Signal frequency and process sensitive
- 😊 No power consumption
- 😊 High Linearity
- ☹️ Unilateral
- 😊 Moderate phase accuracy

[TMTT, Peng Gu, 2019]



[Access, T.Wu, 2020]

- ☹️ Design Complexity
- ☹️ Moderate power consumption
- 😊 Poor Linearity
- ☹️ Unilateral
- 😊 High phase accuracy

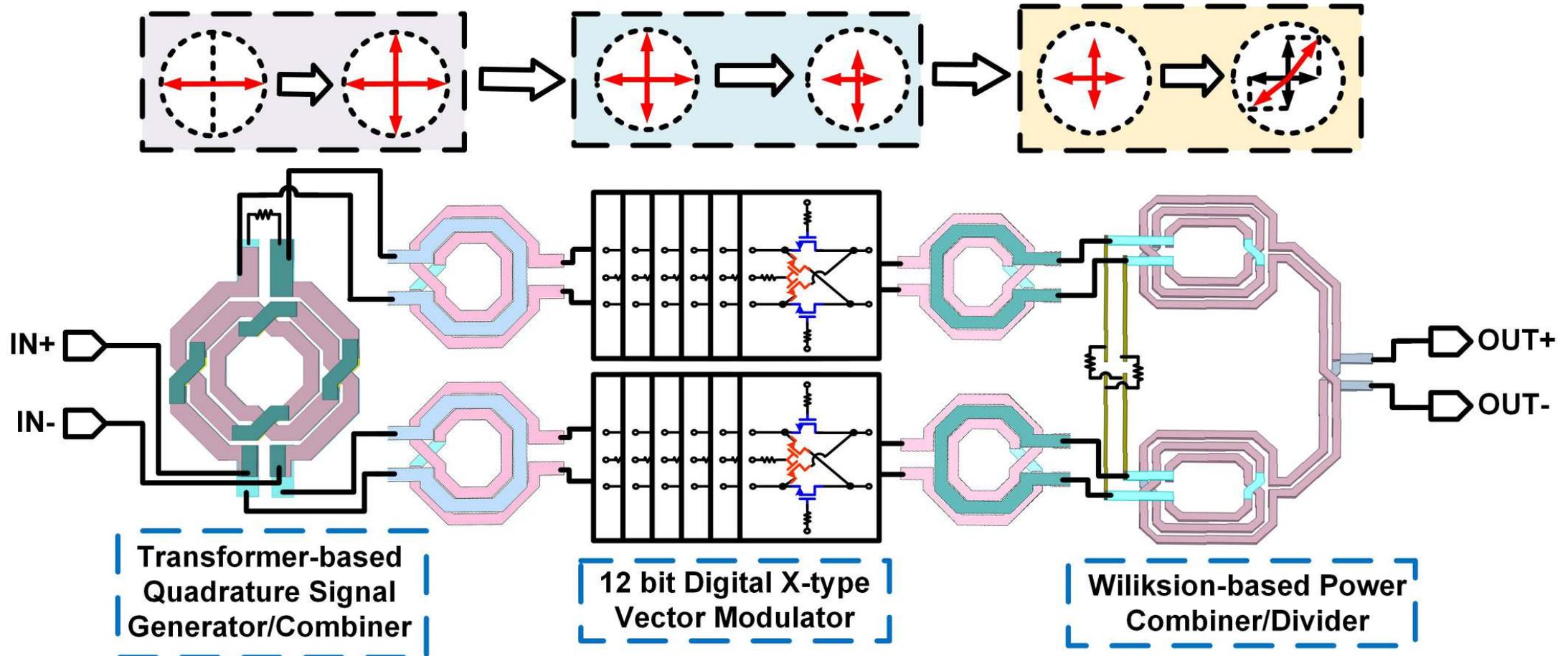


- ☹️ Design Complexity
- 😊 No power consumption
- 😊 High Linearity
- 😊 Low imbalance
- 😊 High phase accuracy

[TCAS-I, Peng Gu, 2021]

Architecture overview

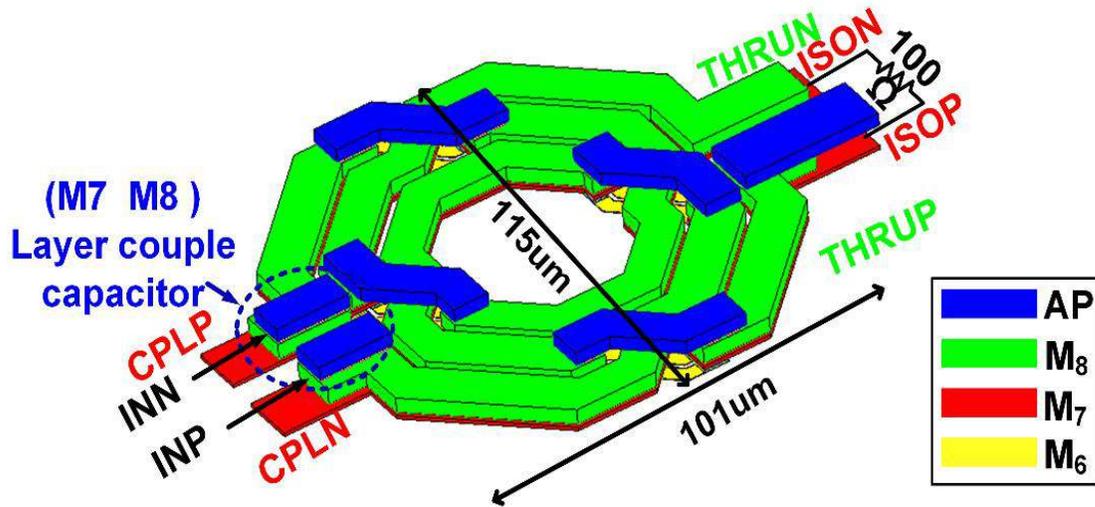
- Bidirectional Passive Vector Modulation Phase Shifter
 - Fully symmetric passive implementation



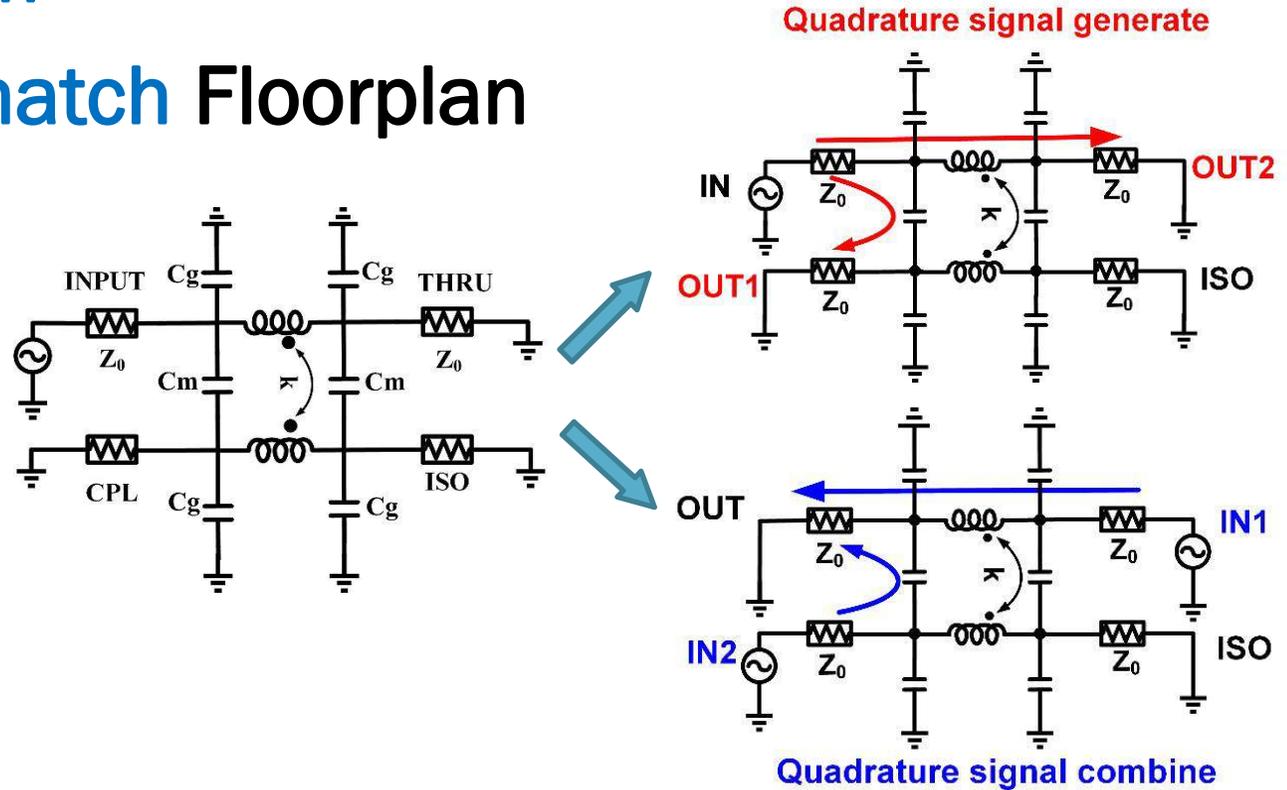
Vertically stacked metals coupled

Quadrature Signal Generator

- Compact Area: $101 \times 115 \mu\text{m}^2$
- Low imbalance and IQ mismatch Floorplan



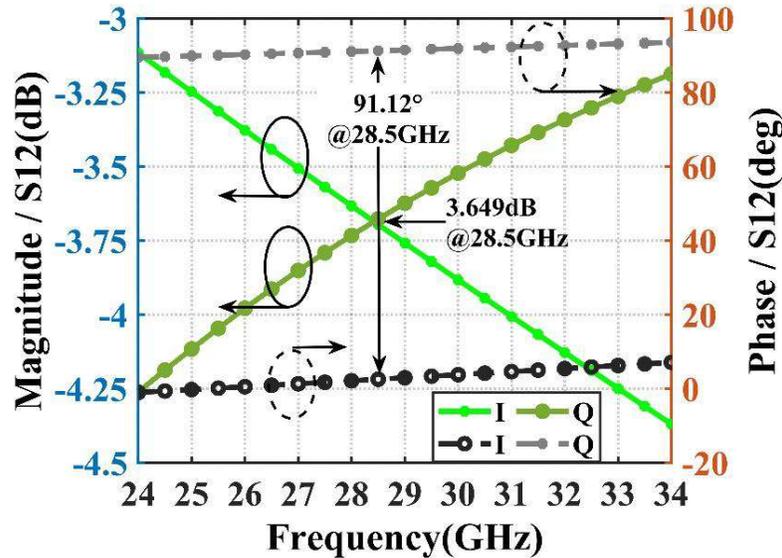
3D EM view of Quadrature Signal Generator



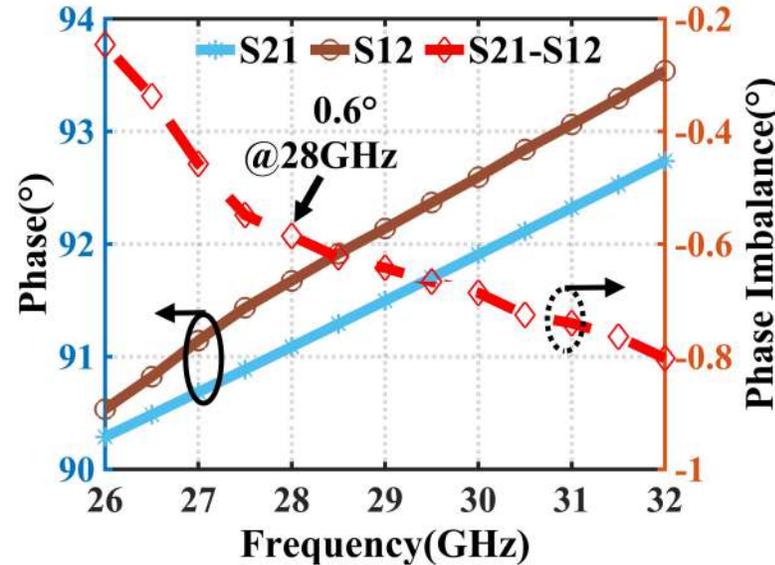
Equivalent circuit and bidirectional working principle

Vertically stacked metals coupled Quadrature Signal Generator

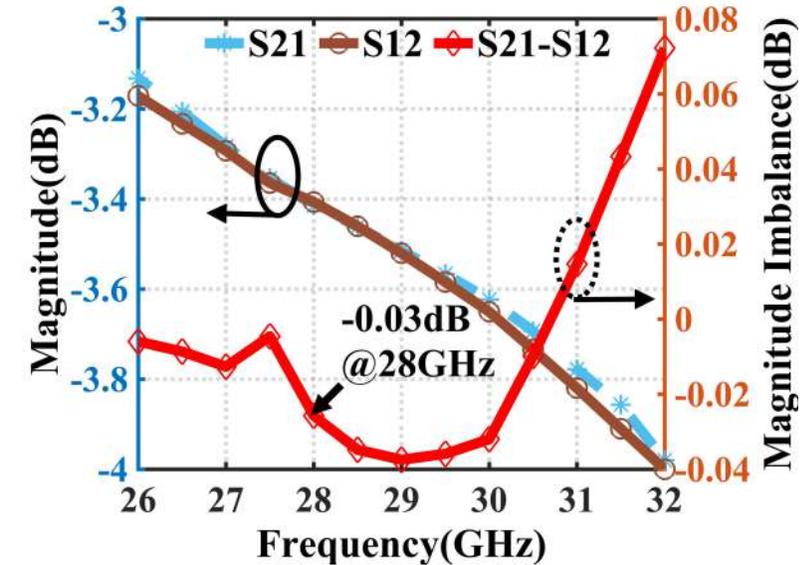
- Electromagnetic simulation from 26 to 32 GHz
 - Magnitude imbalance $<0.06\text{dB}$ and phase mismatch $<0.8^\circ$
 - Magnitude IQ mismatch $<0.7\text{dB}$ and phase IQ mismatch $<1.2^\circ$



IQ mismatch



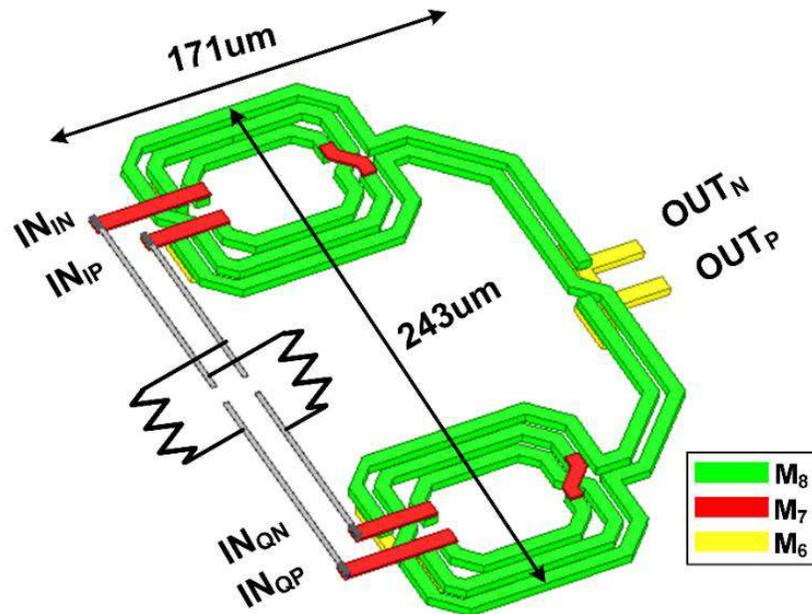
Phase imbalance



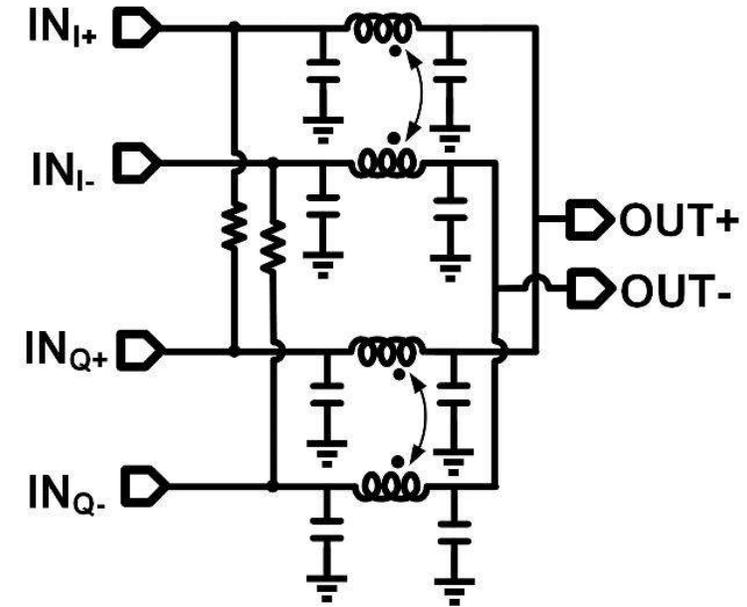
Magnitude imbalance

Wilkinson-based Differential Power Combiner/Divider

- Compact Area: $243 \times 171 \mu\text{m}^2$
- Low imbalance and IQ mismatch Floorplan



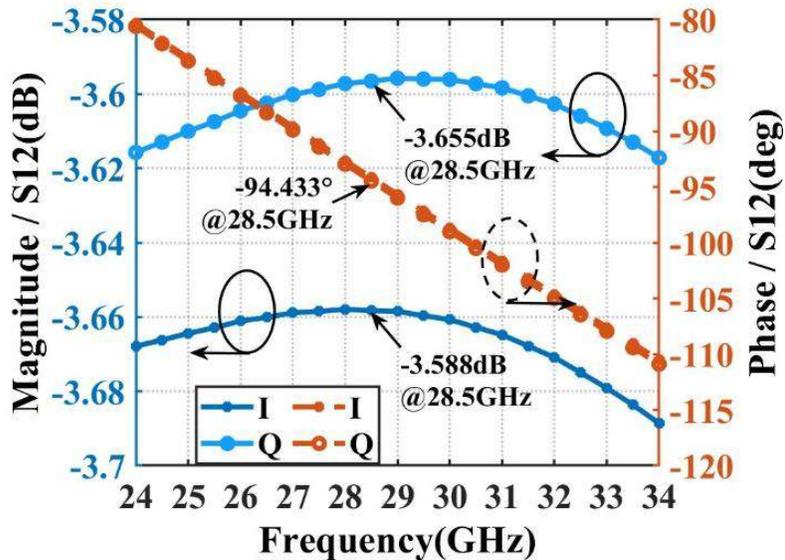
3D EM view of Power Combiner/Divider



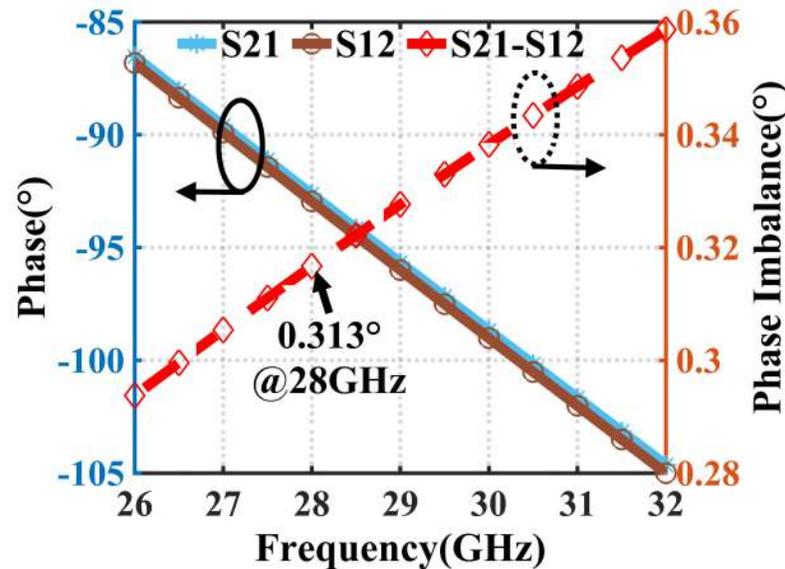
Equivalent circuit

Wilkinson-based Differential Power Combiner/Divider

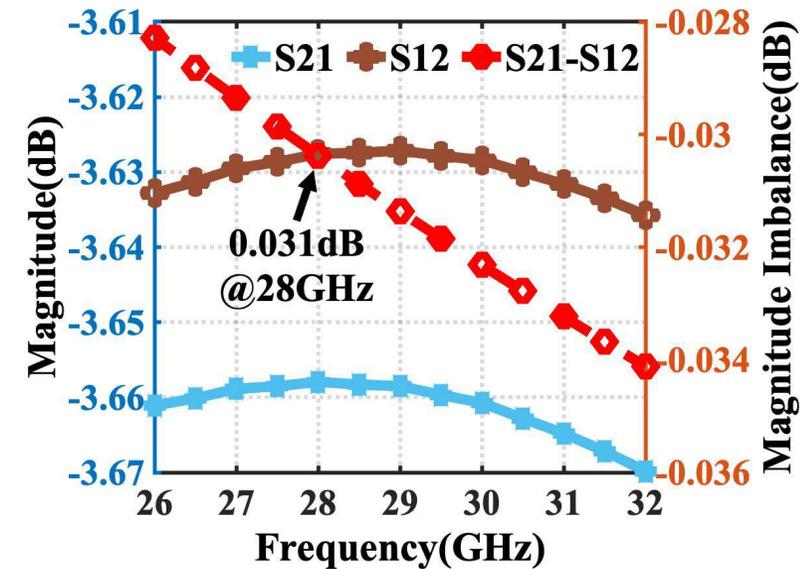
- Electromagnetic simulation from 26 to 32 GHz
 - Magnitude imbalance $<0.04\text{dB}$ and phase mismatch $<0.32^\circ$
 - Magnitude IQ mismatch $<0.7\text{dB}$ and phase IQ mismatch $<0.1^\circ$



IQ mismatch



Phase imbalance

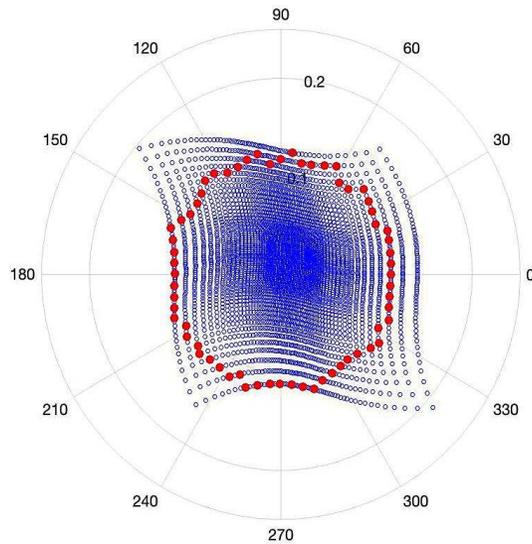


Magnitude imbalance

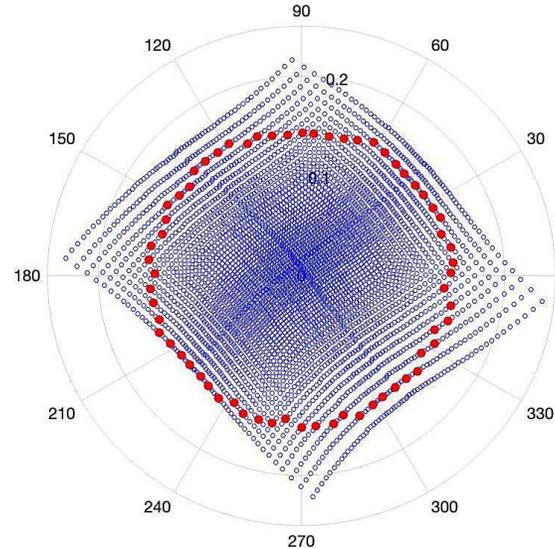
- X-type Vector Modulator
 - Controlled by 6 bit digital code for I/Q path
 - Code selection algorithm for constellation diagram

Width $8 \times (2^0, 2^1, 2^2, 2^3, 2^4, 2^5) \mu\text{m}$
Length 40nm

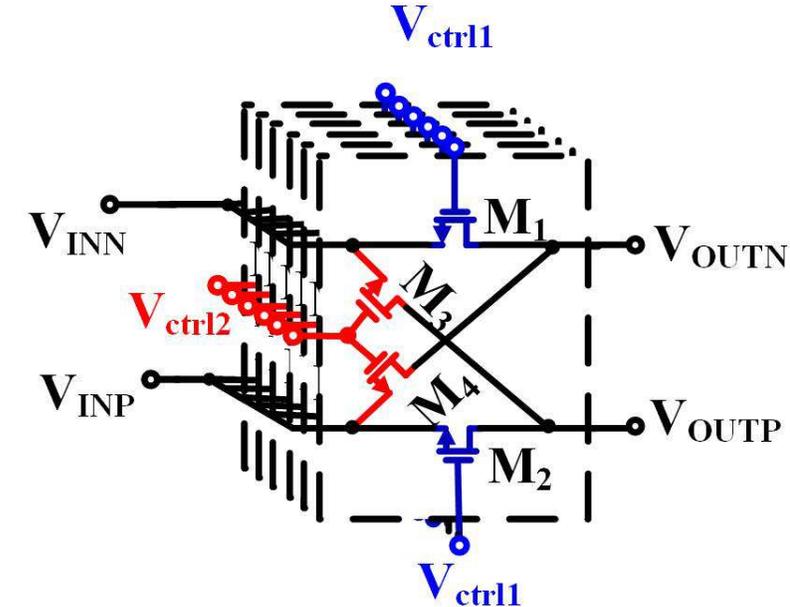
Deformity Correction



Before Deformity Correction



After Deformity Correction



Schematic of X-type Vector Modulator

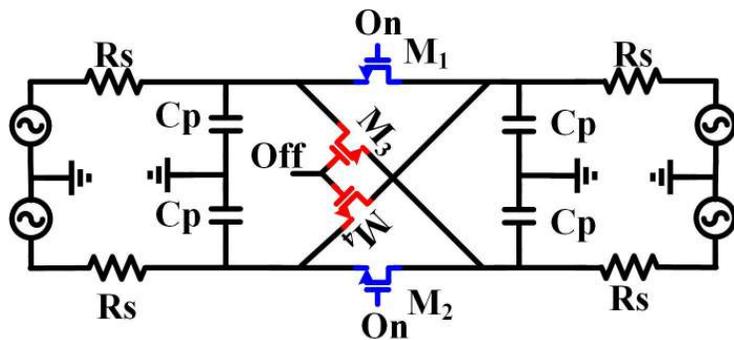
- Linearity Optimization Technology

- Distortion induced **Ron modulation model** analysis:

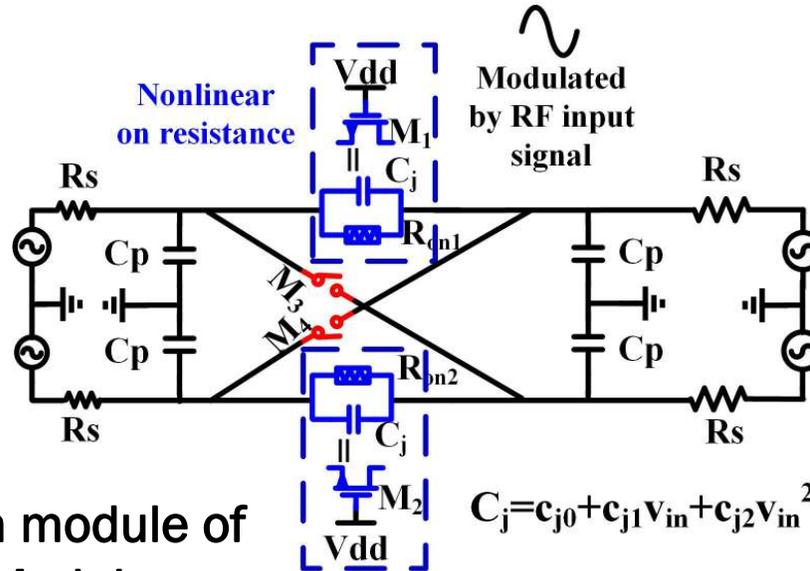
$$IM_3 = HD_3 = \left[\frac{n^2 (C_p + c_{j0})}{\beta V_{ov}^3} + \frac{nc_{j1}}{\beta V_{ov}} + c_{j2} \left(R_s + \frac{1}{\beta V_{ov}} \right) \right] \frac{\omega_0 A_0^2}{4} \approx \frac{1}{4} \left(\frac{nA_0}{V_{ov}} \right)^2 R_{on} C_p \omega_0$$

$$2(IP1\text{ dB (dBm)} + 9.6\text{ dBm}) \approx 3Pin\text{ (dBm)} - IM_3\text{ (dBm)}$$

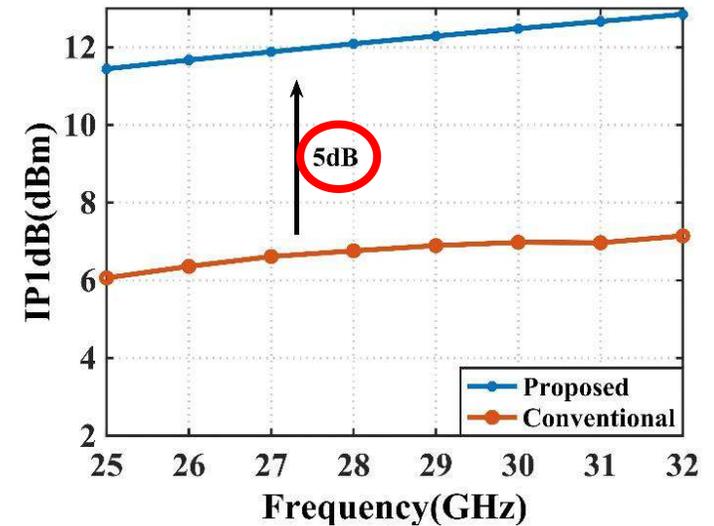
- Simulated X-type Vector Modulator IP1dB: **>11.2dB@28GHz**



Ron modulation module of X-type Vector Modulator



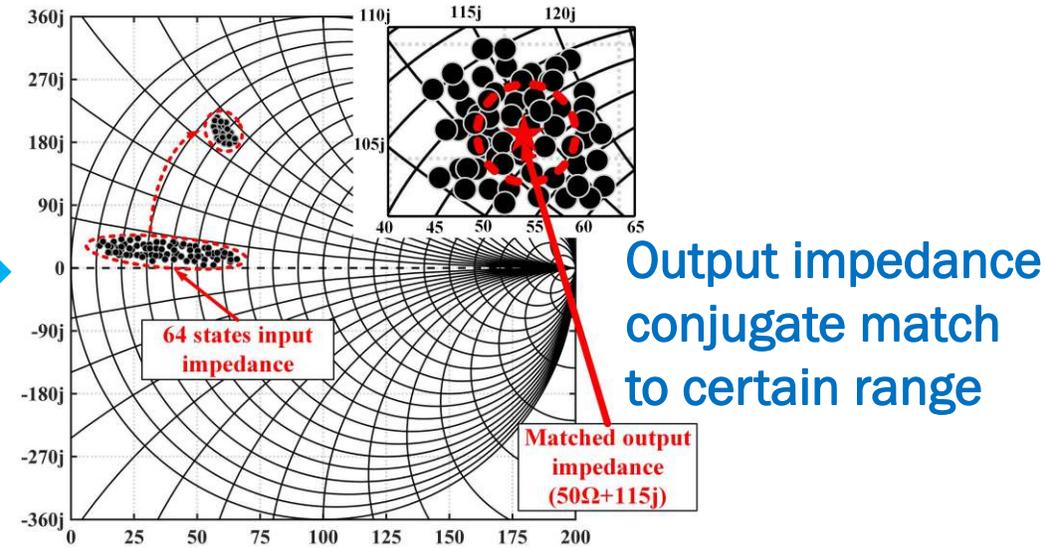
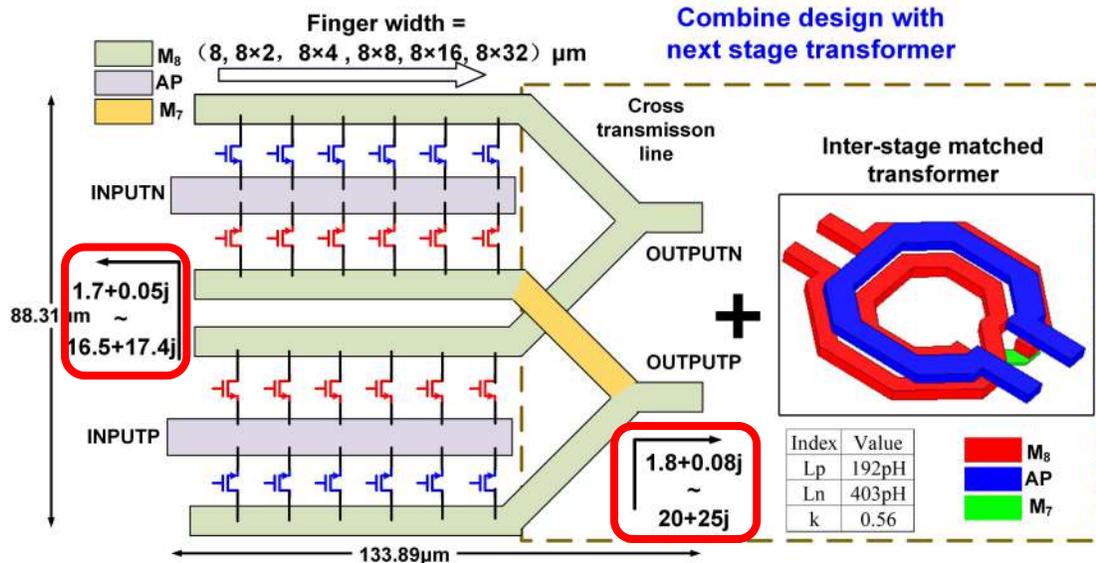
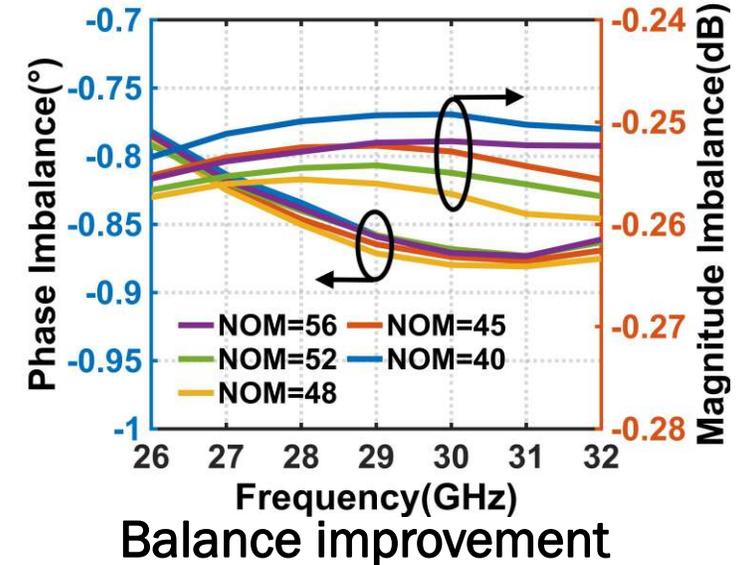
$$C_j = c_{j0} + c_{j1}V_{in} + c_{j2}V_{in}^2$$



Linearity Improvement

Passive Vector Modulator

- Multi-state Inter-stage Matching Technology
 - Code-dependent Input/Output impedance of X-type Vector Modulator
 - Conjugate Matching 54 states of selected 64 for phase and magnitude balance

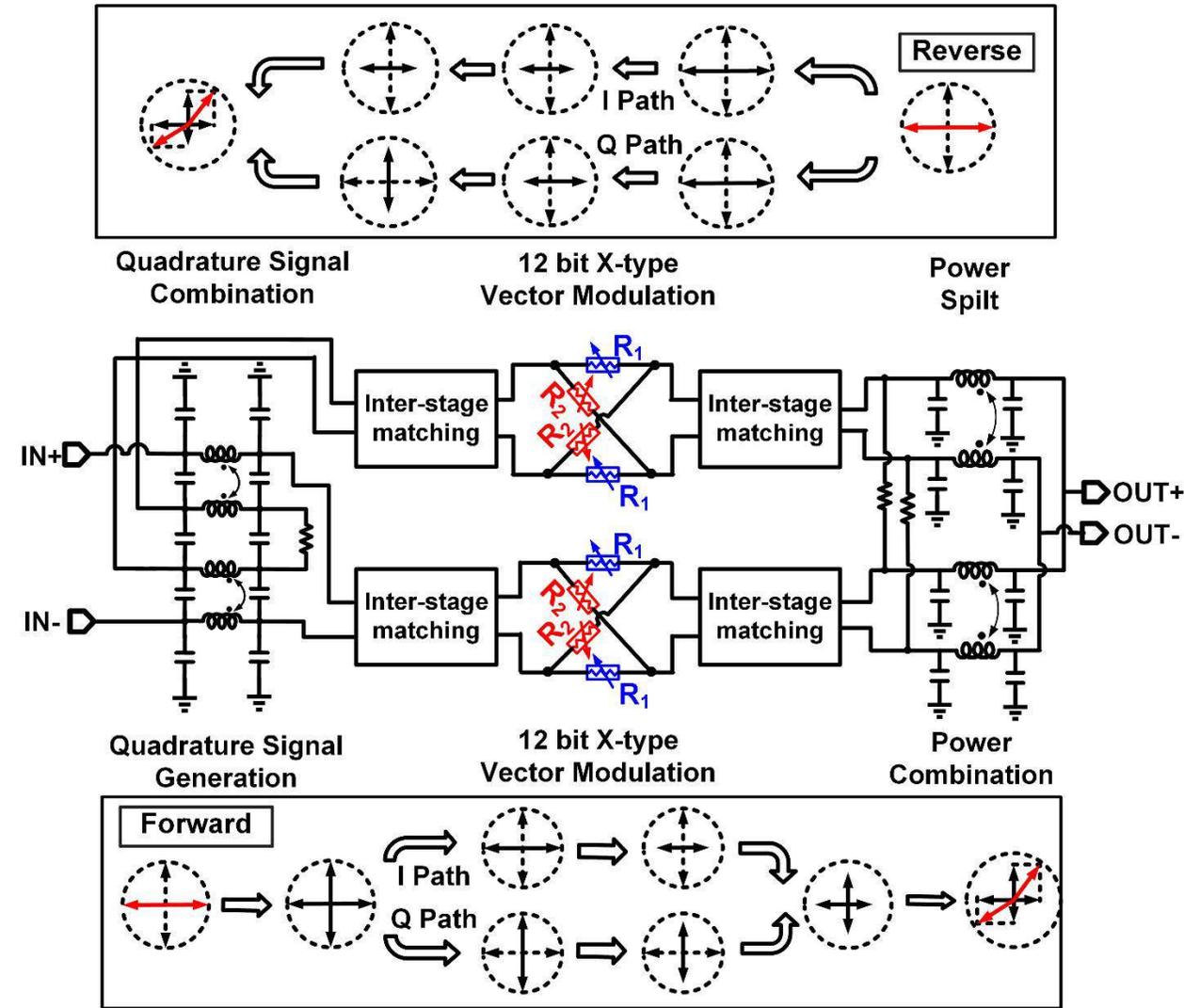


- Condition to minimize the phase/magnitude imbalance :

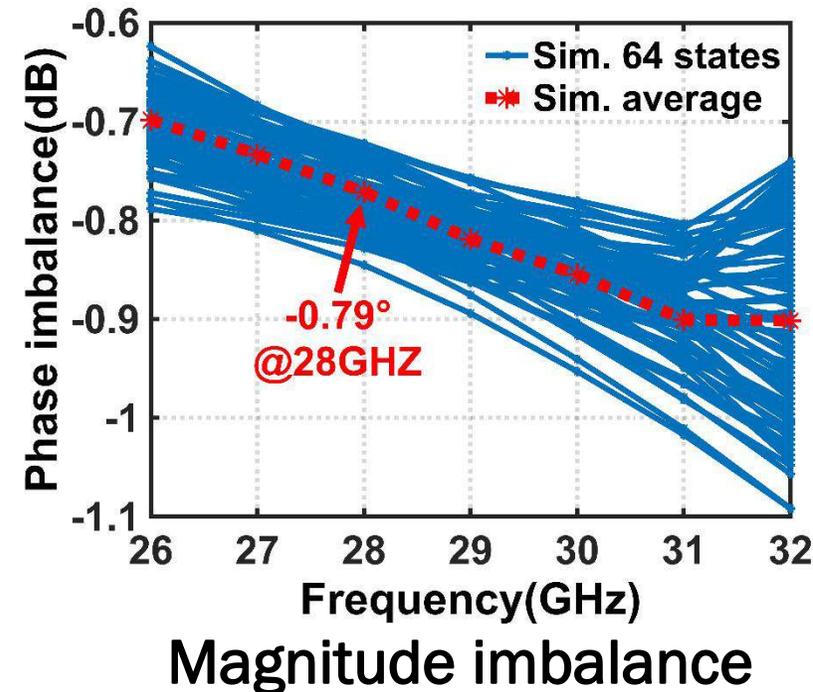
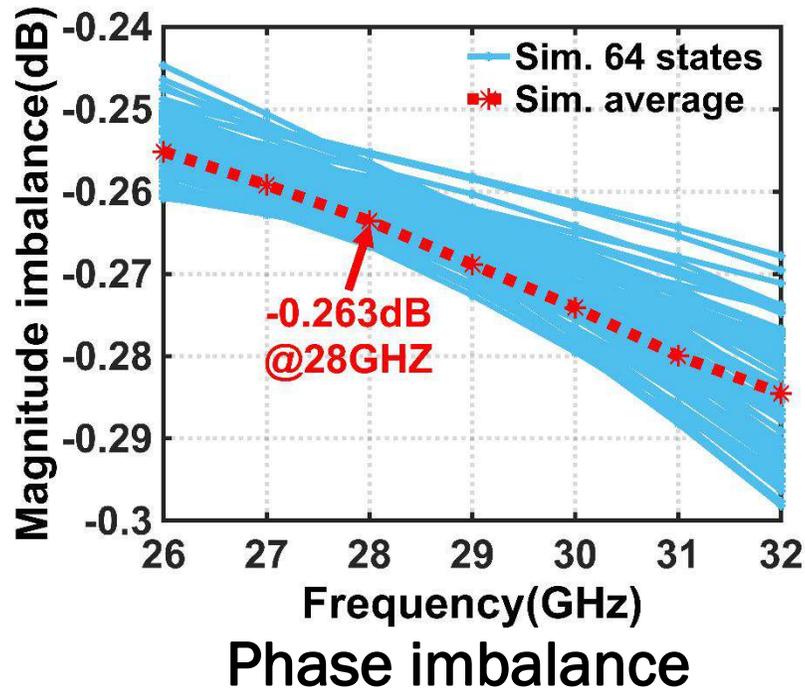
$$-R_1 R_2 = Z_0^2$$

$$-R_1 - R_2 = 0$$

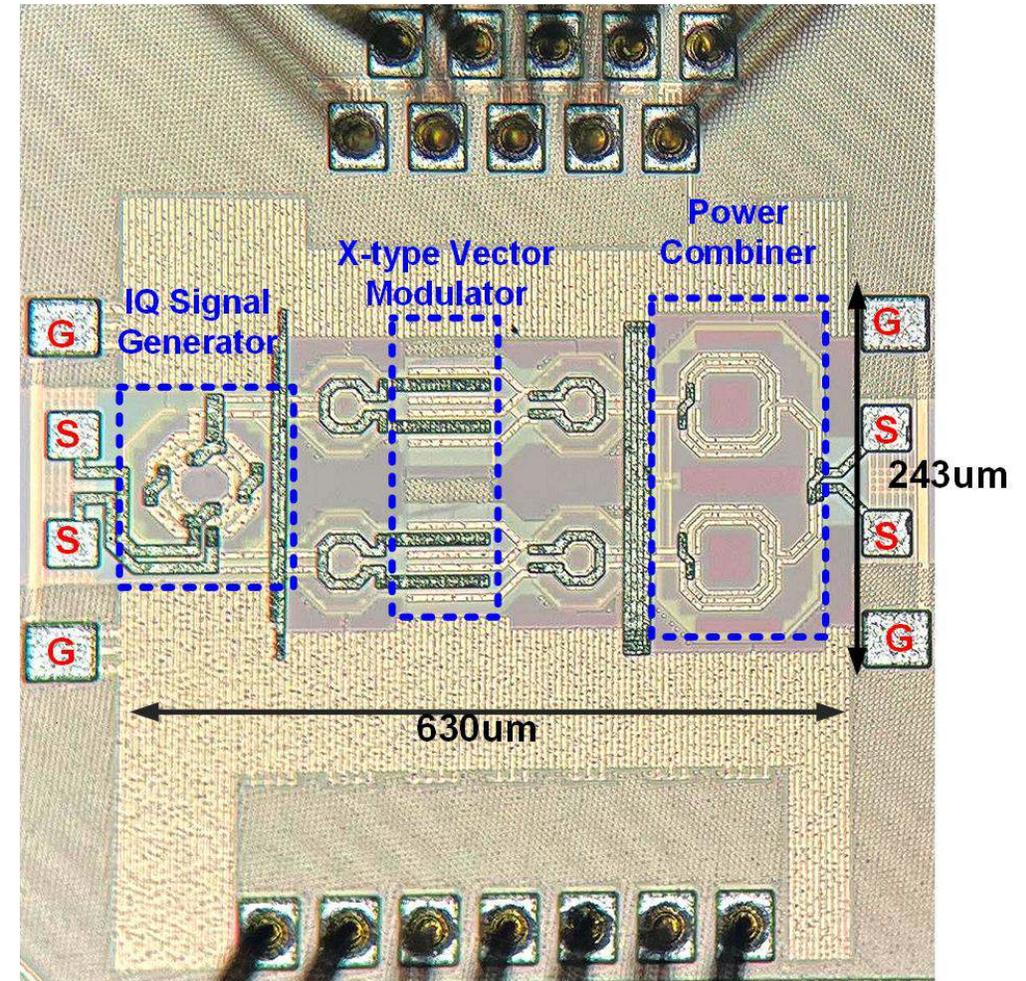
(R_1/R_2 : Tunable resistance of transistors, $Z_0=50\Omega$)



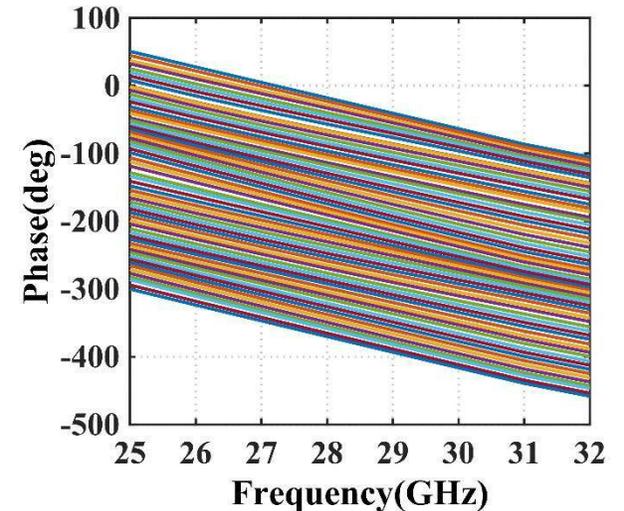
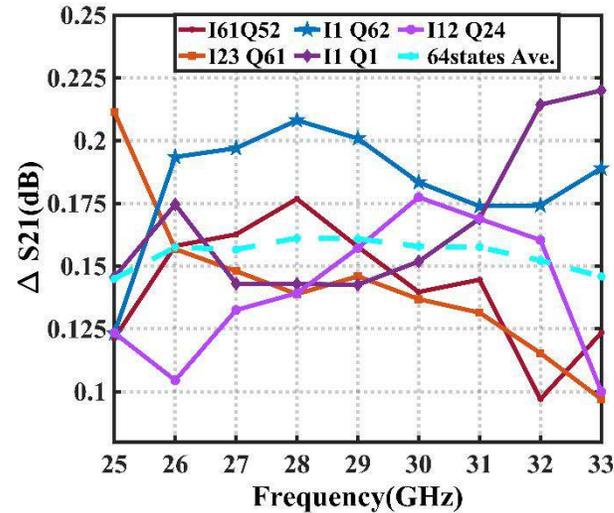
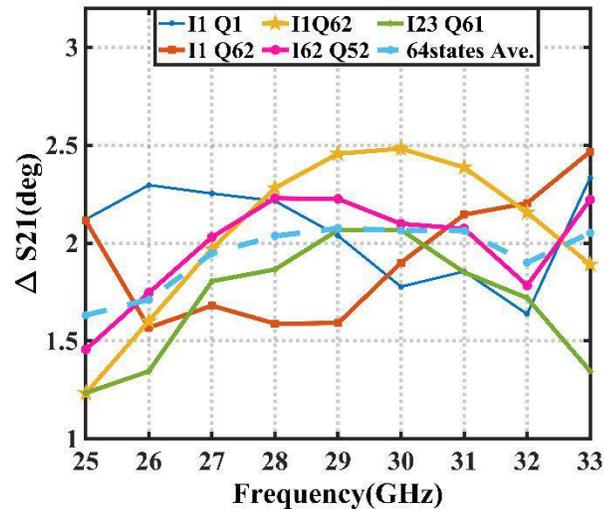
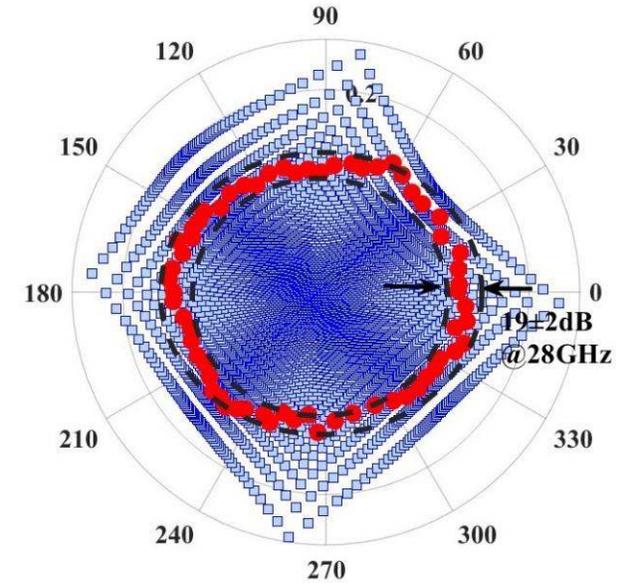
- Electromagnetic simulation from 26 to 32 GHz
 - Simulated PS magnitude imbalance: $<0.265\text{dB @}28\text{GHz}$
 - Simulated PS phase mismatch: $<0.8^\circ @28\text{GHz}$



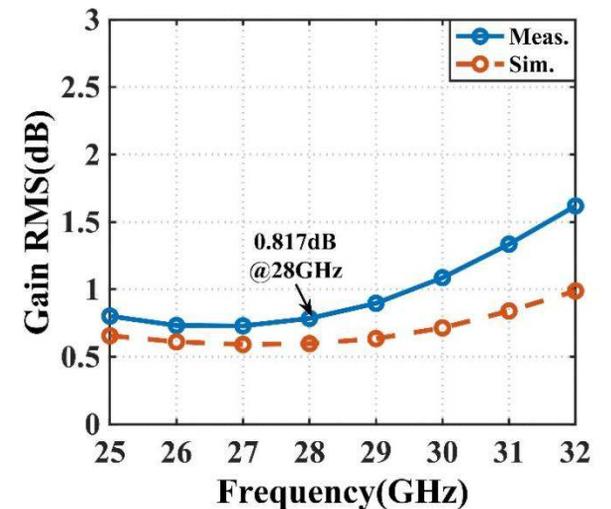
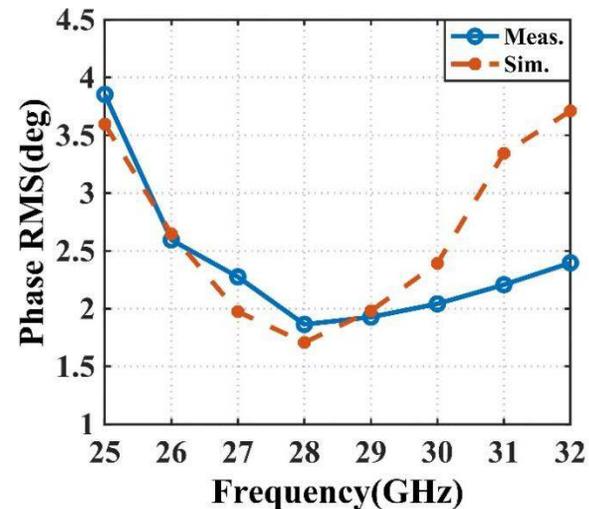
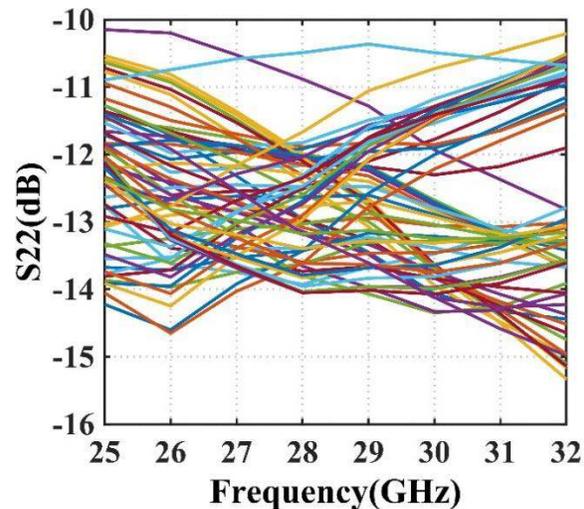
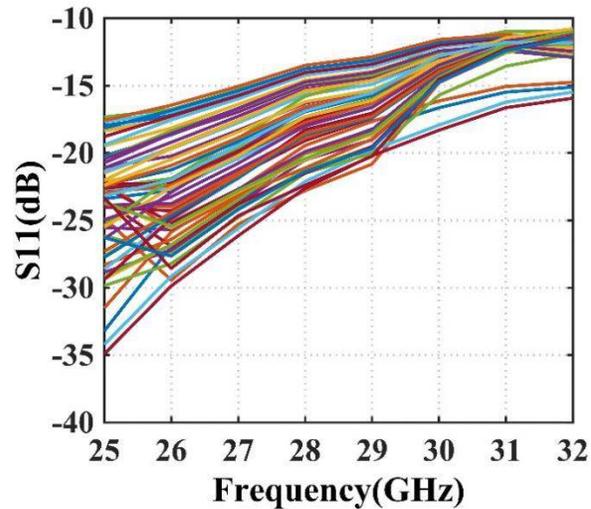
- Chip photo
- Die size
 - $0.63 \times 0.243 \text{ mm}^2$ (core)
 - $0.72 \times 0.25 \text{ mm}^2$ (including pad)
- Test Method
 - Keysight N53478 PNA-X Network Analyzer after standard SOLT calibration



- Phase shift range and step: 360° , 5.625°
- Bidirectional imbalance:
 - Average phase imbalance: $<2.1^\circ$
 - Average magnitude imbalance: $<0.16\text{dB}$



- Input/Output Reflection Loss: $<-10.5\text{dB}$
- RMS phase error $< 2.6^\circ$ and gain error $< 1.2\text{dB}$



Performance Comparison

	TCAS-I'21	TMTT'19	TMTT'17	JSSC'07	TSCA-II'19	TSCA-I'21	TMTT'13	TCAS-I'22	This work
Process	0.25 μ m BiCMOS	65nm CMOS	65nm FD-SOI	0.18 μ m CMOS	45nm CMOS	40nm SOI	0.18 μ m BiCMOS	65nm SOI	40nm CMOS
Topology	STPS	RTPS	RTPS	AVMPS	AVMPS	PVMPS	PVMPS	PVMPS	PVMPS
Working Mode	Unilateral	Unilateral	Unilateral	Unilateral	Unilateral	Bidirectional	Bidirectional	Bidirectional	Bidirectional
Frequency(GHz)	25.5~33	29	28	15~26	27~33	70~90	45~35	32~40	26~32
Phase resolution($^{\circ}$)	5.6	Const	11.25	11.25	5	5.625	22.5	2.8	5.625
IP1dB (dBm)	NA	NA	NA	-0.8 \pm -1.1	2.2	NA	-6.25	10.2~13.5	\geq 14.5
Insertion Loss (dB)	-8.3 \pm 0.55	-8.3 \pm 0.2	NA	-4.6~-3	-5.8	-15.1	-13.5~-5	-16.9~-18.1	-19
RMS Gain Error (dB)	<0.6	NA	NA	1.1~2.1	NA	<1.3	1~2.2	0.2~0.36	<1.2
RMS Phase. Error($^{\circ}$)	<3	NA	0.3	6.5~13	0.5~0.8	<2.4	4.1~13	0.45~1.6	1.8~2.6
Chip Area(mm ²)	0.1	0.076	0.16	40.45	0.27	0.15	0.19	0.14	0.15

- **Passive symmetric design for bidirectional operating mode**
- **Linearity improvement of X-type Vector Modulator enabling by quantitative analysis of distortion**
- **Method to minimize I/Q imbalance across Multi-state transformer-based inter-stage matching**

Acknowledge

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