Tu3D-5

Design of Highly-Efficient Dual-Band GaN HEMT Power Amplifier With Dual-Class E/F-1 Operation

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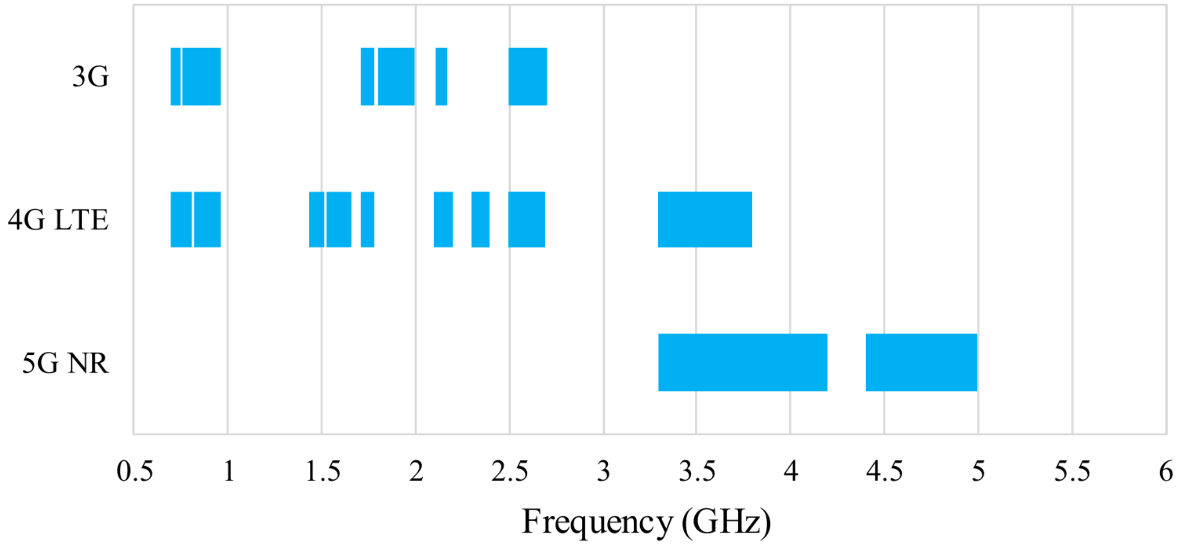
Outline

- Motivation
- Proposed Structure and Design
- Verification Results
- Conclusion

Motivation

- Wireless communication spectra – the sub-6 GHz
  - scattering widely, best compromise between capacity and coverage



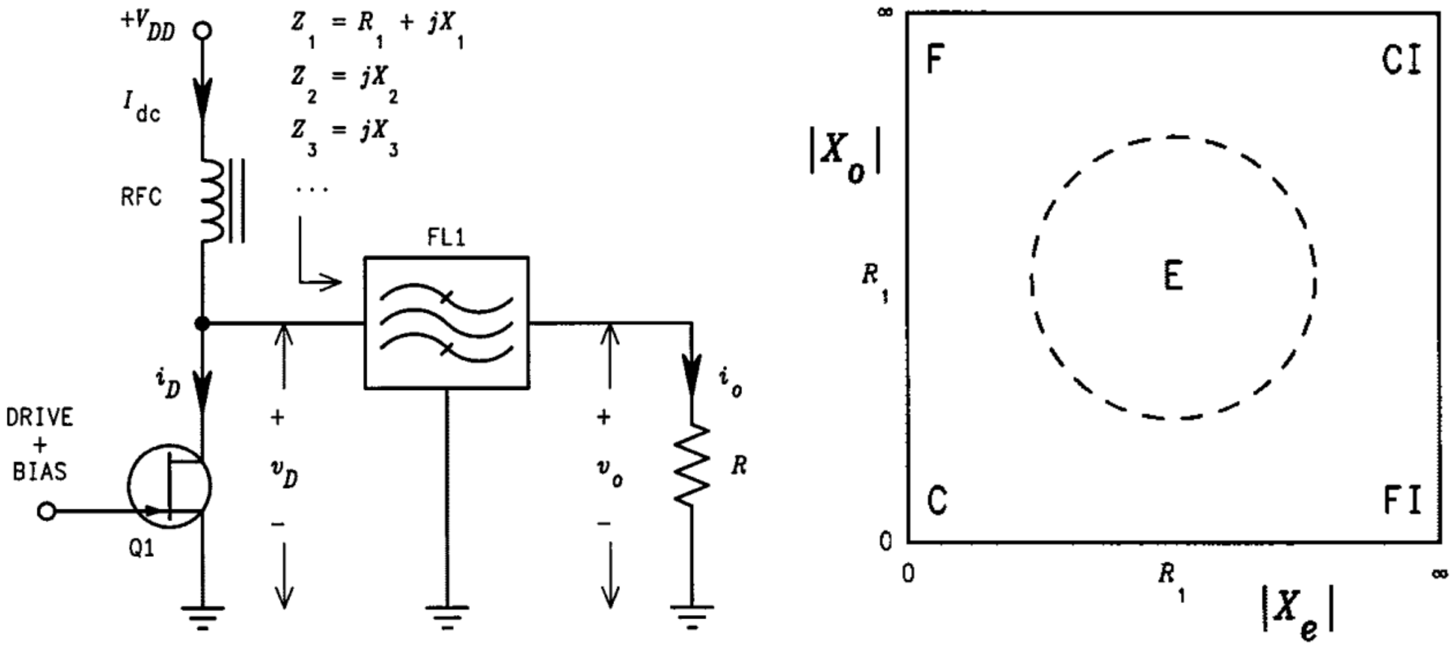
Sub-6-GHz frequency bands for 3G, 4G LTE, and 5G NR [1]

- Multi-band mode for RF transmitters
  - reconfigurable and highly-integrated solution, low cost.

Motivation

- RF Power Amplifier (PA)– the sub-6 GHz
  - most expensive, challenging
  - performance matrices: drain efficiency (DE), power-added efficiency (PAE), output power, linearity, and size
  - high DE/PAE: priority in design
- High-PAE PA
  - switch-mode PAs: class D, class E
  - harmonic-tuned PAs: class J, class F/inverse class F (class F-1)

Motivation



X_o: odd harmonic reactance
X_e: even harmonic reactance

Generic PA structure and class theoretical classification based on harmonic impedance [2]

- Class F/F-1: even/odd harmonics are low, odd/even harmonics are high
- Class E: all harmonic reactances are comparable in magnitude to the fundamental-frequency load resistance

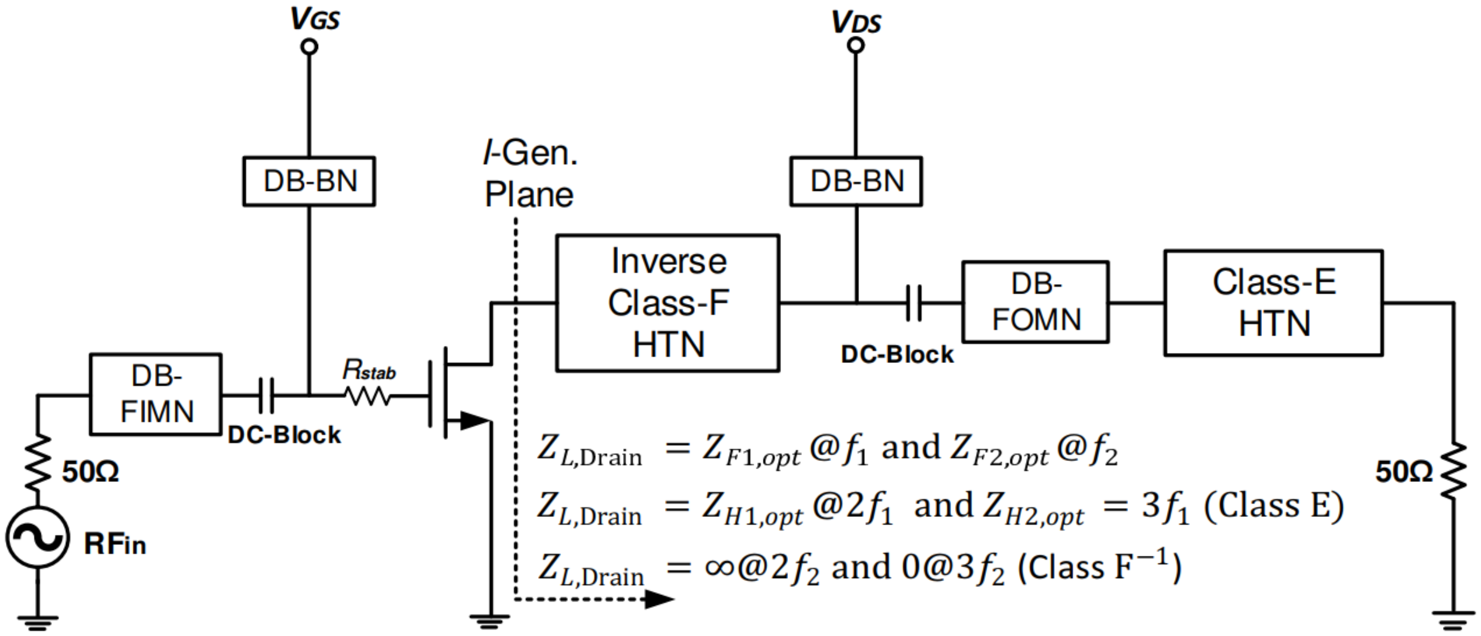
Motivation

- Comparison between class E and class F/F-1 modes [3]

Class E	Class F/F-1
High Efficiency (up to 100%)	High Efficiency (up to 100 %)
Harmonic requirements are more forgiving→ simple load network	Harmonic requirements are more rigorous→ complicated load network
Subject to operating frequency limitation	No operating frequency limitation

- Dual-band (DB) operation: class-E for low band, class F-1 for high band→ high PAE and uncomplicated design.

Proposed Structure and Design

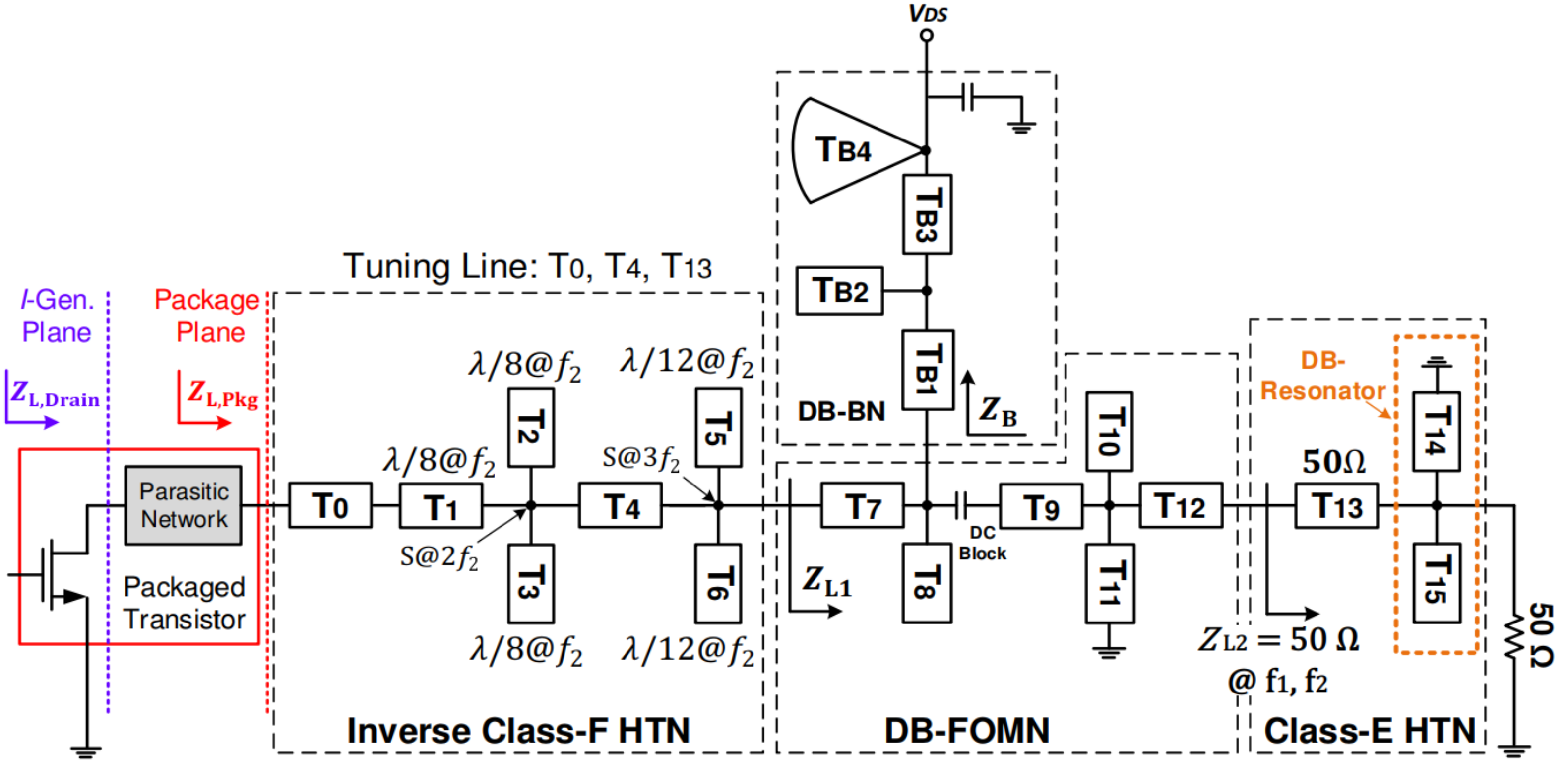


Proposed structure for dual-class E/F-1 operation

- ✓ HTN: Harmonic Termination Network
- ✓ DB: Dual-band
- ✓ FOMN: Fundamental Output Matching Network
- ✓ FIMN: Fundamental Input Matching Network
- ✓ DB-BN: Dual-Band Biasing Network

- Harmonic Control: Inverse class F HTN, class-E HTN.
- Fundamental Matching: DB-FOMN, DB-FIMN
- DC Biasing: DB-BN

Proposed Structure and Design



Detail load structure for dual-class E/F-1 operation

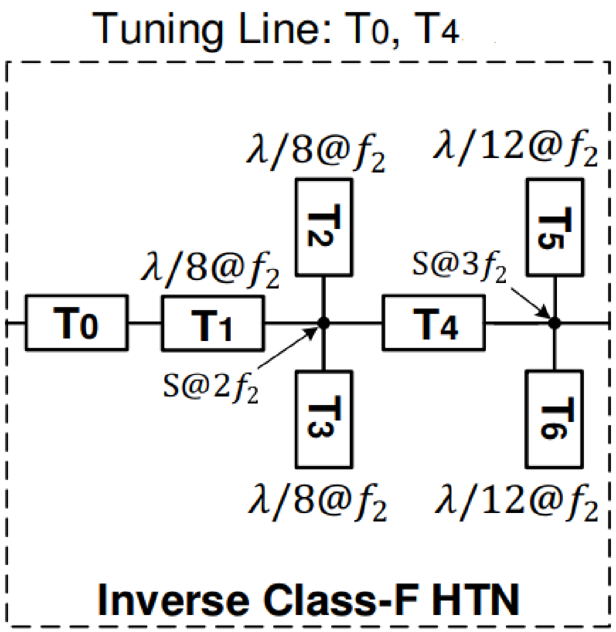
- Implementation based on transmission lines
- Active device: packaged transistor

Proposed Structure and Design

- Inverse class F HTN
  - open circuit for $2f_2$, short circuit for $3f_2$ at *I*-Gen plane
  - considering effects of parasitic network, isolated with others
- DB-FOMN: -- DB matching to 50 Ω
- DB-BN: -- shorted at DC and open at fundamental frequencies
- Class-E HTN
  - as a 50 Ω - 50 Ω transformer at the fundamentals
  - Class-E harmonic termination at f_1, does not affect to others

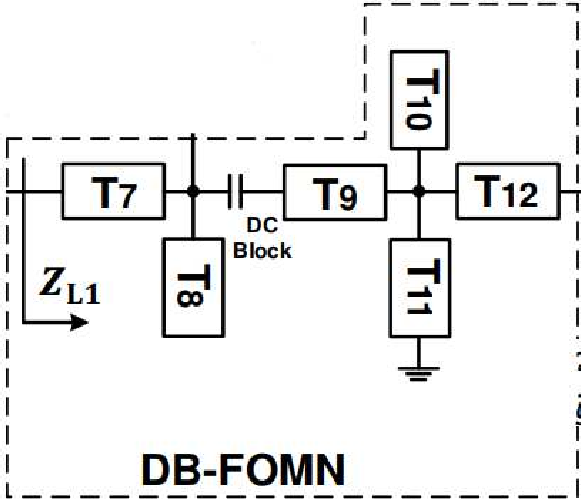
Proposed Structure and Design

- Inverse Class-F HTN [4]



  - Including two shunt stubs in each of two arms
  - Based on tuning mechanism

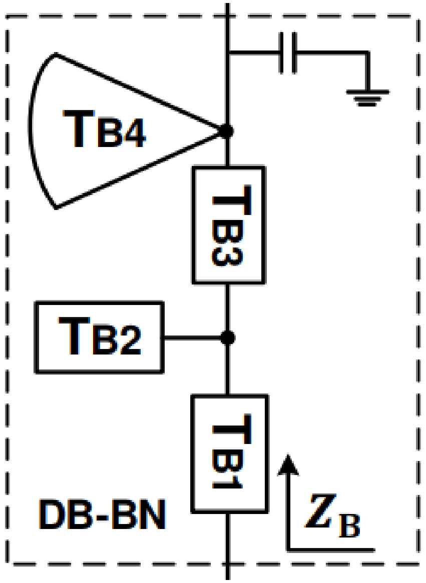
- DB-FOMN [5]



  - matching fundamental optimal impedance Z_{L1} to 50 Ω

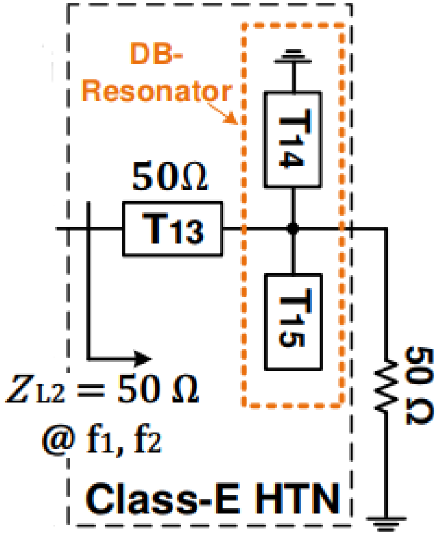
Proposed Structure and Design

- DB-BN [6]



  – Z_B: zero at DC, infinite at f_1, f_2

- Class-E HTN [5]

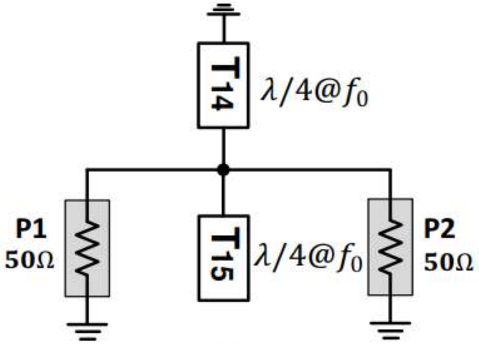


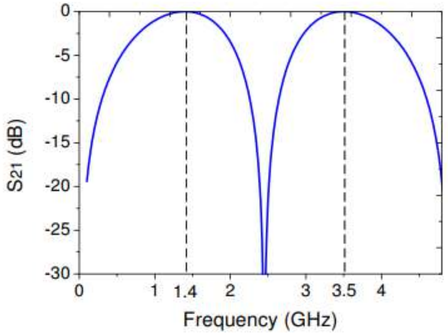
  - Including a dual-band resonator and a 50 Ω tuning transmission line

$$Z_{14} = \frac{1}{4f_0C_0}\sec^2\left(\frac{\pi}{2}\times\frac{f_2-f_1}{f_2+f_1}\right)$$

$$Z_{15} = \frac{1}{4f_0C_0}\mathrm{cosec}^2\left(\frac{\pi}{2}\times\frac{f_2-f_1}{f_2+f_1}\right),$$

  - Adding T_{13} does not influence the fundamental impedance, harmonics of f_1 are modified with its length





Proposed Structure and Design

- Design Process - Three Steps
  - Step 1: first realizing class F-1 HTN, yielding class F-1 operation at the *I*-generation plane.
  - Step 2: then designing DB-FOMN, correctly matching fundamental optimal impedance to 50 Ω. At this step, adding a DB-BN which does not affect to the matching performance.
  - Step 3: class E HTN follows the DB-FOMN, acting as a 50 Ω - 50 Ω transformer and only influencing to the harmonics of f_1.

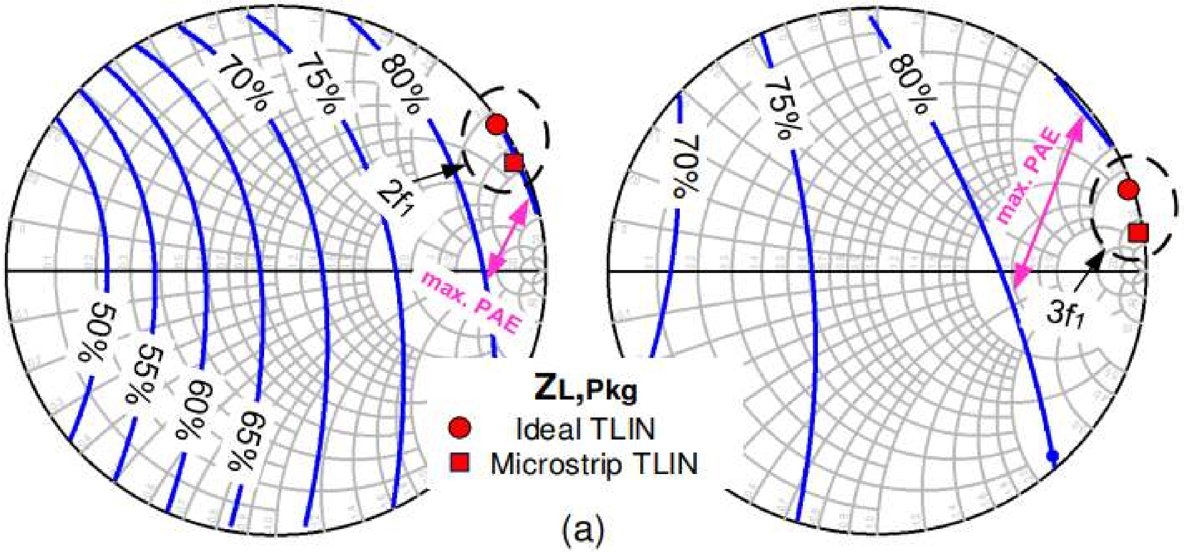
Verification Results

- Active Device: 5-W Cree transistor CGH40006P
- Operating Frequency: f_1=1.4 GHz, f_2=3.5 GHz
- Biasing Voltage: V_{GS}=−3.2 V, V_{DS}=28 V

TLIN	T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Z (Ω)	90	90	120	120	90	120	120	90	90	126.4
θ (°)	43.3	45	45	45	54.1	30	30	10	60	24.6
f (GHz)	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	1.4
TLIN	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	T_{B1}	T_{B2}	T_{B3}	T_{B4}
Z (Ω)	75.7	106.3	115.5	50	41.7	65.6	90	90	90	
θ (°)	50.2	51.2	56.4	19	90	90	90	90	86	90
f (GHz)	1.4	1.4	1.4	1.4	2.45	2.45	3.5	3.5	3.5	1.4

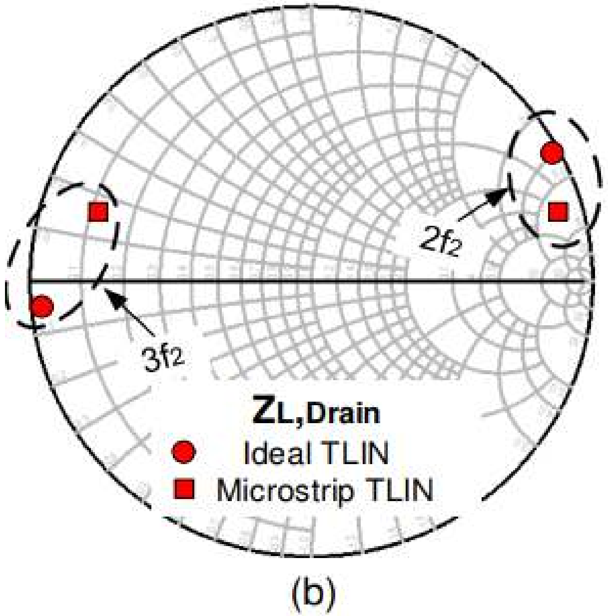
Extracted TLIN parameters for dual-class E/F-1 operation

Verification Results



Simulated PAE contours and location of $Z_{L,Pkg}$ at $2f_1$ and $3f_1$

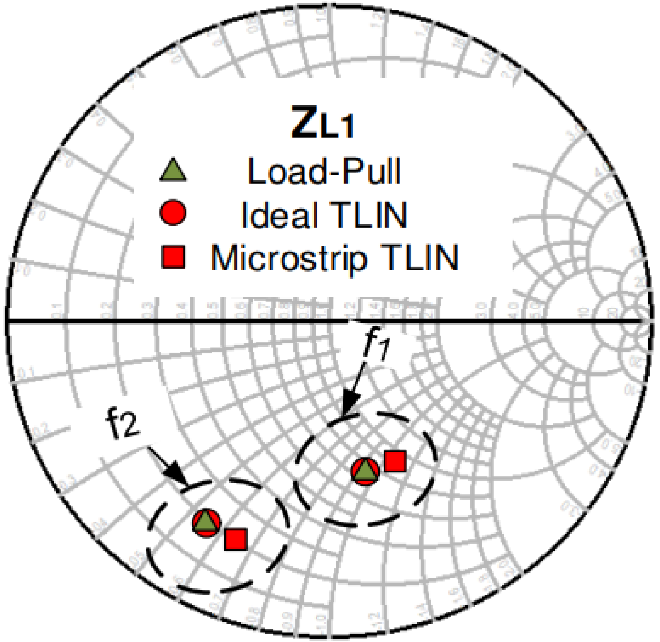
- 2nd and 3rd harmonics are located at optimal regions
- Efficient class-E operation at f_1



Simulated location of $Z_{L,Drain}$ at $2f_2$ and $3f_2$

- Second harmonic spreads near the open-circuit point while third harmonic resides close to the short-circuit region.
- Reliable class F-1 operation at f_2.

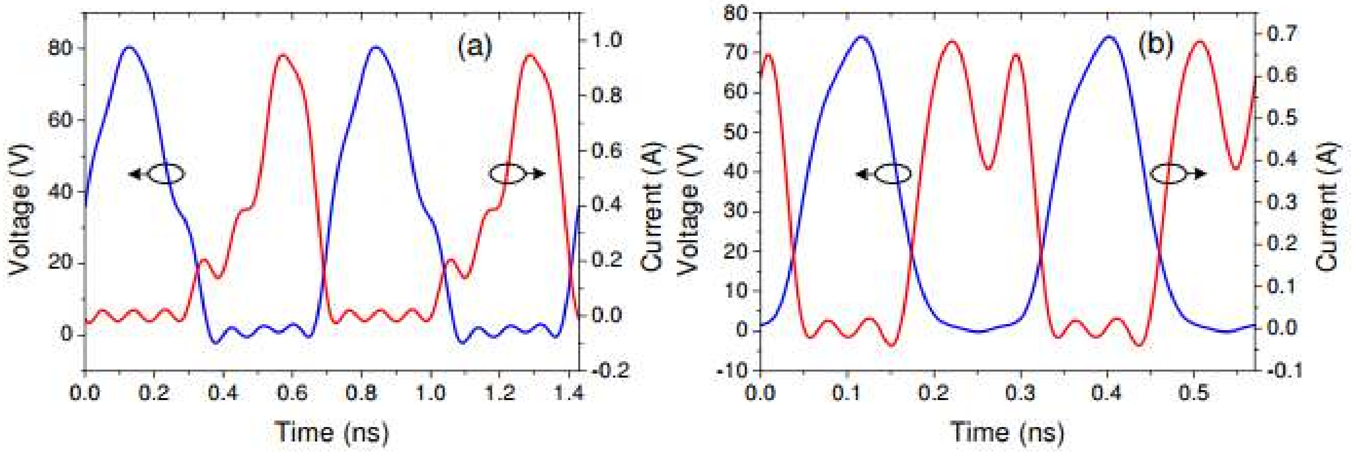
Verification Results



(c)

Simulated fundamental impedance location of Z_{L1} at f_1 and f_2

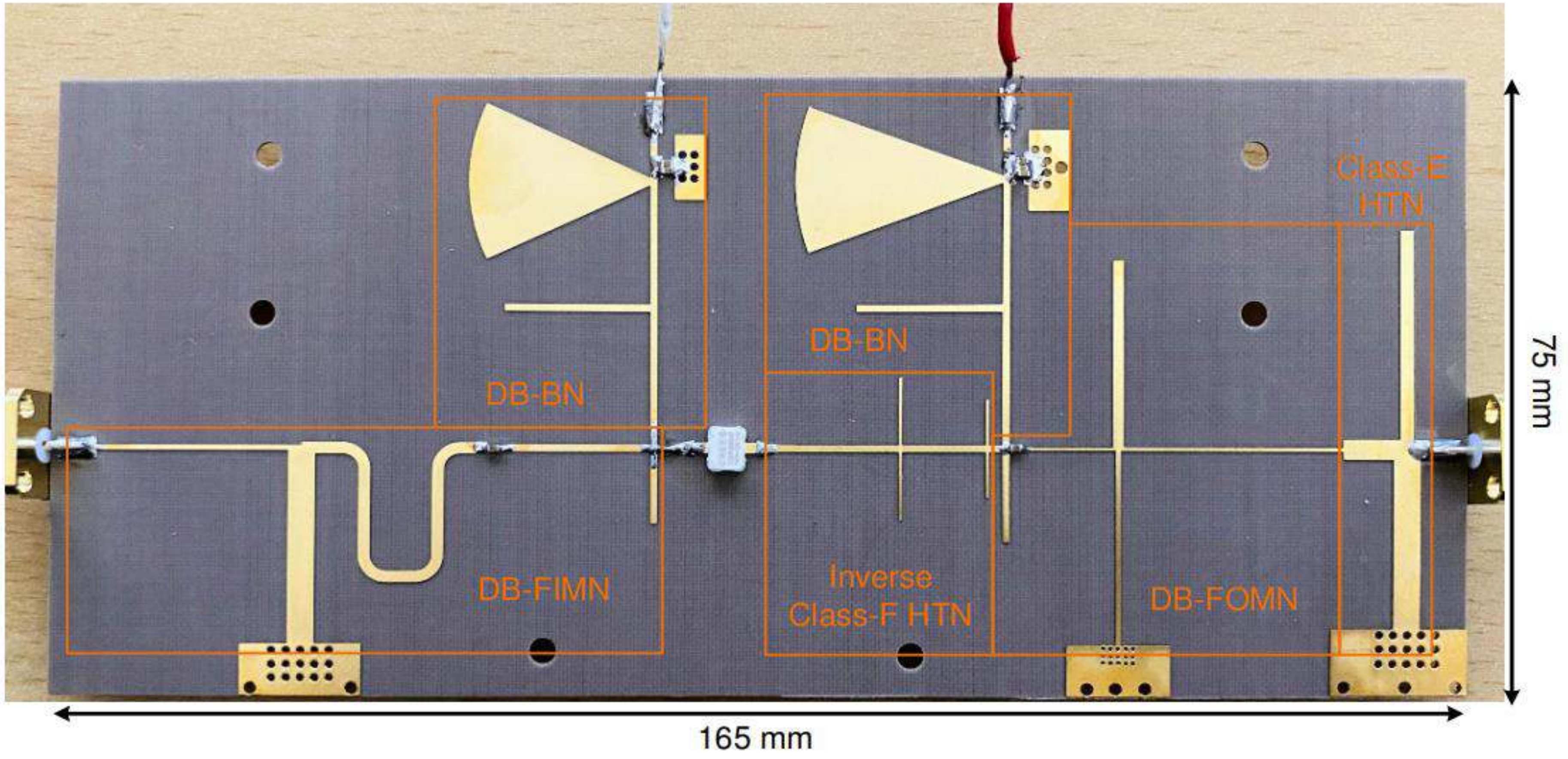
- **Good agreement between load-pull and circuit simulations.**



Simulated intrinsic drain waveforms of voltage and current at (a) f_1 and (b) f_2

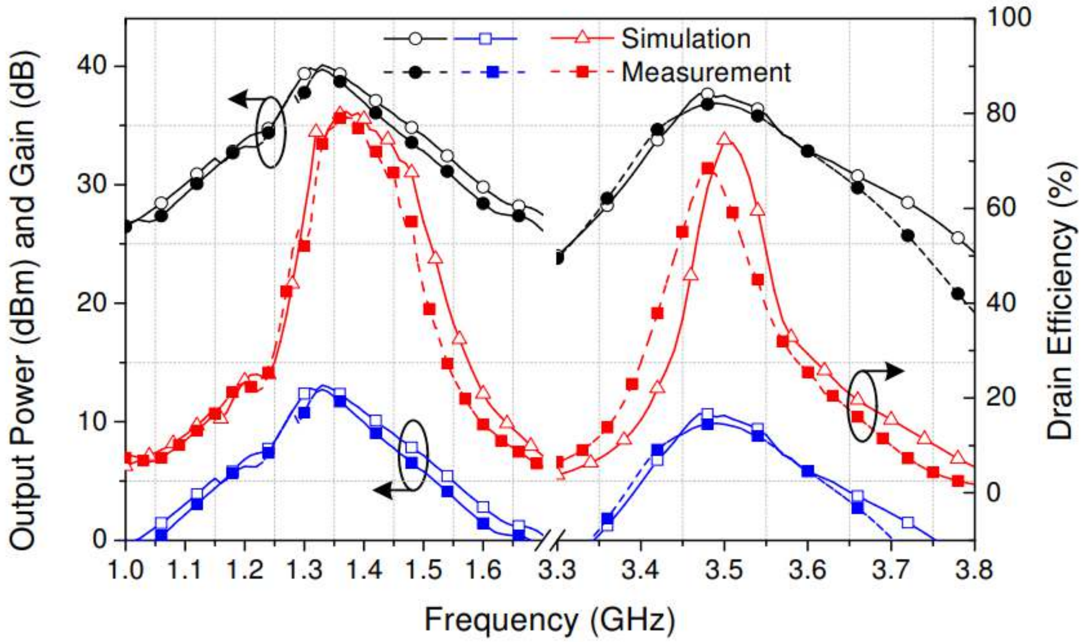
- **Class E waveforms at $\boldsymbol{f_1}$.**
- **Inverse Class F waveforms at $\boldsymbol{f_2}$.**

Verification Results

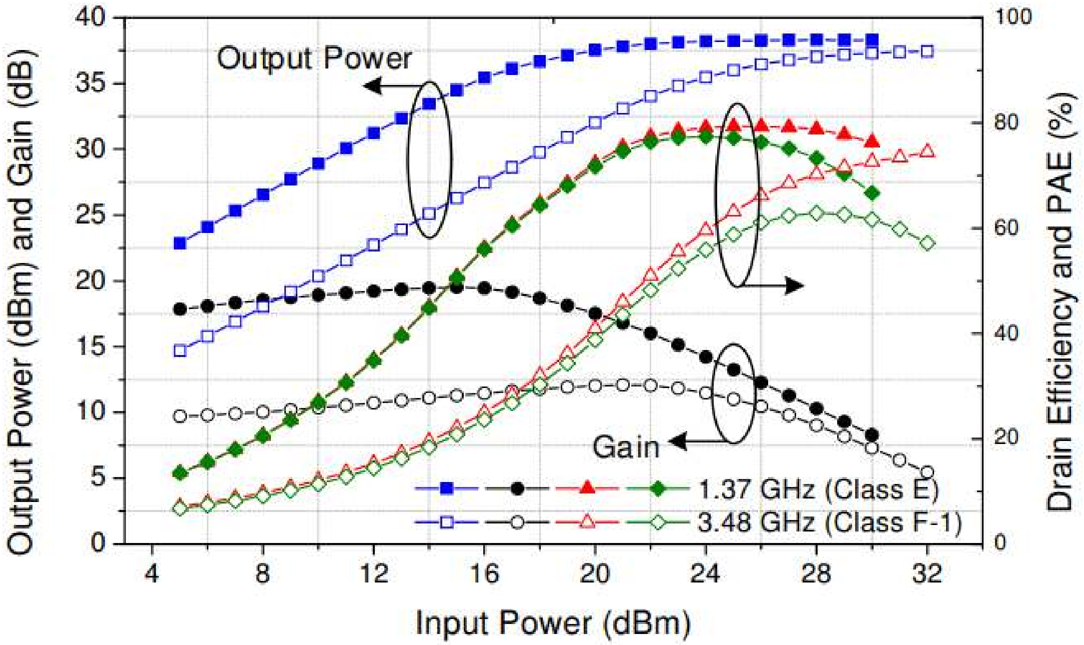


Photograph of the fabricated prototype on Taconic TLY-5 substrate ($\varepsilon_r = 2.2$ and $\tan\delta = 0.0009$)

Verification Results



Simulated and measured drain efficiency, output power, gain versus frequency at an input power of 27 dBm.



Measured efficiency, PAE, output power, gain versus input power.

- **Measured peak efficiency: 79.2% at 1.37 GHz, 68.5% at 3.48 GHz.**
- **Output Power: 38.3 dBm at 1.37 GHz, 36.8 dBm at 3.48 GHz**

- **Highest PAE: 77.4% at 24 dBm for 1.37 GHz; and 62.9% at 28 dBm for 3.48 GHz.**

Conclusion

- This work presents a high efficiency DB PA with low design complexity
  - Dual-class E/F-1 strategy: class E operation for low band and class F-1 operation for high band
  - A novel structure with its design process: realizing the dual-class E/F-1 operation
  - Verification: simulation and measurement using a packaged transistor

References

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Thank you for your attention!

Q & A