

Tu3E-1

# Low Jitter Frequency Generation for 5G mm-Wave Cellular Applications

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# Outline

- LO design challenges for 5G mmW handsets
- DTC-assisted Low-jitter PLL design
- Advanced techniques to achieve low jitter
- High performance 5G FR2 LO chain
- Summary

# Smart Phones with 5G mmW Chipset

## ■ FR2 system

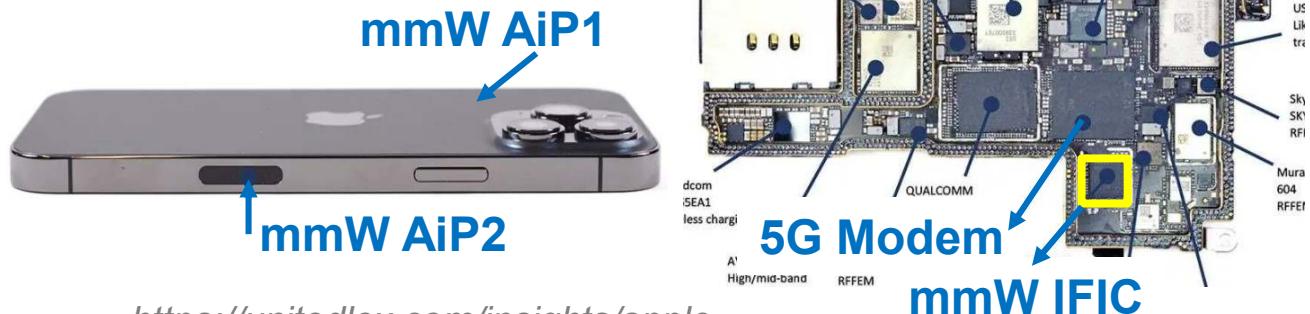
Modem + mmW IFIC + mmW AiP



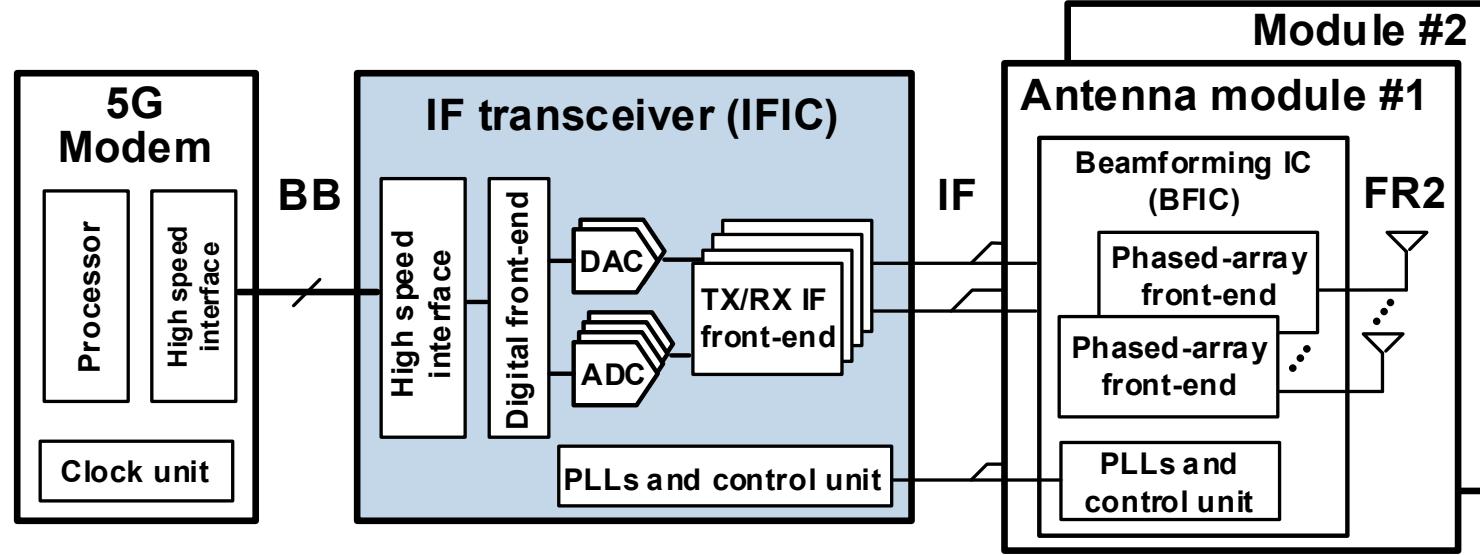
<https://www.ifixit.com/Guide/Google+Pixel+7+Pro+5G+mmWave+Antenna+Replacement/154719>



<https://www.techinsights.com/blog/muratasamsung-2nd-gen-mmwave-aip-discovered-samsung-galaxy-a53>



<https://unitedlex.com/insights/apple-iphone-13-pro-max-teardown-report/>

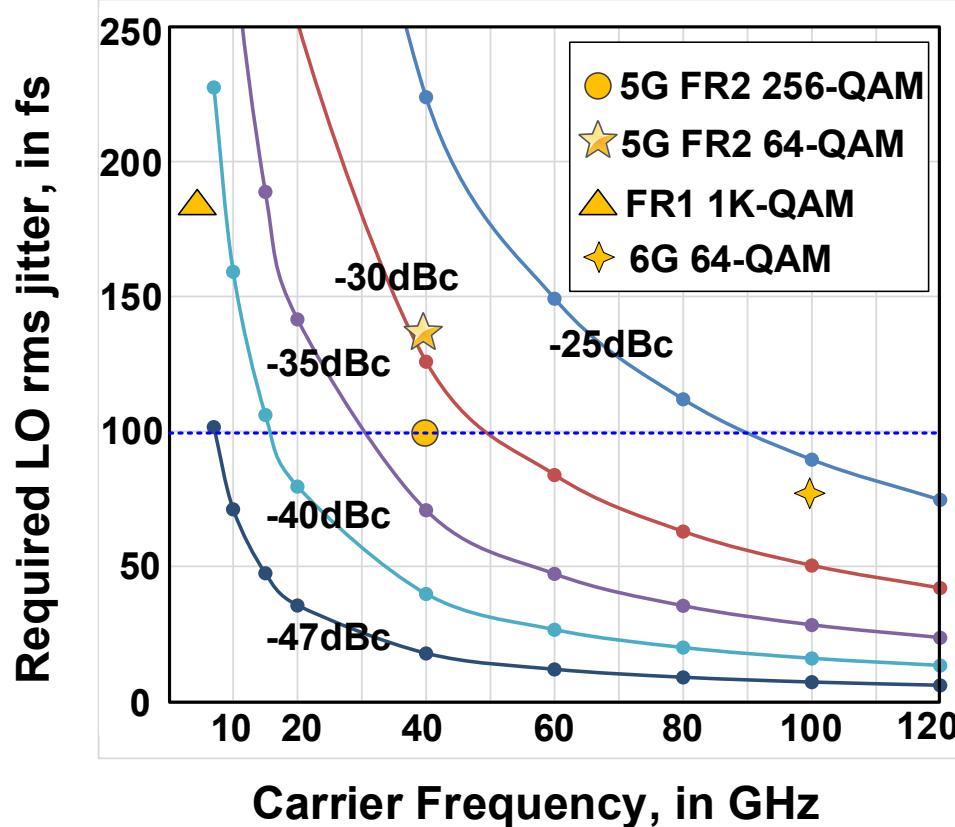


FR2 Band	Uplink/Downlink (GHz)
N257	TDD 26.5 – 29.5
N258	TDD 24.25 – 27.5
N261	TDD 27.5 – 28.35
N260	TDD 37.0 – 40.0
N259	TDD 39.5 – 43.5

LB      HB

- mmW LO circuitry on both IFIC and BFIC
- Multi-band support with low power and low cost
- 256-QAM support demands low jitter LO

# LO RMS Jitter Requirement for 5G mmW



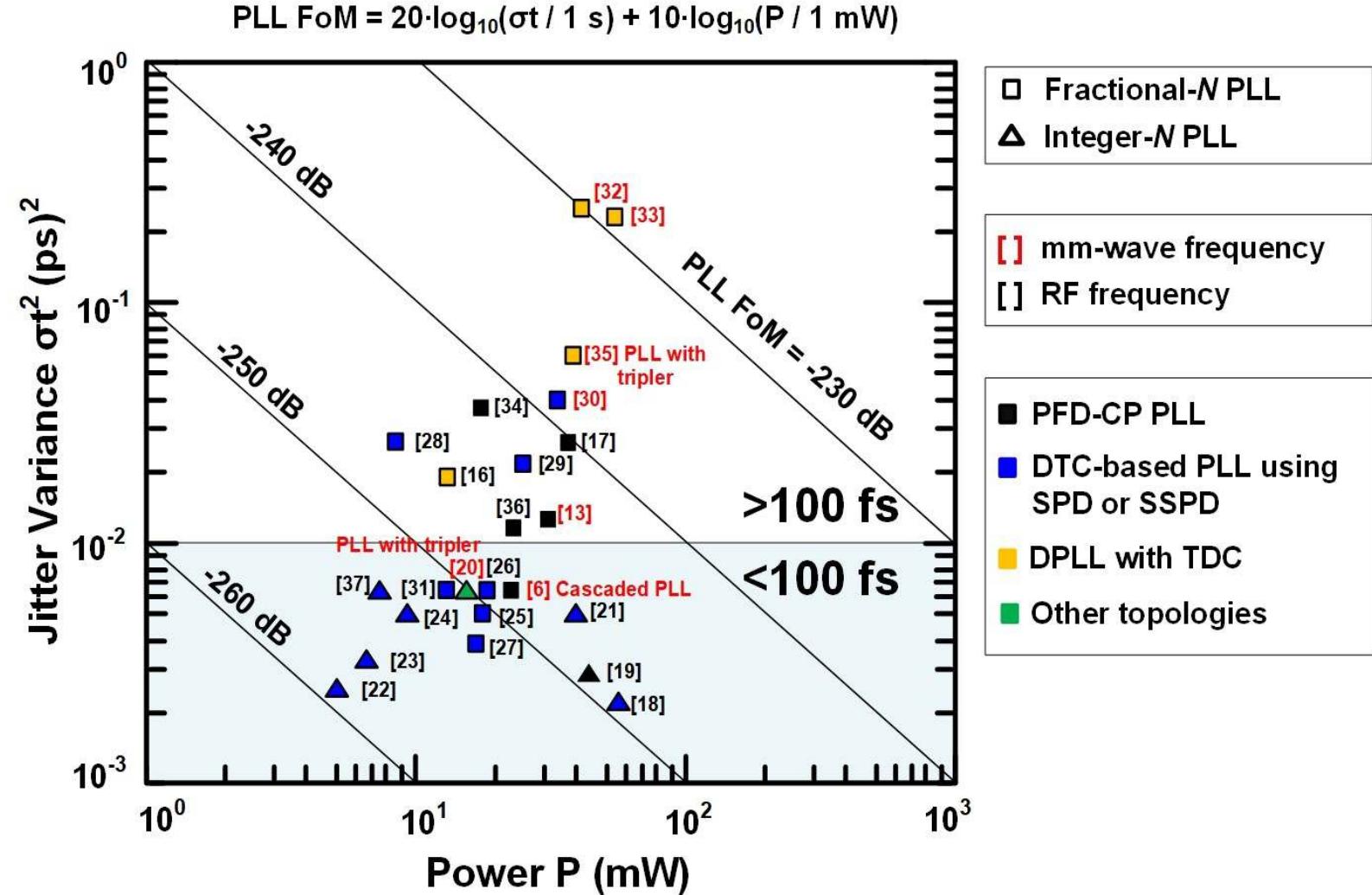
RF freq. (GHz)	Wireless applications	Modulation	EVMmax	EVMmax (dB)	Tentative LO DSB IPN Spec. (dBc)	Margin	LO rms jitter (fs)
40	5G FR2	64-QAM	6%	-24	-29	5	141
		256-QAM	4.50%	-27	-32	5	100
7	5G FR1	256-QAM, MIMO	3.00%	-30	-40	10	227
		1K-QAM, MIMO	2.00%	-34	-42	8	181
100	6G	QPSK	17.50%	-15	-23	8	111
		16-QAM	12.50%	-18	-26	8	79
		64-QAM	8%	-22	-27	5	71

$$\text{Jitter}_{\text{rms}} = \frac{\sqrt{2} \cdot 10^{\text{IPN dBc}/10}}{2\pi f_0} \leq \frac{\sqrt{10^{\text{EVM dB}/10}}}{2\pi f_0}$$

<100 fs low-jitter LO is required for 5G FR2 256-QAM  
 → Very challenging to achieve

# State-of-the-Art Low-Jitter PLLs

- Only a few frac. N PLLs achieves <100 fs
- Even harder for mmW PLLs
- PLLs with DTC-assisted PD show lower jitter, better FoM

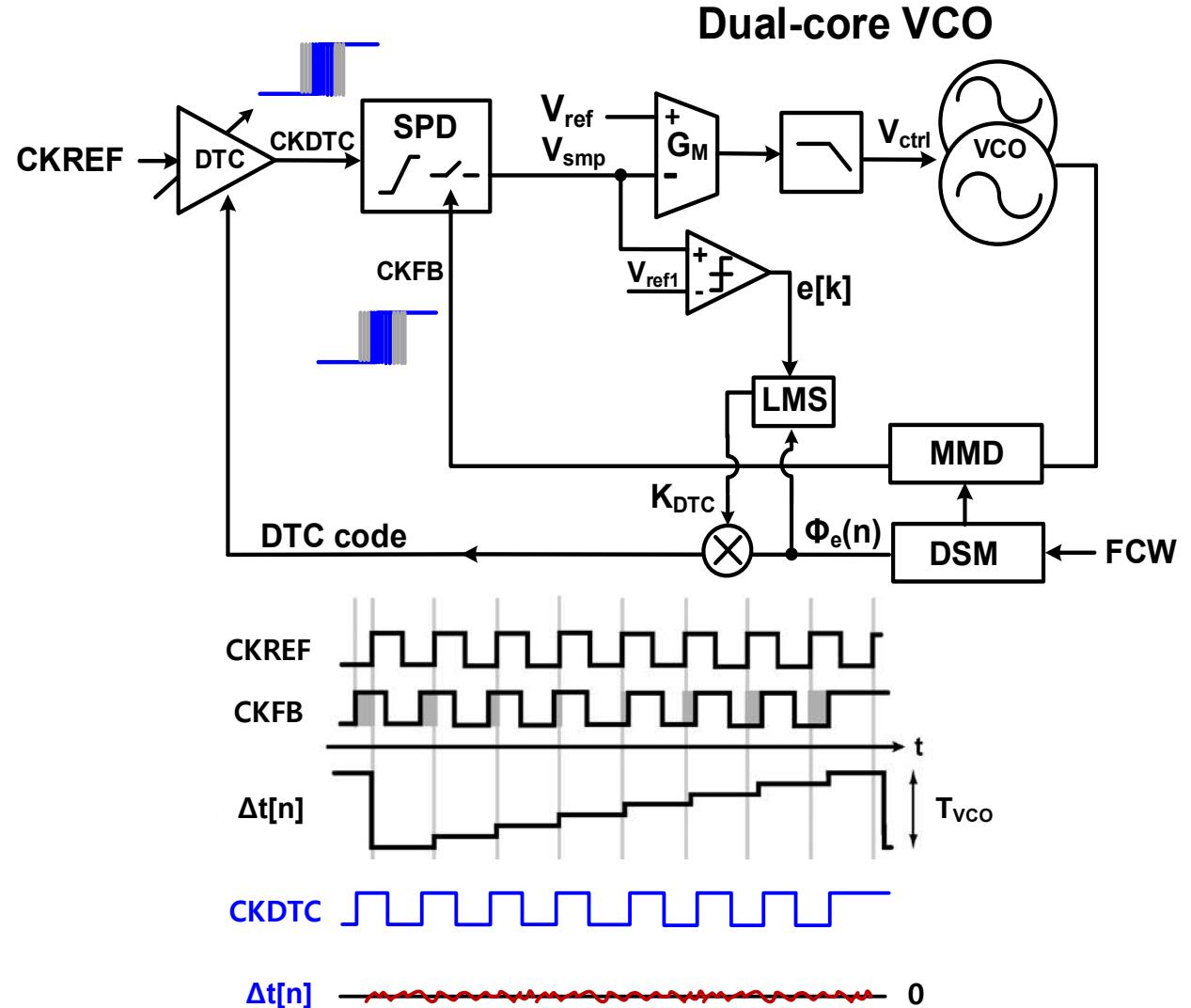


# Outline

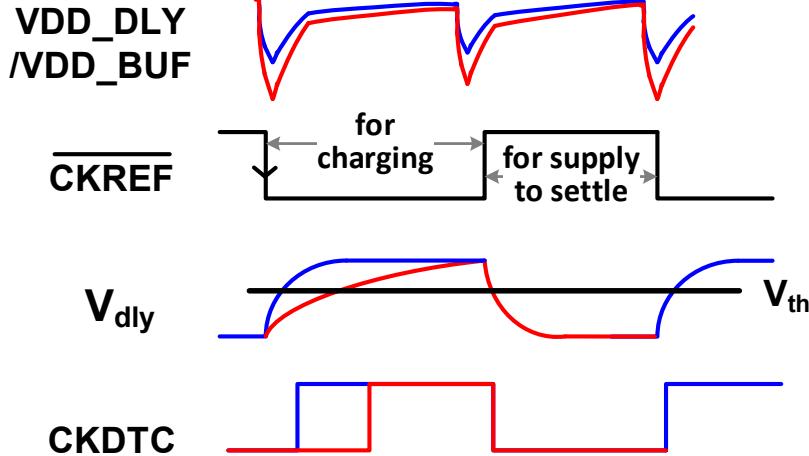
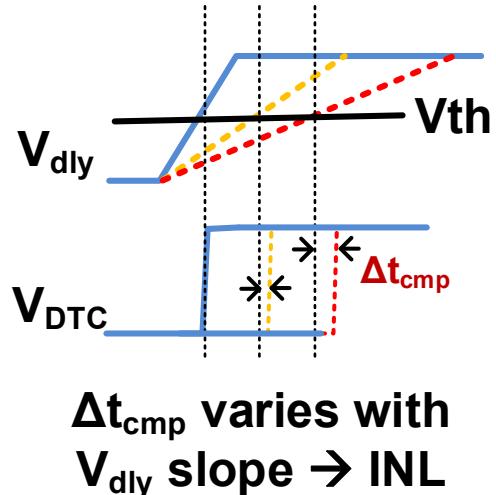
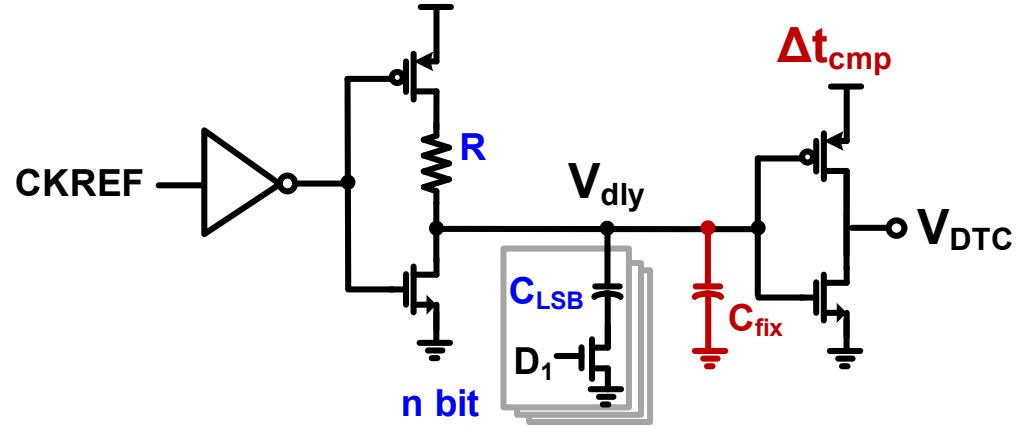
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# DTC-Based Low-Jitter Fractional-N PLL

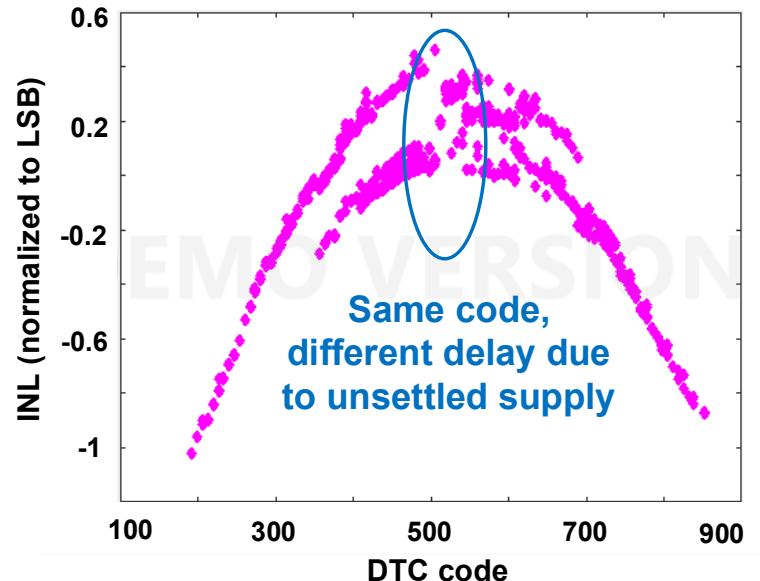
- Digital-to-time converter (DTC) cancels accum. QE on CKFB  
 → Near zero phase error at PD,  
 Just like integer-N case!
- Use high gain sampling PD  
 → Lower inband noise, high linearity, lower Pdc
- Dual-core VCO  
 → PN and power tradeoff



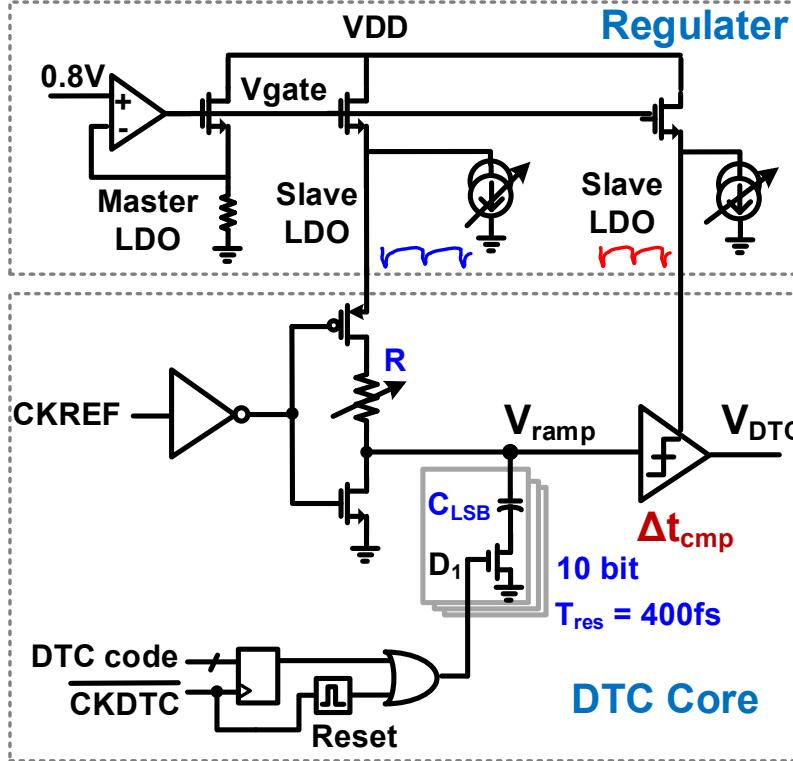
# DTC Design – Focus on Linearity



- 10 bit with fine resolution ( $\sim 400$  fs)
- Code/slope dependent propagation delay  
 $\Delta t_{cmp} \rightarrow$  static NL
- Code-dependent supply settling error  $\rightarrow$  dynamic NL

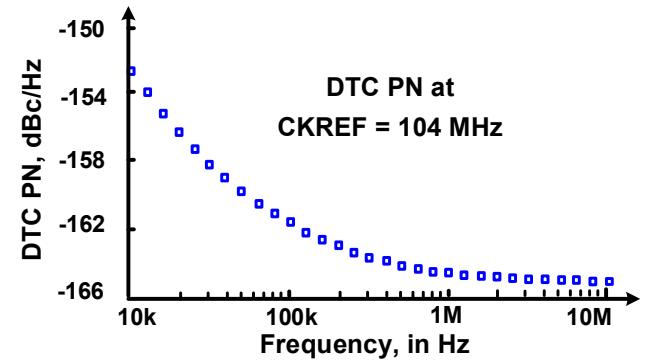
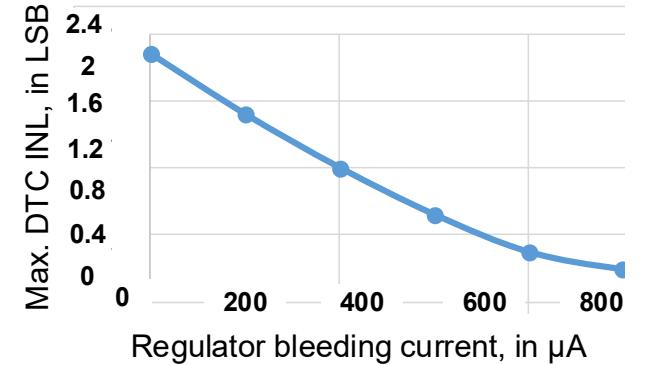
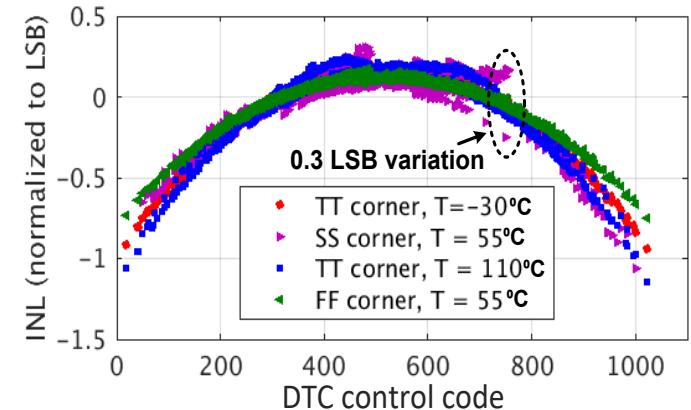


# High Performance DTC Design



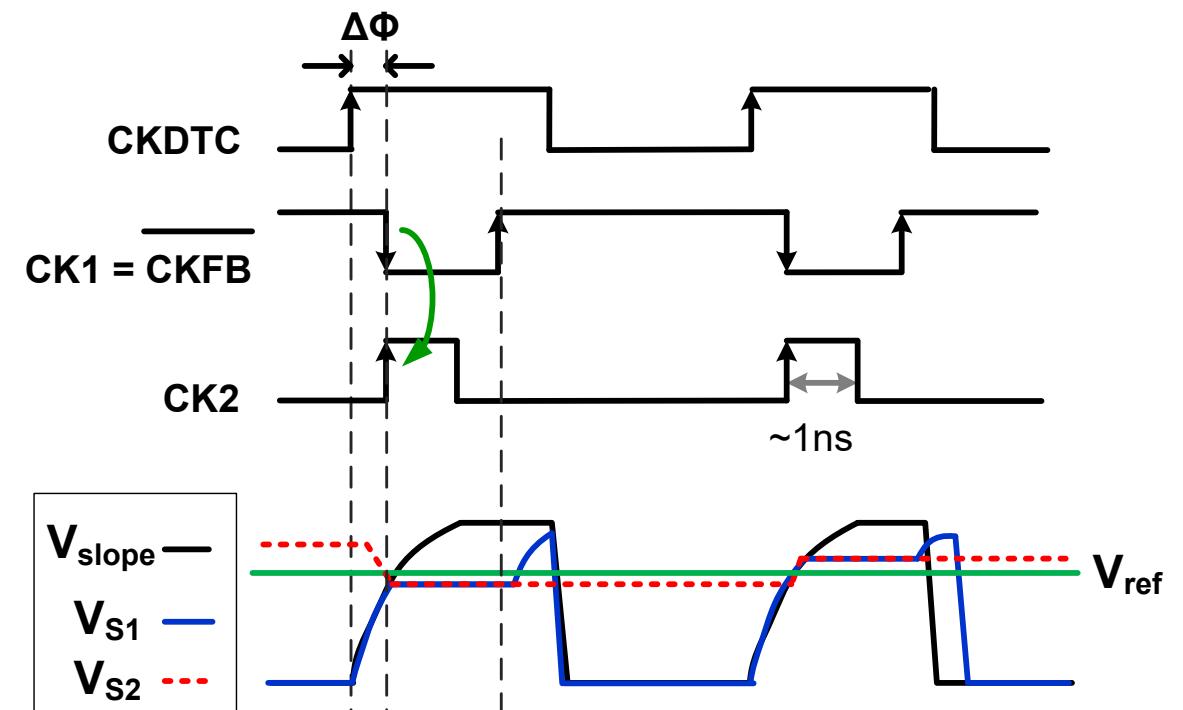
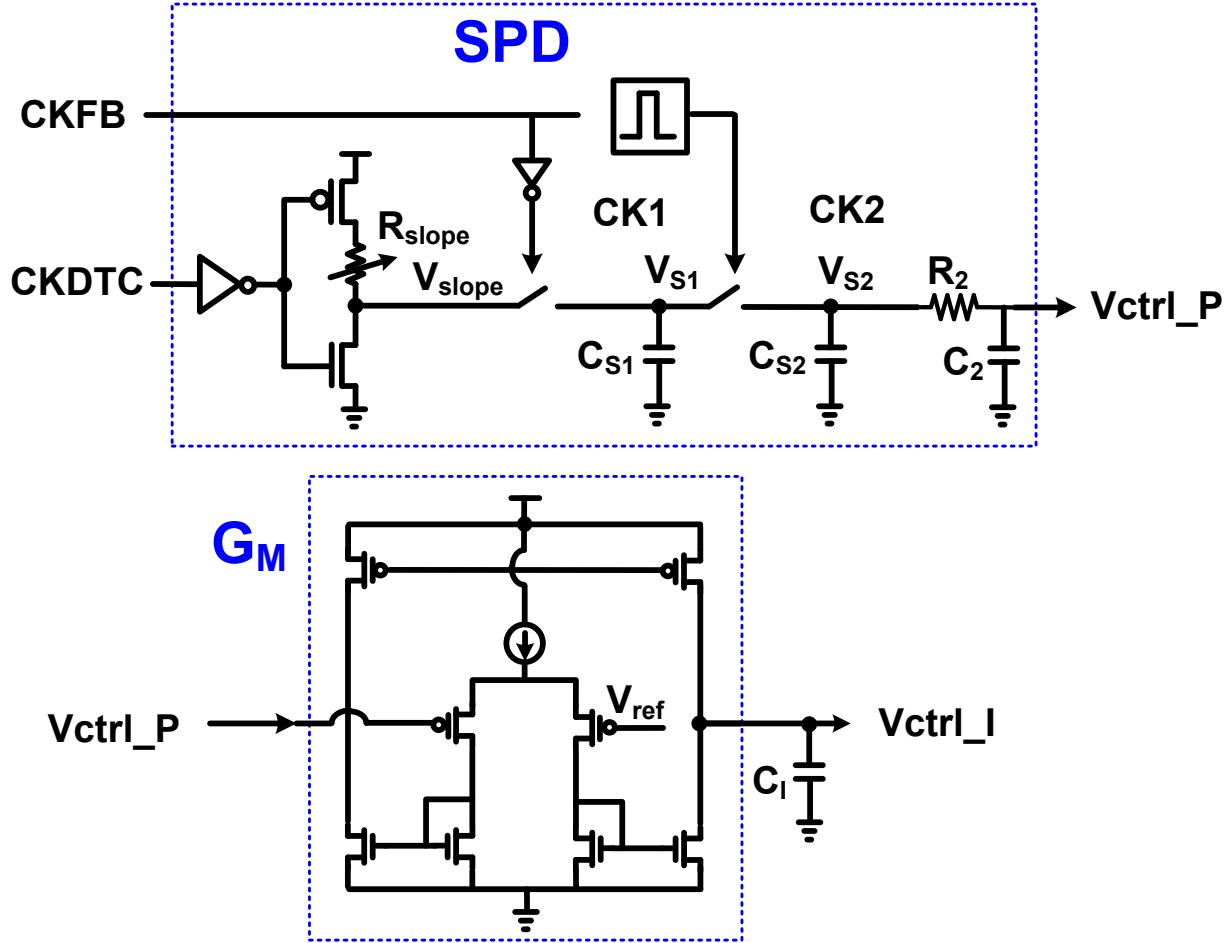
- DTC code reset to “1” each cycle to fully discharge tuning cap.

- Master-slave regulator for fast settling
- Bleeding current  
↑ gm/C to speed up settling at cost of higher  $I_{dc}$
- Programmable R cover process variation



[W. Wu JSSC Dec 2021]

# Implementation of SPD and $G_M$



# Dual-Core VCO for Low PN

## ■ Leeson's equation

$$\mathcal{L} = 10 \cdot \log_{10} \left[ \frac{1}{2} \left( \left( \frac{f_0}{2Q_l f_m} \right)^2 + 1 \right) \cdot \left( \frac{f_c}{f_m} + 1 \right) \cdot \frac{FkT}{P_s} \right]$$

Oscillator output power  $P_s = V^2 / R$

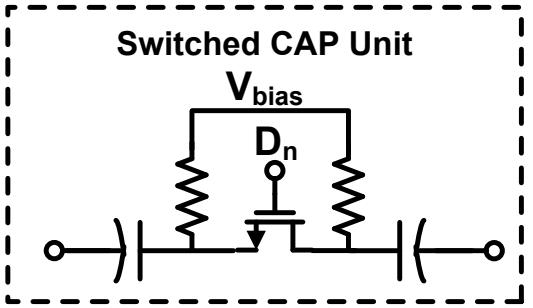
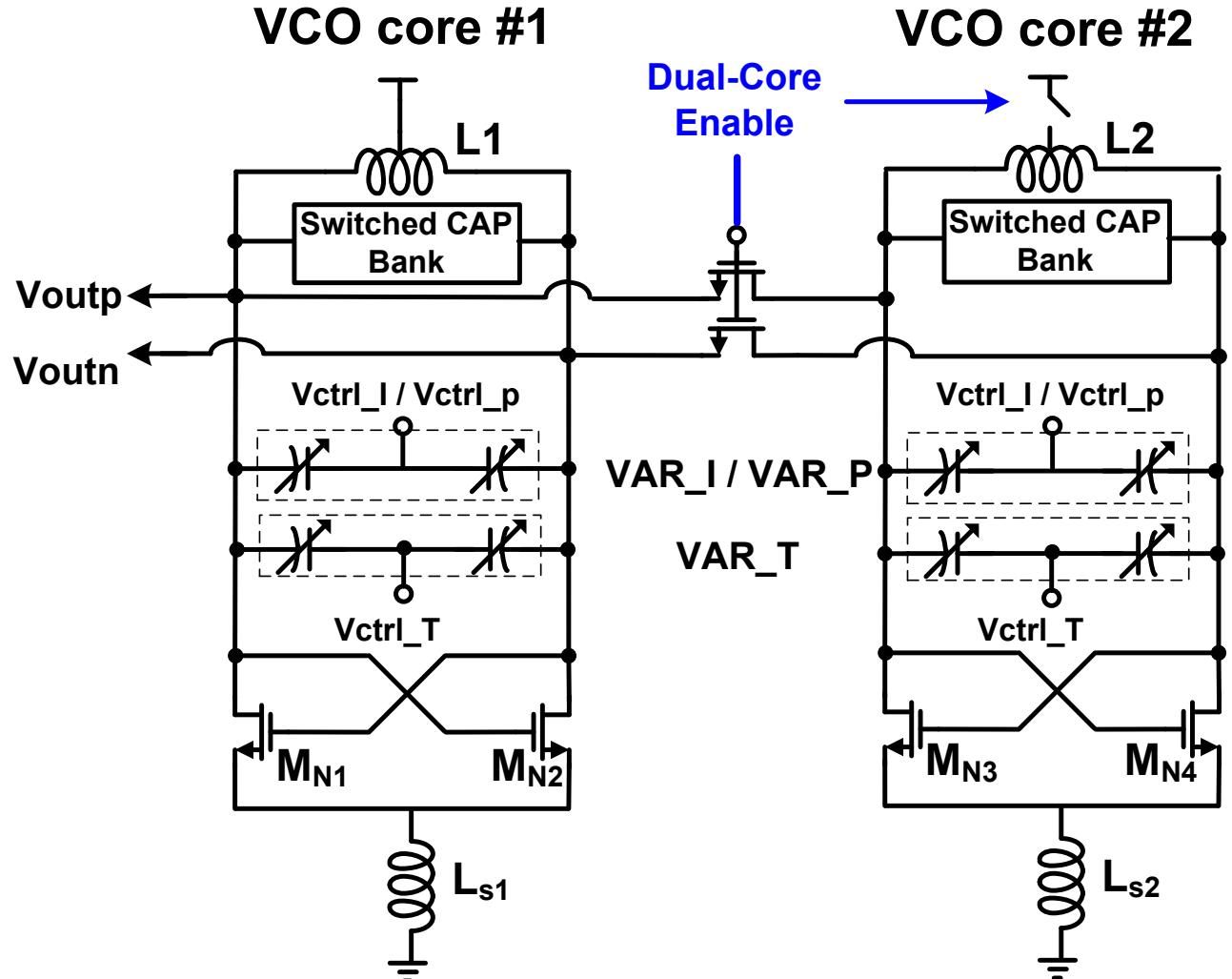
$f_m$  is offset frequency

Quality factor  $Q = R / \omega L = R \cdot \omega C$

$f_c$  is flicker corner frequency

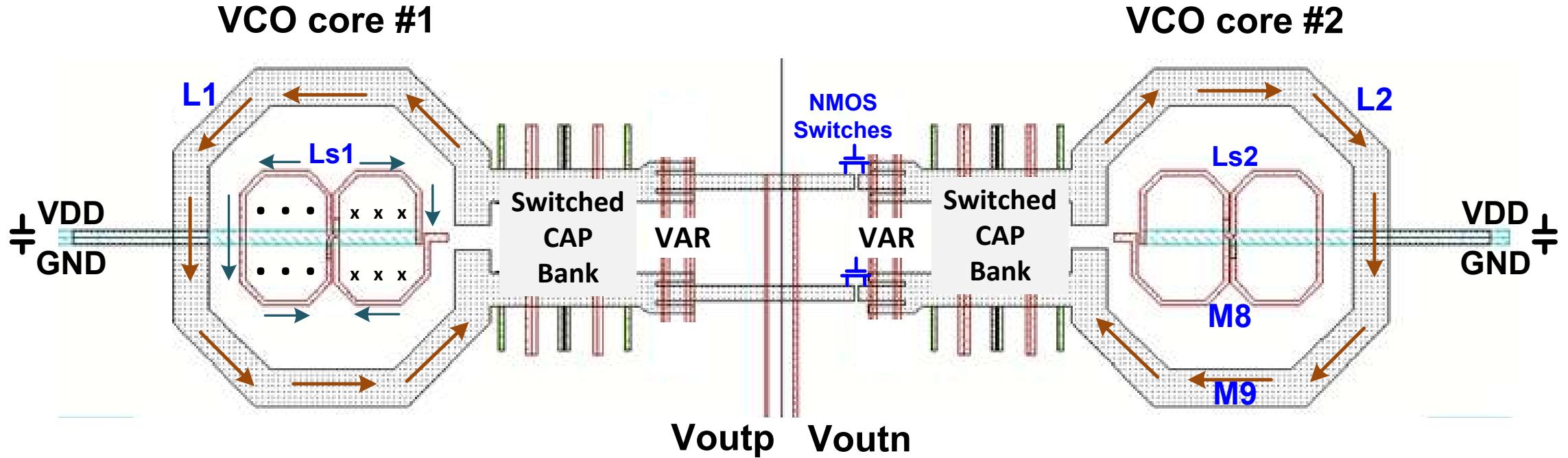
- V is limited by process
- $R \downarrow, L \downarrow$  and  $C \uparrow$ , given Q remains the same  $\rightarrow$  Improves PN
- Cannot reduce L any more  $\rightarrow$  use two VCOs in parallel

$L_{eq} = L/2, C_{eq} = 2 \cdot C \rightarrow f_0$  the same, Q the same, PN 3 dB better



- Reconfigurable: 1-core or 2-core
- Same VCO FoM, tradeoff power for PN

# Layout of Dual-Core VCO

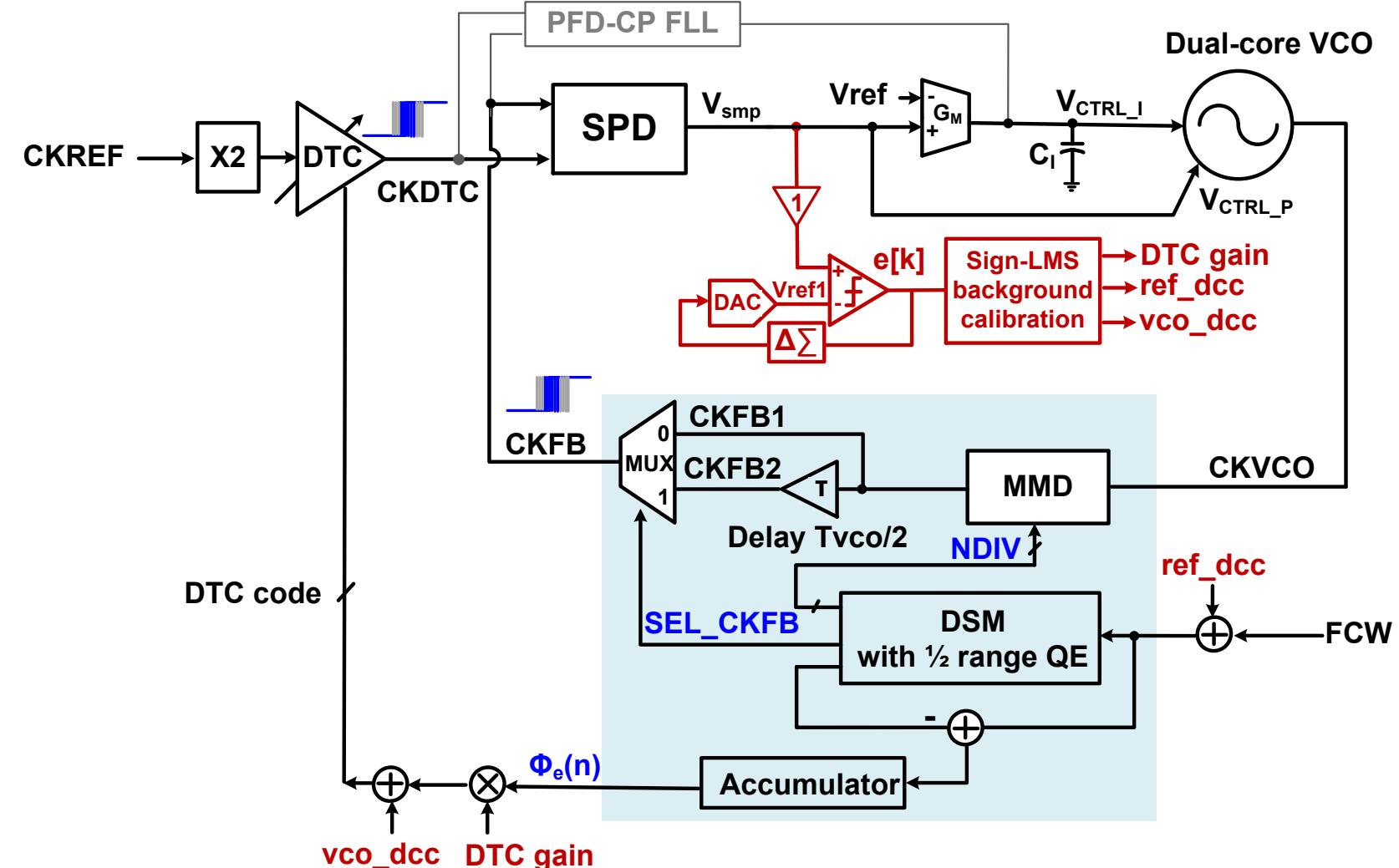


- Good EM isolation → same  $f_{VCO}$  for 1- or 2-core
- Figure-8 tail  $L_s$  put inside main  $L$  to save area
- Fully symmetrical → little current flow through SW

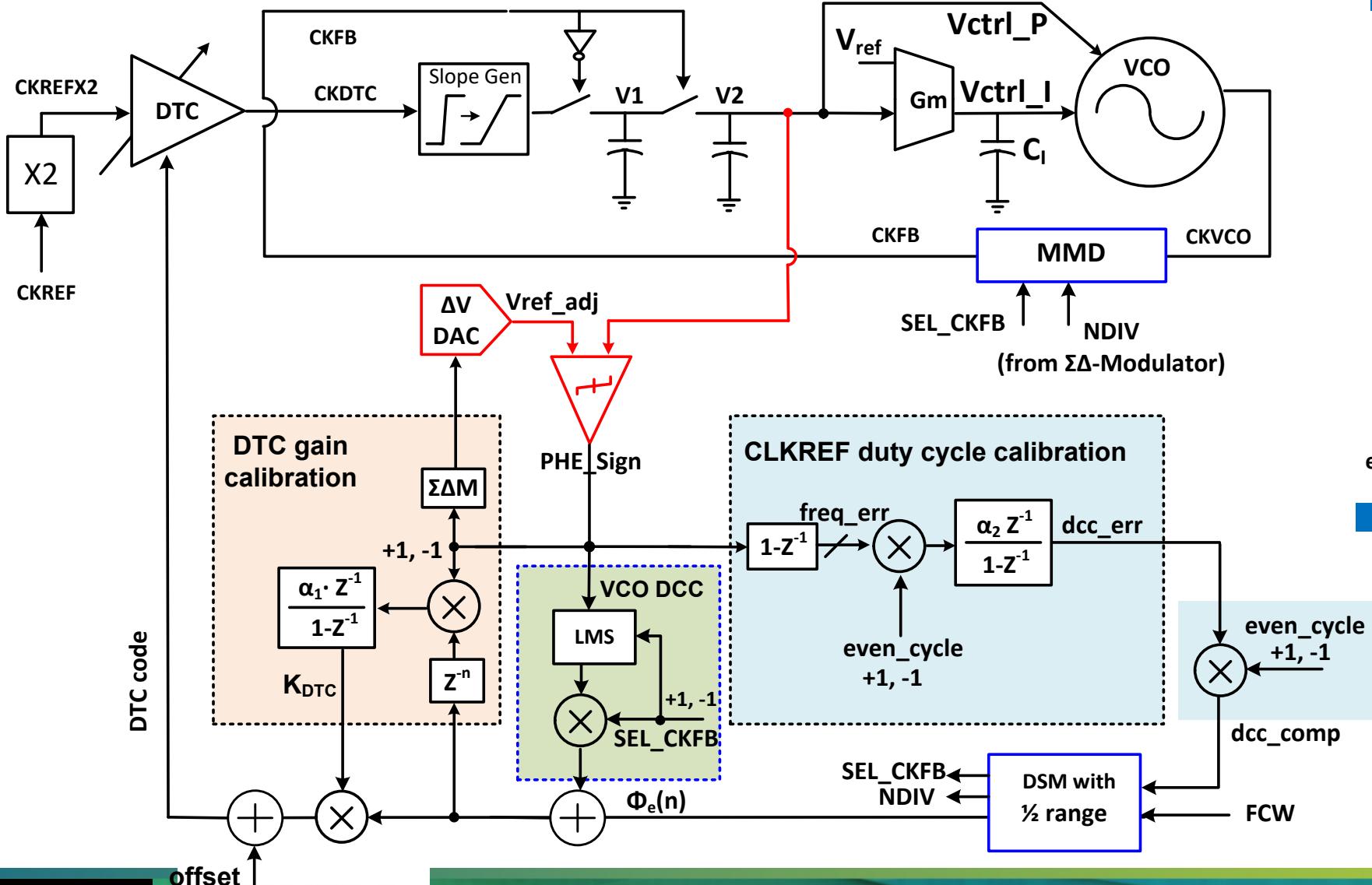
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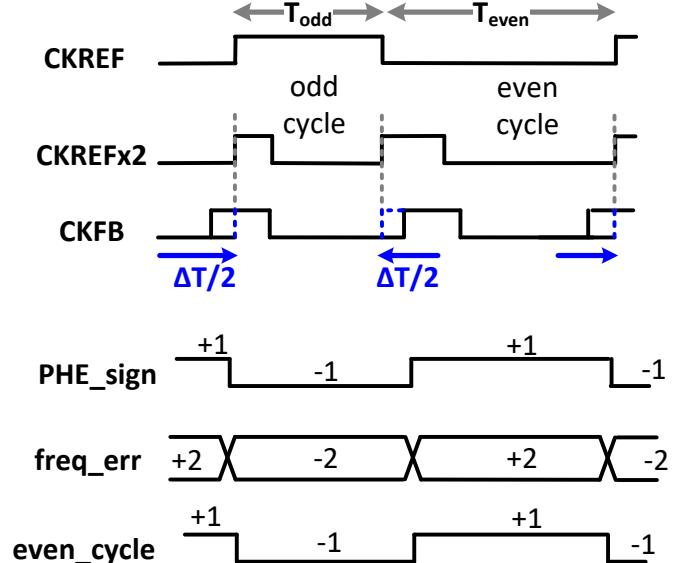
# Advanced Techniques to Lower PLL IPN



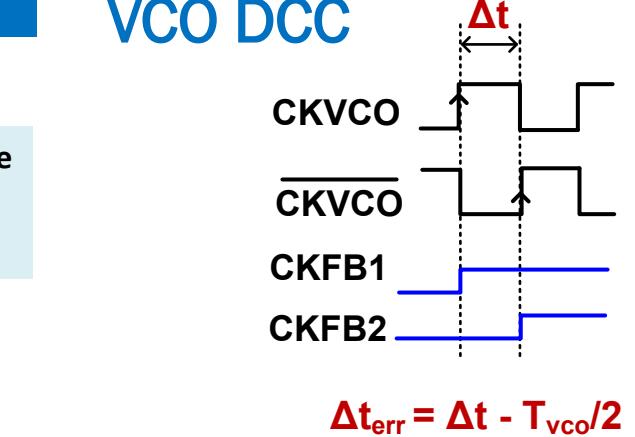
- CKREF doubler → lower inband PN
- DTC range reduction  
*DR↓ → less bits, lower thermal noise and power, more linear*



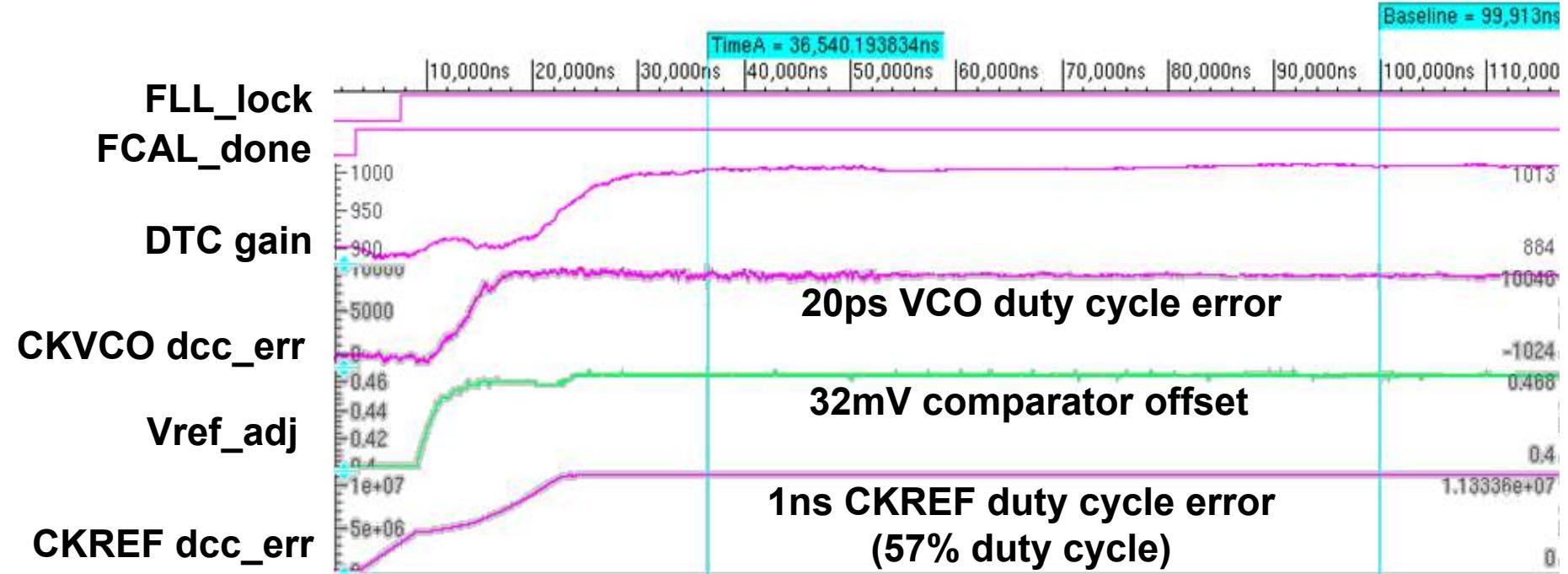
## CLKREF DCC



## VCO DCC

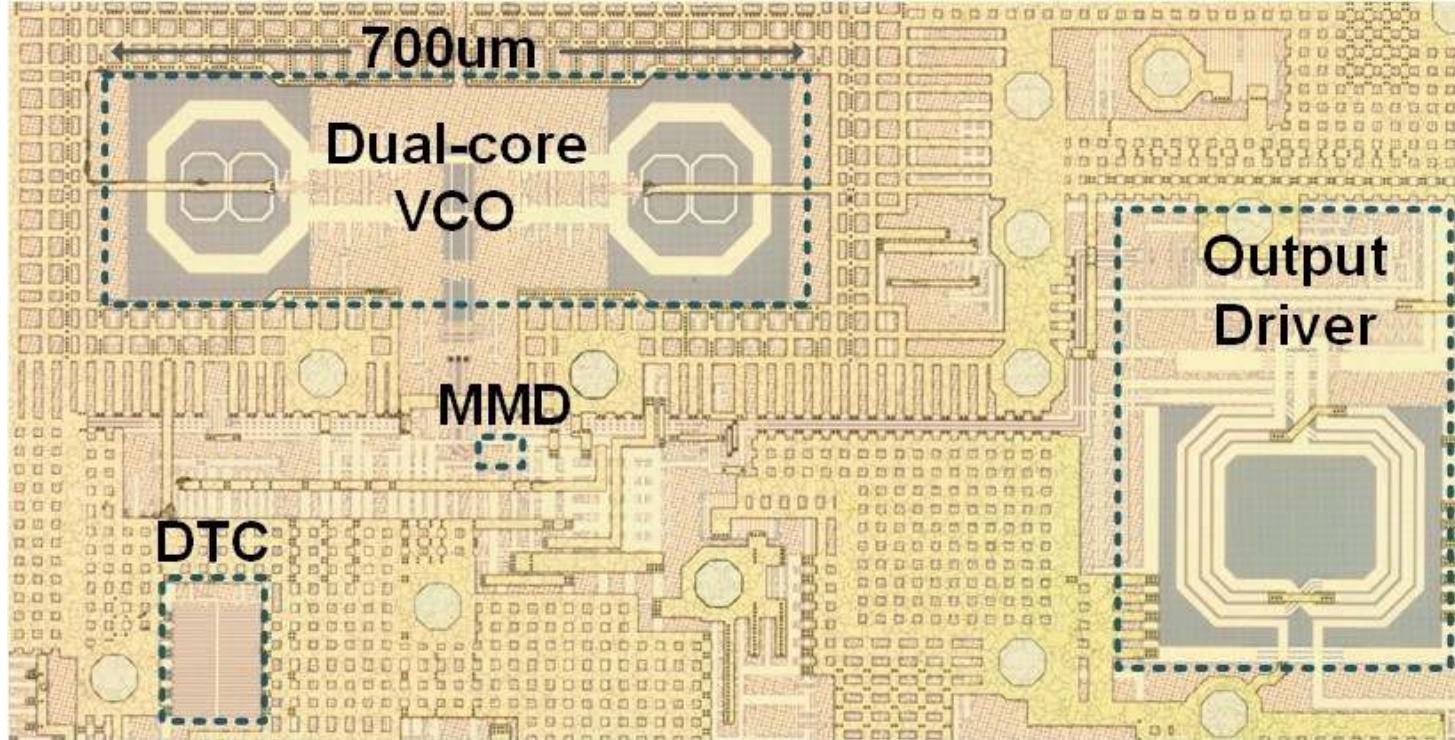


# Simulated Background Calibration

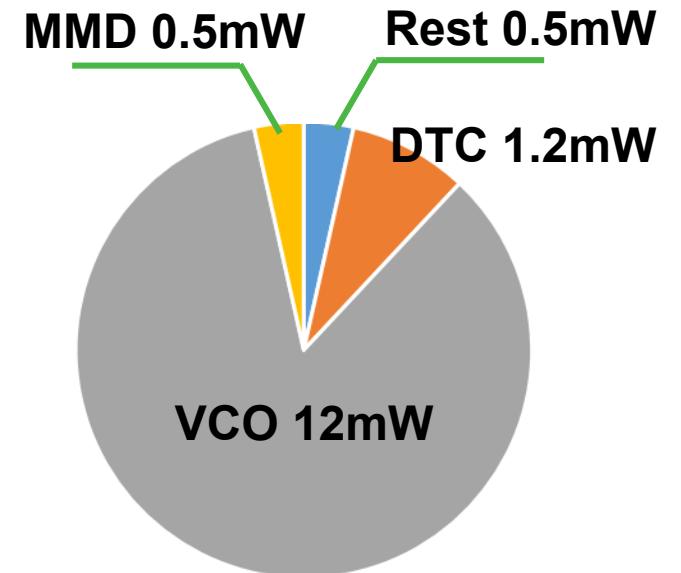


- All calibrations converge < 30us and track PVT
- Works robustly for both integer and fractional channels

# Low-Jitter PLL Die Micrograph

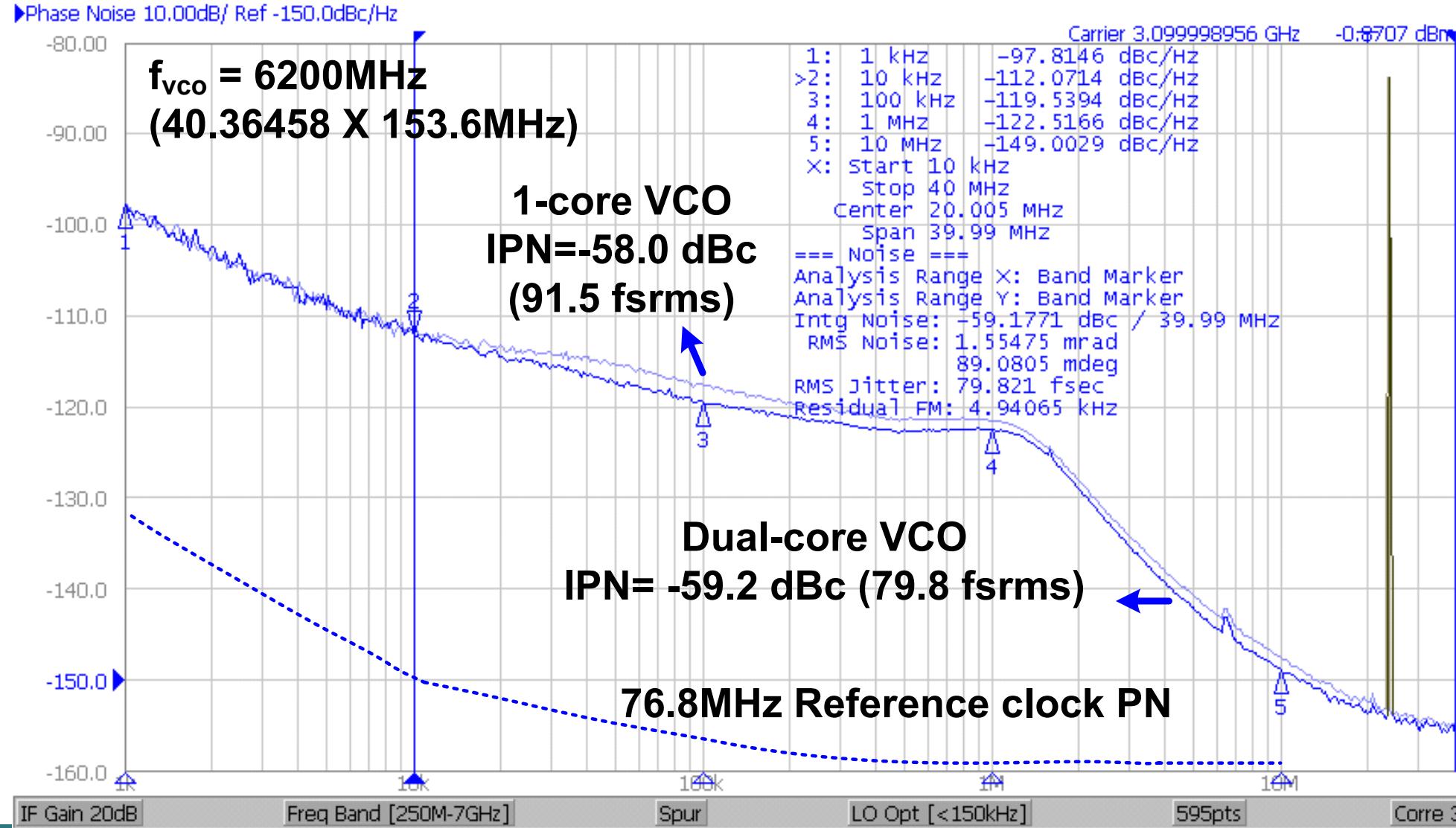


- 14nm FINFET
- Core  $0.31\text{mm}^2$
- Power



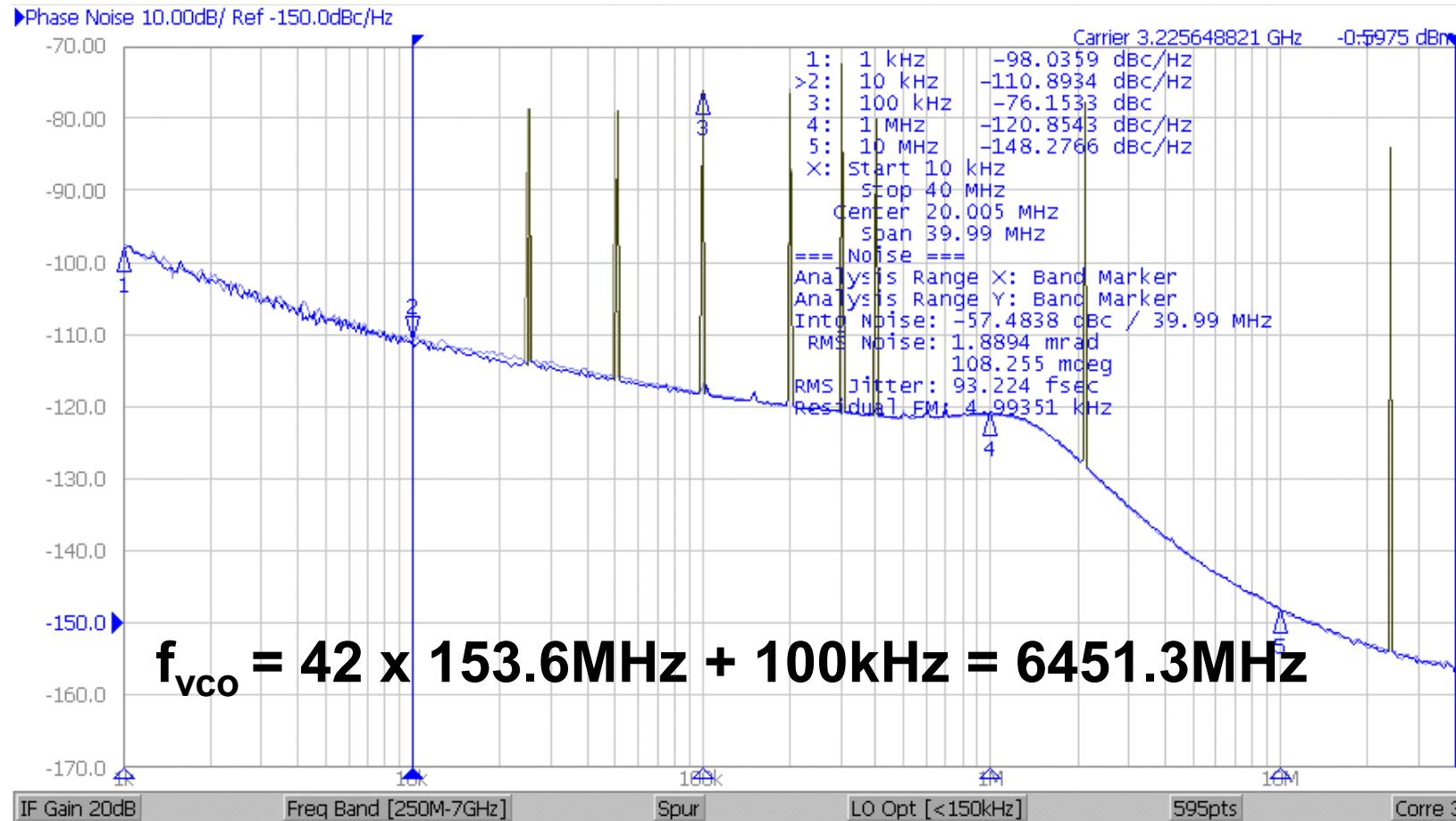
[W. Wu. ISSCC 2021]

# Measured PLL Phase Noise Plot



# Measured Fractional-N Spurs and Jitter

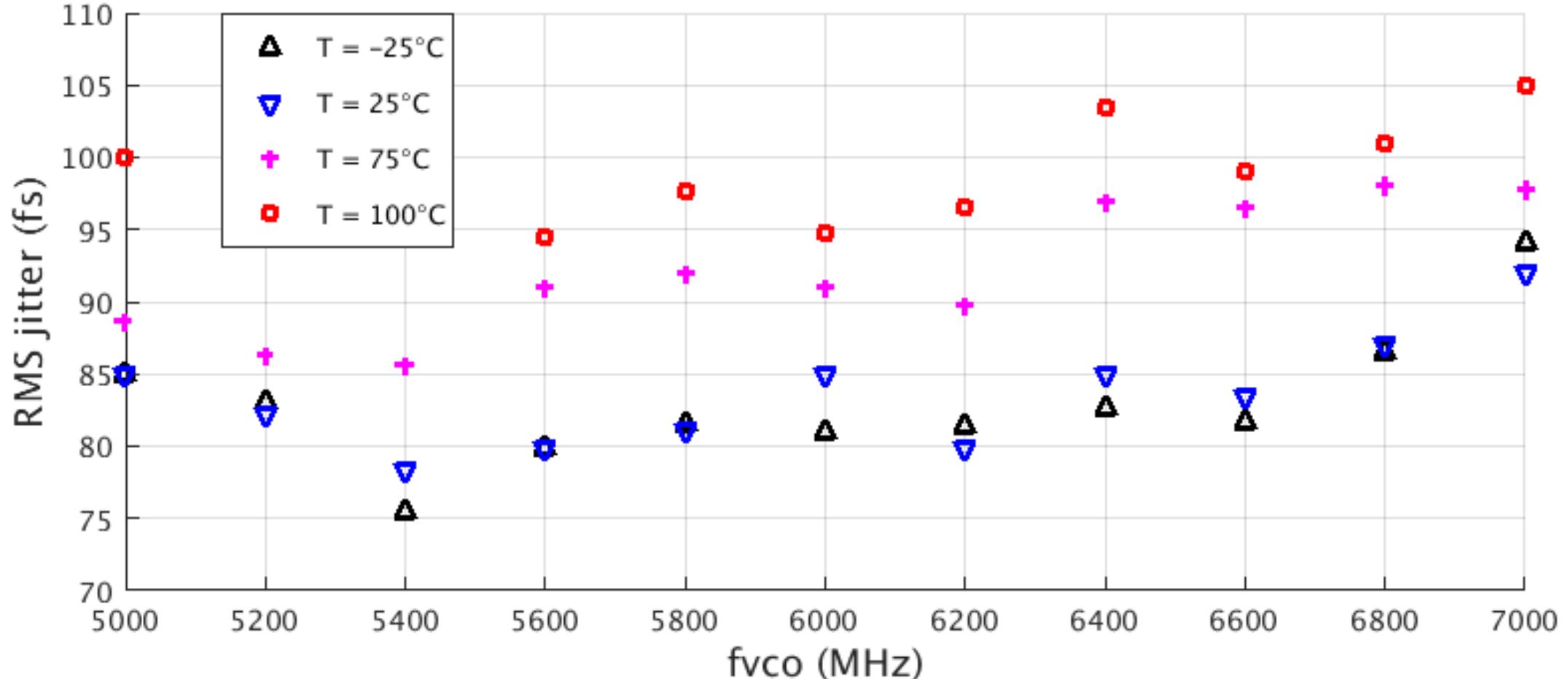
- Near Integer Channel



Spurious Tone Table

Offset Freq.	Spur level, dBc
25 kHz	-78.9
50 kHz	-79.1
100 kHz	-76.1
200 kHz	-76.1
300 kHz	-72.4
400 kHz	-80.2
2.116 MHz	-77.9
23.98 MHz	-84.1

# Measured PLL rms Jitter Across Tung Range



# Comparison to State-of-the-Art PLLs

	This work	X. Gao ISSCC'16	C. Yao JSSC'17	W. Wu JSSC'19	Y. Hu ISSCC'20	A. Santiccioli ISSCC'20
Technology	14 nm	28 nm	14 nm	28 nm	28 nm	28 nm
Type	Analog Type-II	Digital Type-II	Digital Type-II	Analog Type-II	Digital Type-II	Analog Type-I
Phase detector	SPD	SPD	TDC	SPD	Charge sharing PD	SPD
Reference (MHz)	76.8X2	40	26	52X2	250	500
F <sub>out</sub> (GHz)	3.1	5.825	2.69	6.33	26.25	12.47
rms jitter (fs)	80/91.5 <sup>1</sup> (10k to 40M)	159 (10k to 10M)	137 (10k to 10M)	75 (10k to 10M)	75.89 (10k to 30M)	58.2 (1k to 100M)
Near-integer fractional spur (dBc)	-72.4	-54	-78.6	-64	Integer-N only	-63.9
Ref. spur (dBc)	-72	-78	-87.6	-70.2	-45.15	-73.5
Power (mW)	14.2/8.2 <sup>1</sup>	8.2	13.4	18.9	16.5	18
FoM (dB)	-250.4/-251.6 <sup>1</sup>	-246.8	-246	-249.7	-250.2	-252.1
Core area (mm <sup>2</sup> )	0.31	0.3	0.257	0.45	NA	0.16

<sup>1</sup> VCO 1-core mode

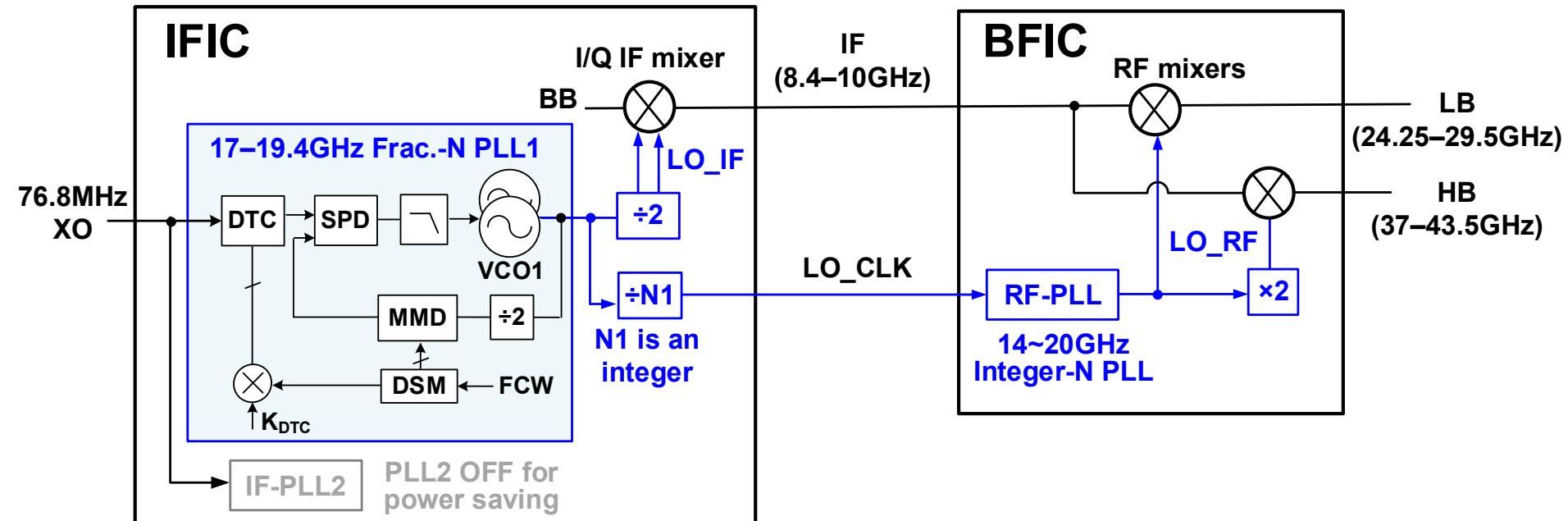
$$\text{FoM} = 10 \cdot \log_{10}((\sigma t / 1 \text{ s})^2 \cdot \text{Power} / 1 \text{ mW})$$

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# Overall LO Topology

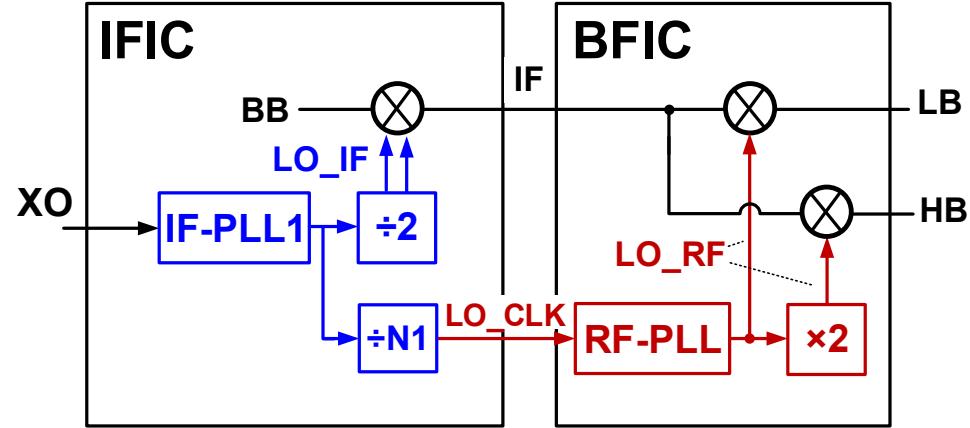
- IFIC generates **LO\_IF** & **LO\_CLK** for BFIC
- DTC-based low-jitter frac.-N PLL in IFIC → dominate LO chain IPN
- RF-PLL in BFIC is integer-N of wide BW  
→ low-power, wideband VCO for **multi-band** (24.25 GHz – 43.5 GHz)



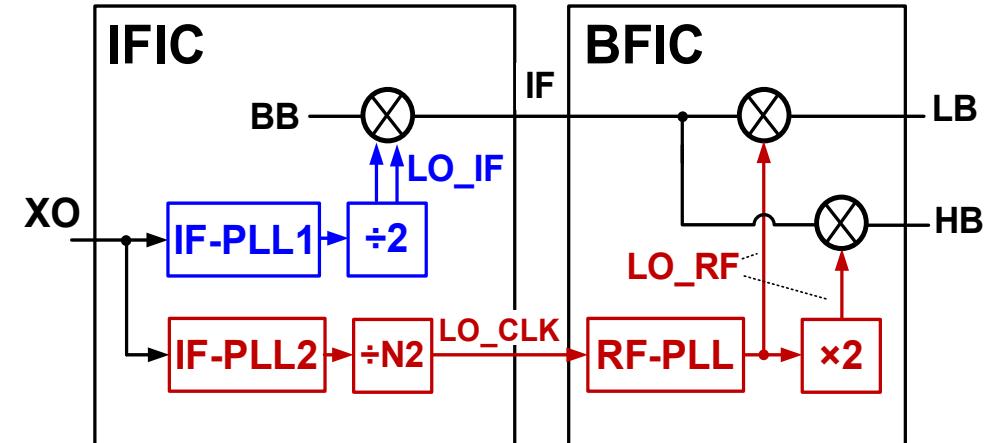
# LO Configuration for Lower IPN

- 256-QAM requires rms jitter of  $\sim 100$  fs
- Use IF-PLL2 to generate LO\_CLK
- PN of LO\_IF and LO\_RF are mostly uncorrelated  $\rightarrow$  lower chain IPN

Low-power mode for 64-QAM/QPSK

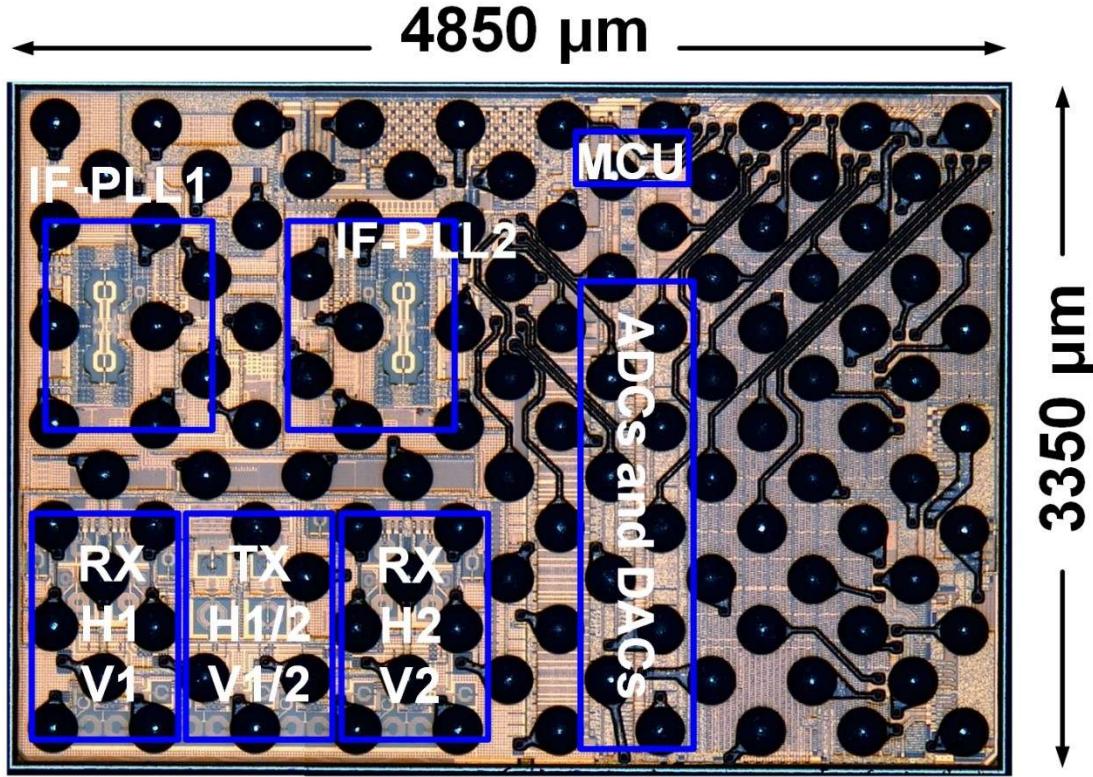


Low-jitter mode for 256-QAM

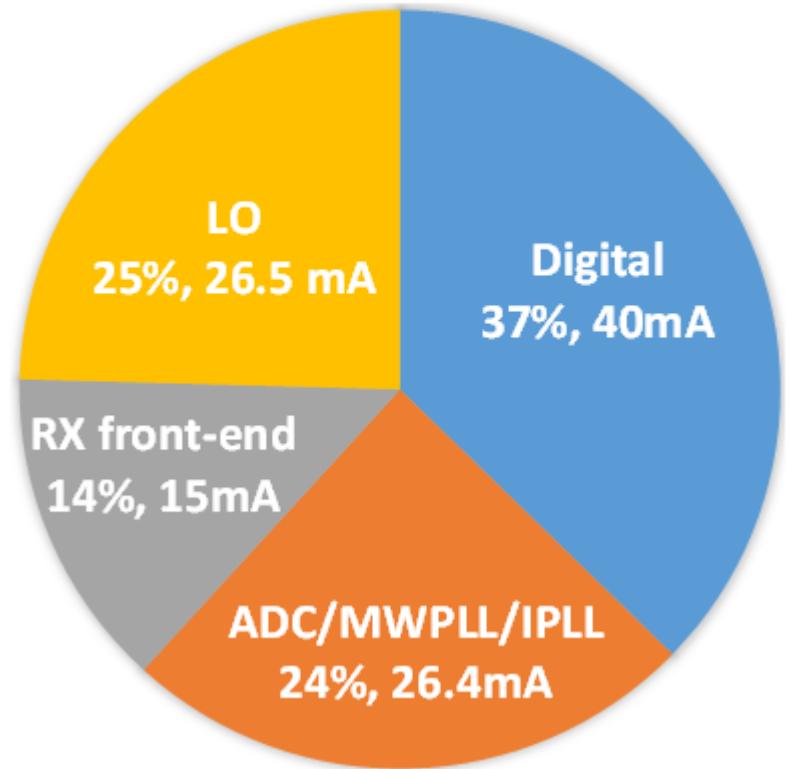


# 5G FR2 IFIC Chip Micrograph

- 14 nm FinFET process

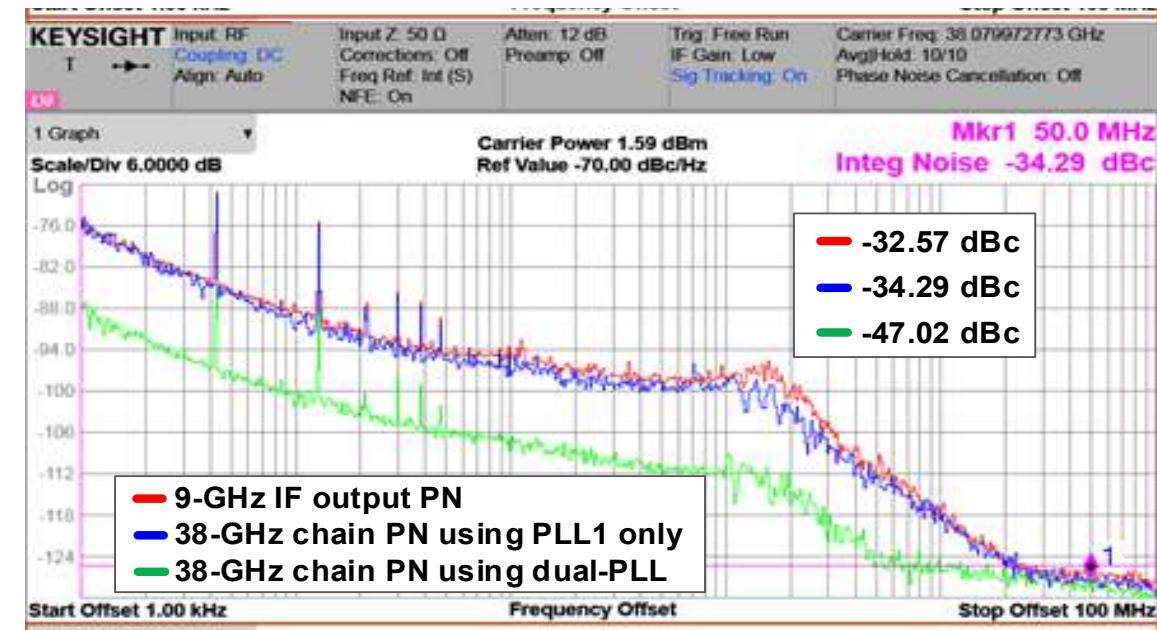
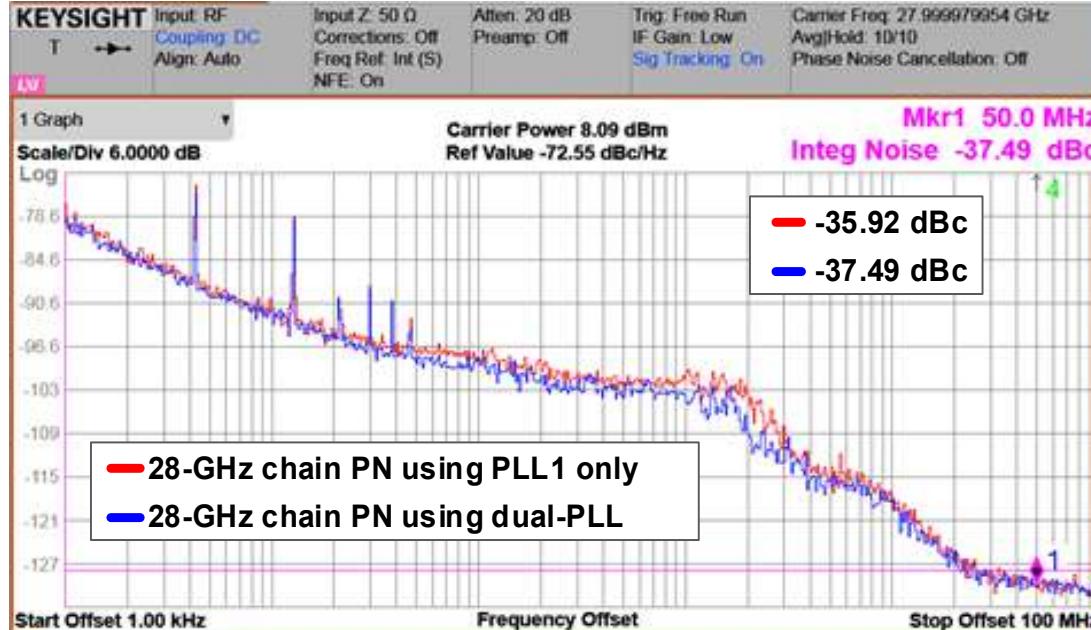


64-QAM DL  
Total Current, mA @ 4V VBAT  
(1CC 100MHz Max TP)



[W. Wu, RFIC 2023]

# Measured Chain IPN at 28 GHz and 39 GHz



- Dual-PLL results in ~1.6 dB lower chain IPN
- -37.49 dBc IPN at 28 GHz → EVM floor of 1.34%
- -34.29 dBc IPN at 38 GHz → 112 fs rms jitter, EVM floor of 1.9%

# Summary

- DTC-assisted fractional-N PLL enables low jitter, low fractional spurs
- Reference CLK doubler, DTC range reduction reduces PLL rms jitter further
- Reconfigurable multi-core VCO provides PN and power tradeoff
- Using dual-PLL to generate IF-LO and RF-LO achieves rms jitter of ~110 fs at 40 GHz for 256-QAM