Tu4B_2

Realization of Low-Loss Fully Passive Harmonic Rejection N-Path Filters

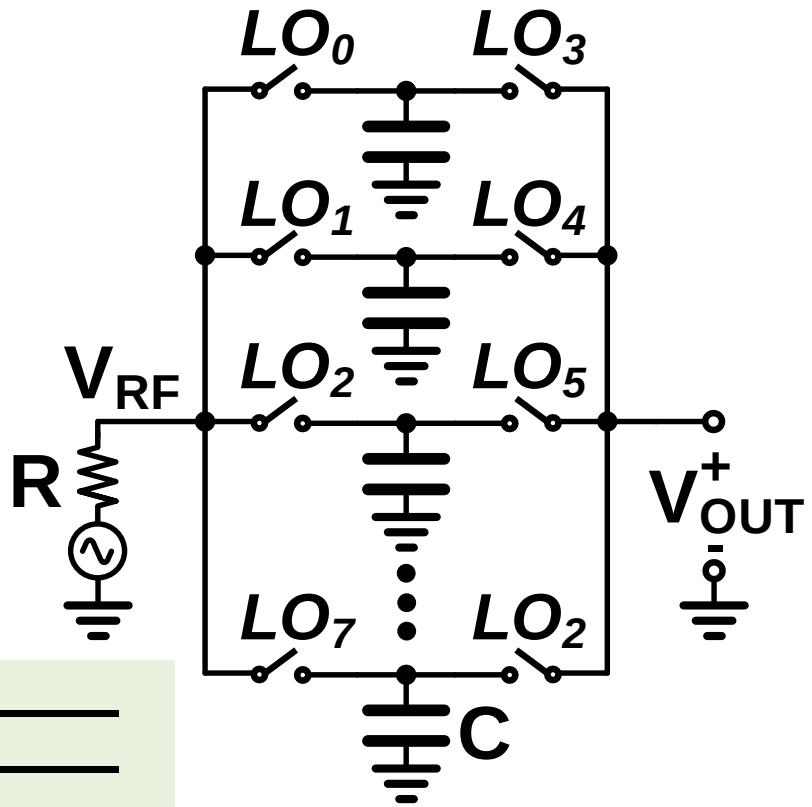
S. Araei, S. Mohin, N. Reiskarimian

Massachusetts Institute of Technology, Cambridge, MA, USA

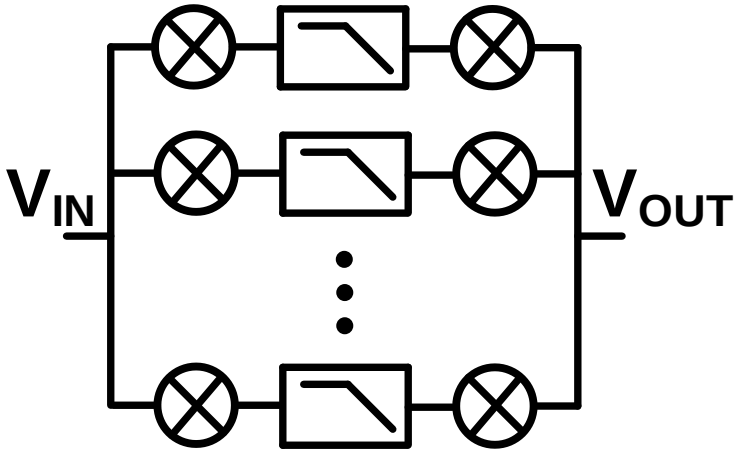
Outline

- Motivation and Introduction
- Switch-Capacitor Harmonic Rejection Approaches
- Circuit Implementation
- Measurement Results
- Conclusion

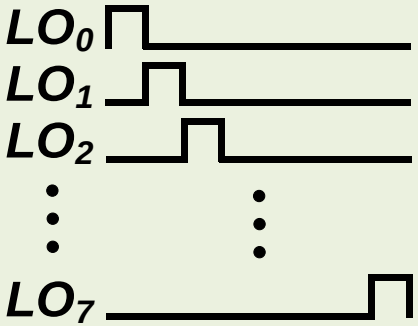
N-Path Filters (I)



High-Q filtering at RF is possible.



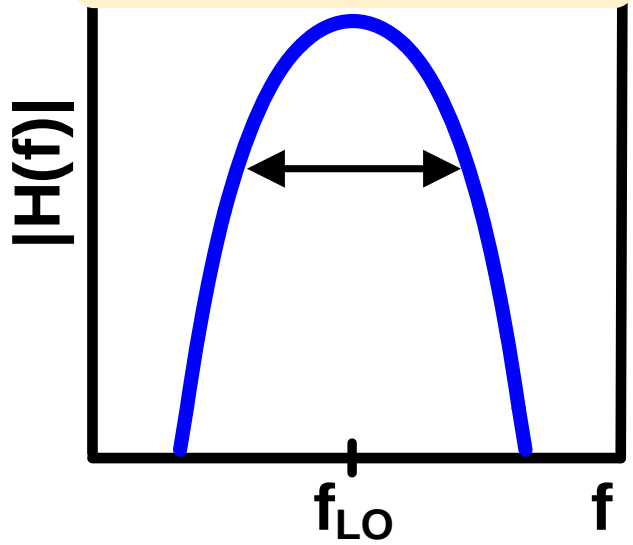
- ❑ Mix down
- ❑ Filter
- ❑ Mix up



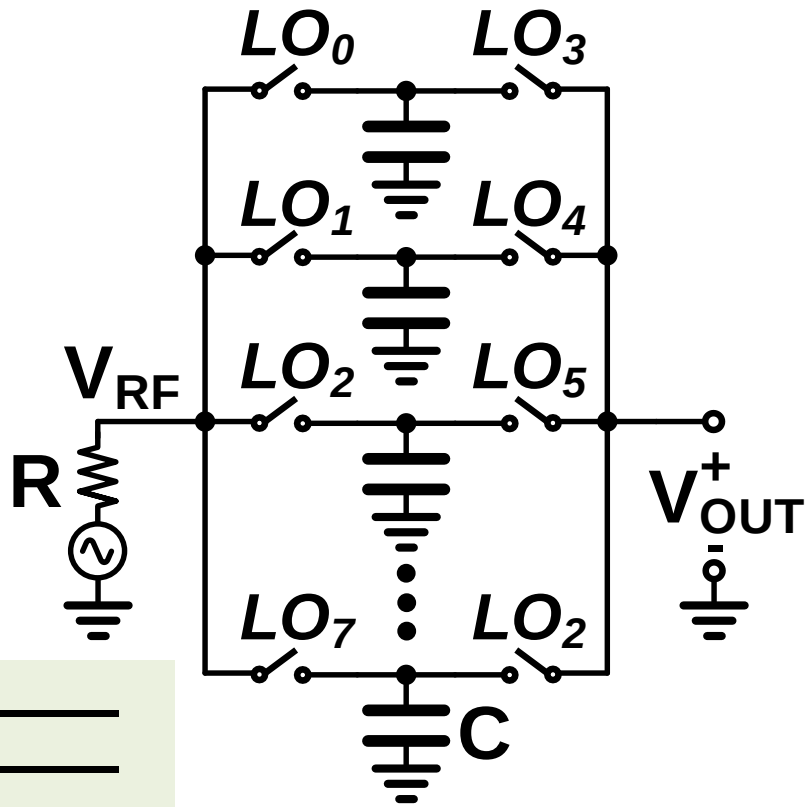
Non-Overlapping Clocks

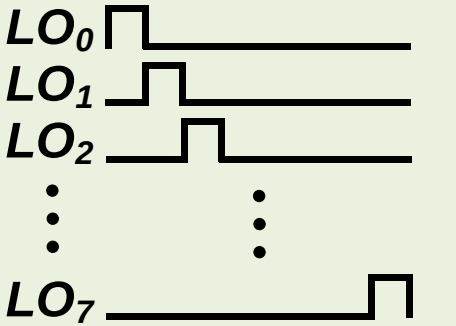
$$Q = \frac{f_{LO}}{BW} = 2\pi NRCf_{LO}$$

$BW = (2\pi NRC)^{-1}$



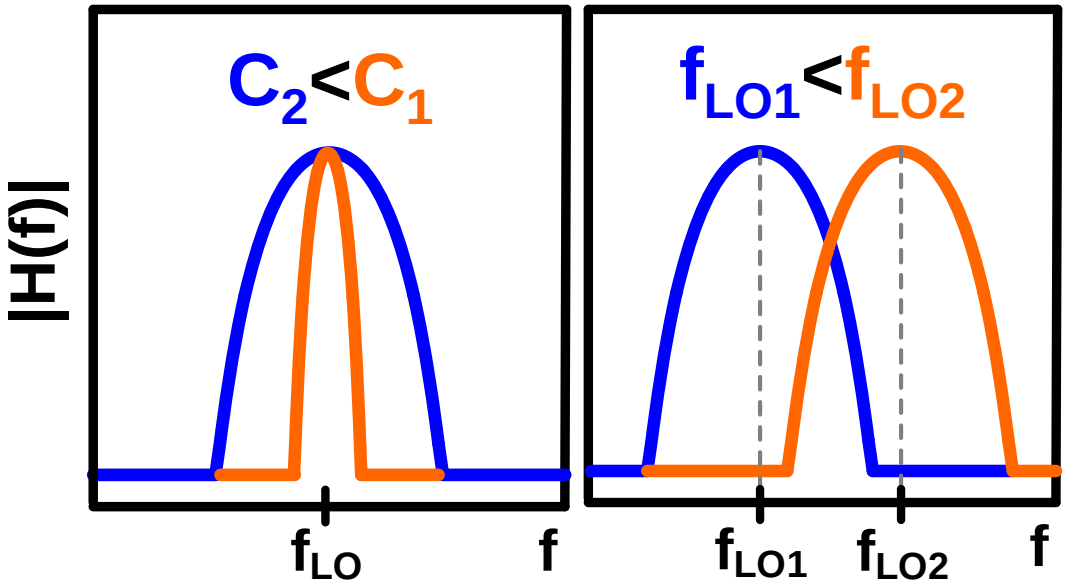
N-Path Filters (II)





Non-Overlapping Clocks

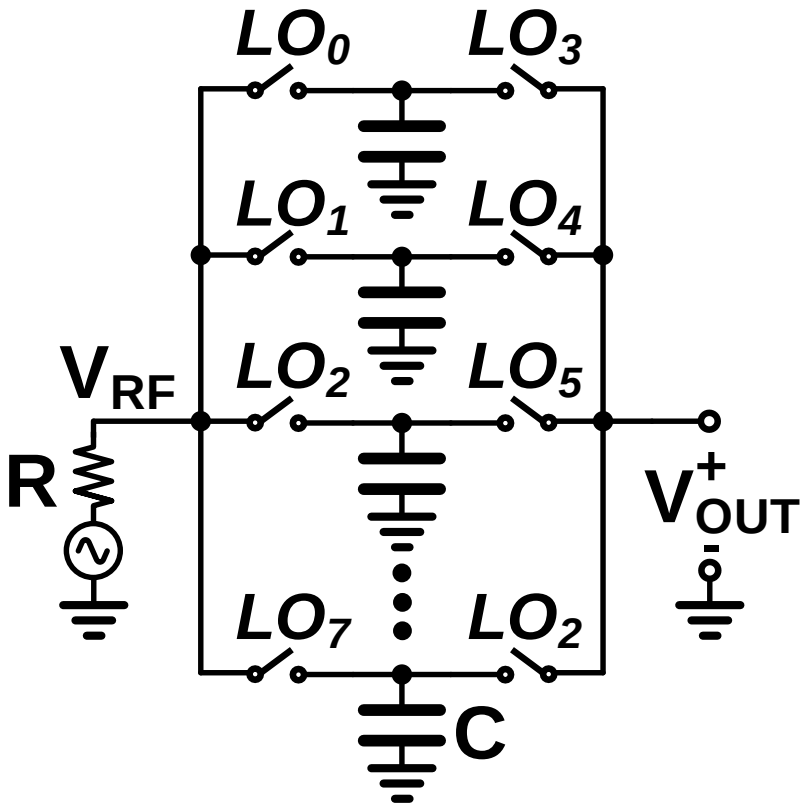
✓ Fully Reconfigurable



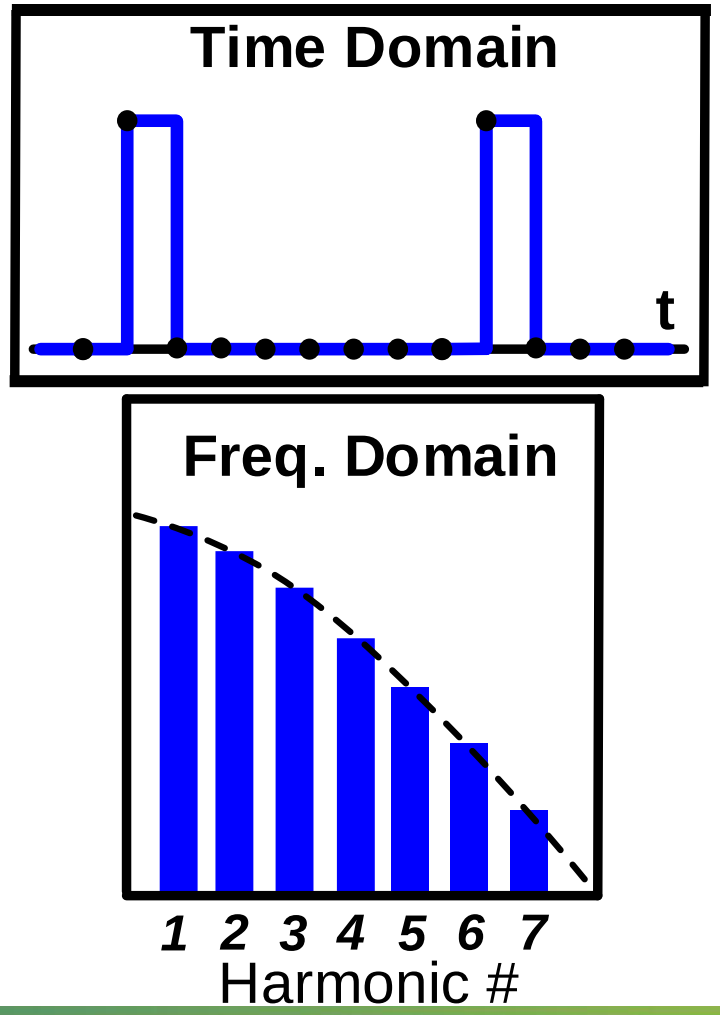
Tunable Bandwidth

Tunable Center Freq

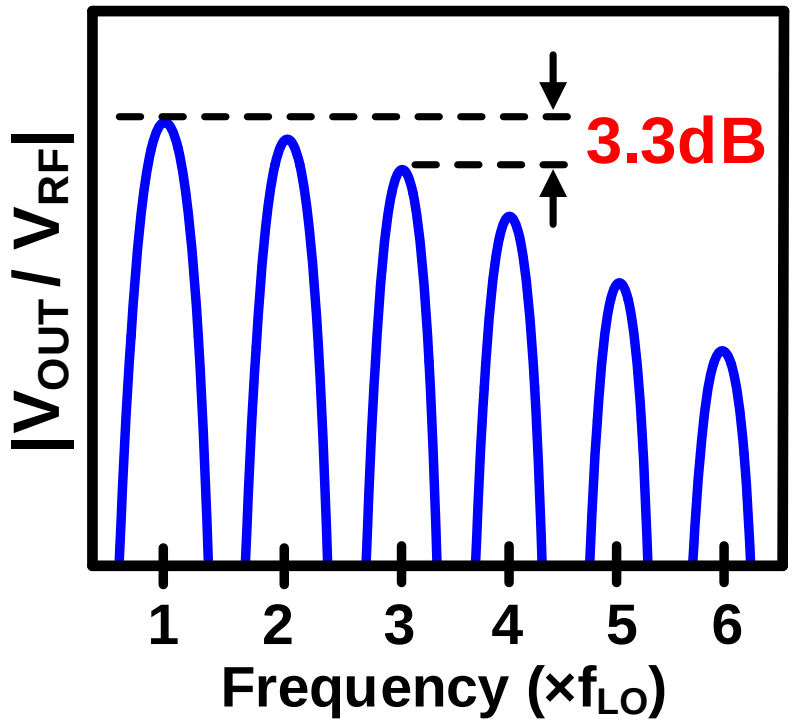
Harmonic Blocker Challenge



LO waveform

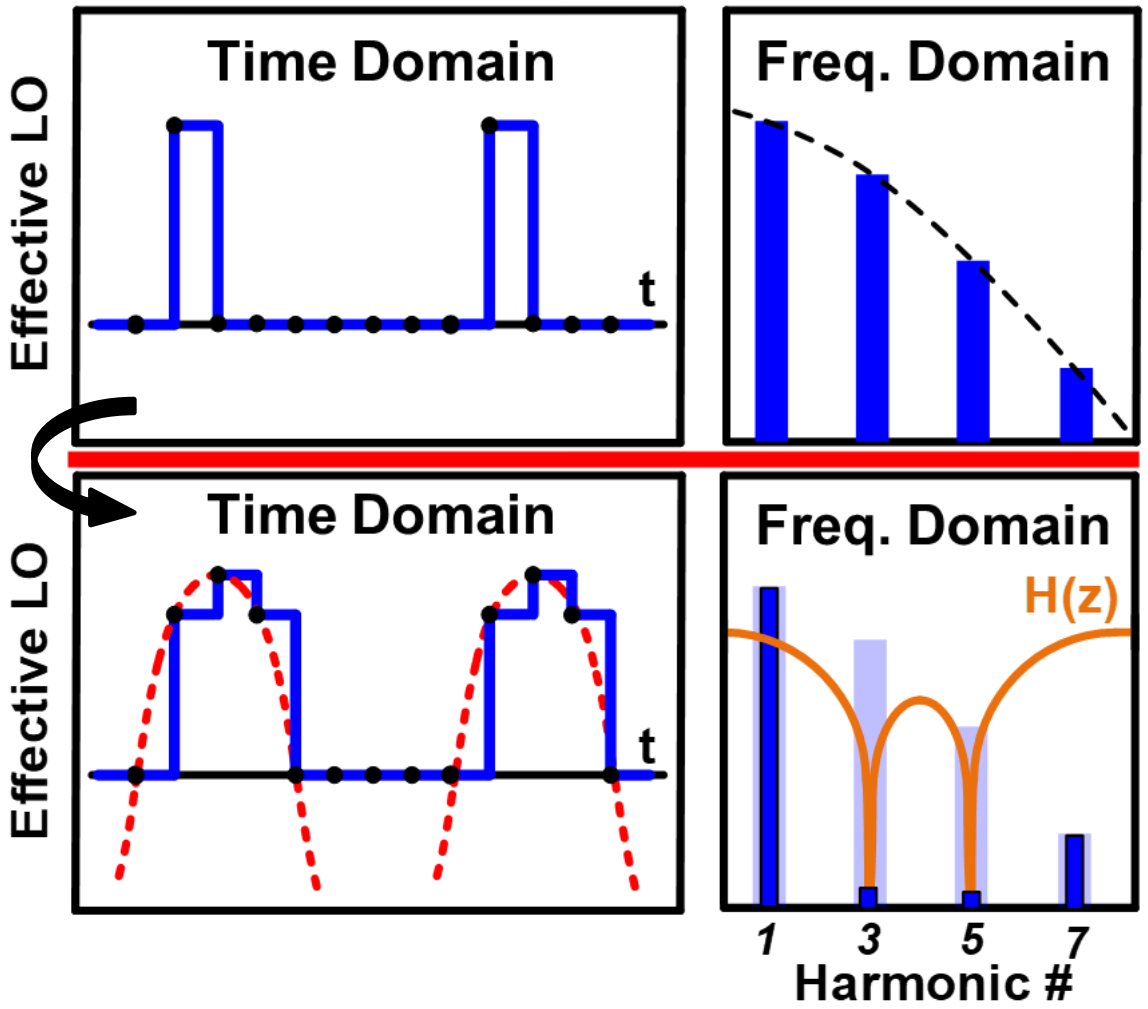


Filter response



Harmonic mixing causes passbands around nf_{LO}

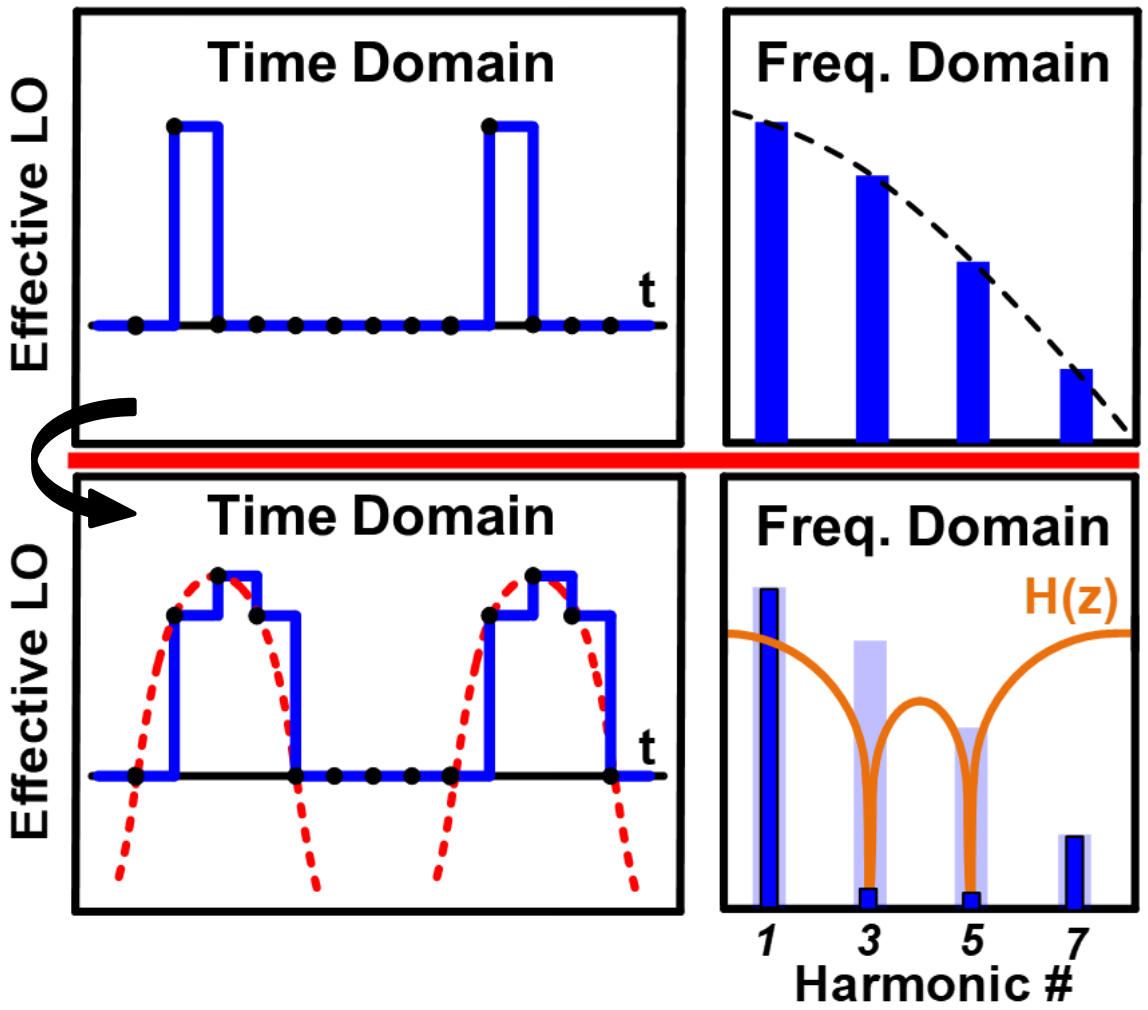
Harmonic Rejection Filter



Desired: Harmonic Rejection FIR Filter

$$H(z) = 1 + \sqrt{2}z^{-1} + z^{-2}$$

Harmonic Rejection Filter

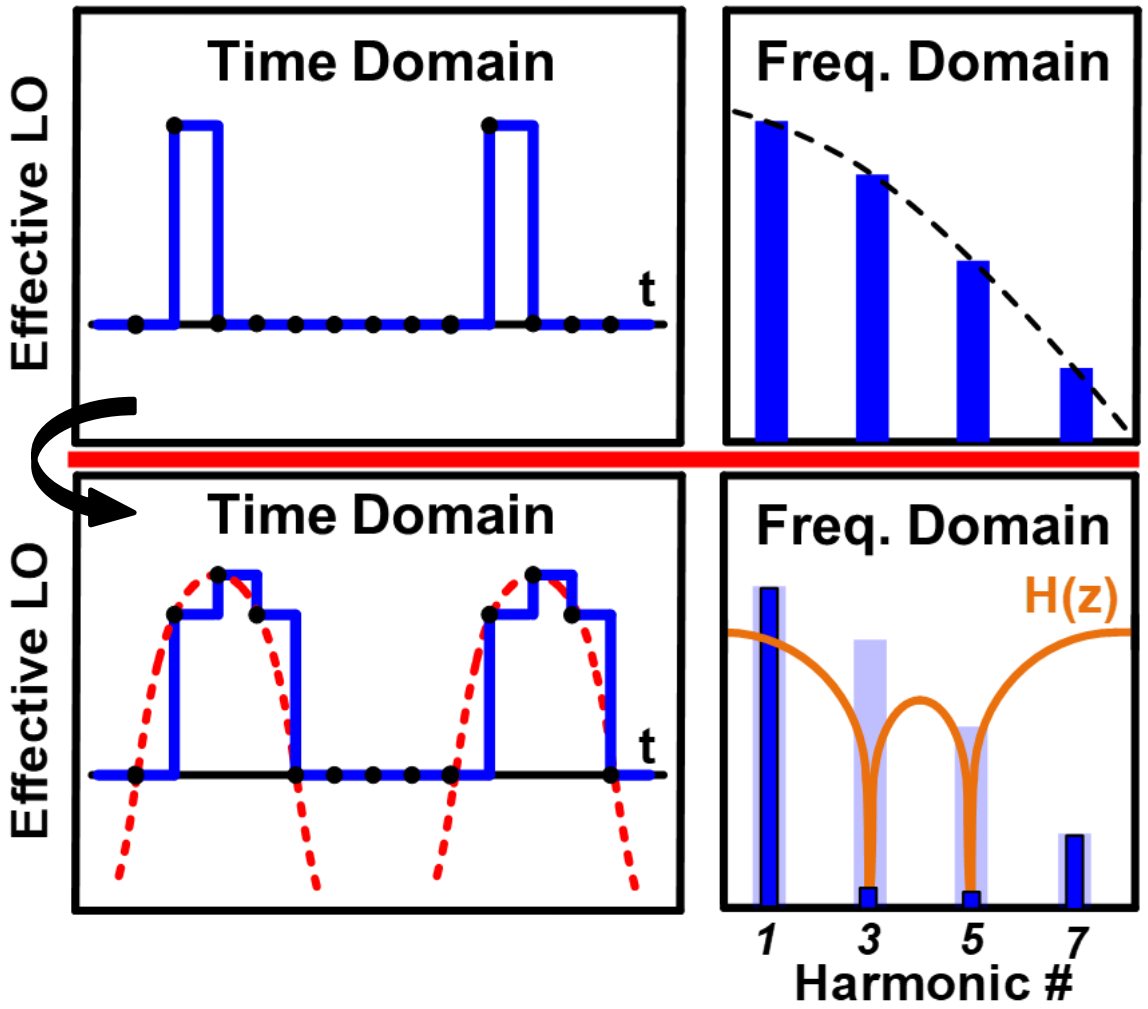


Desired: Harmonic Rejection FIR Filter

$$H(z) = 1 + \sqrt{2}z^{-1} + z^{-2}$$

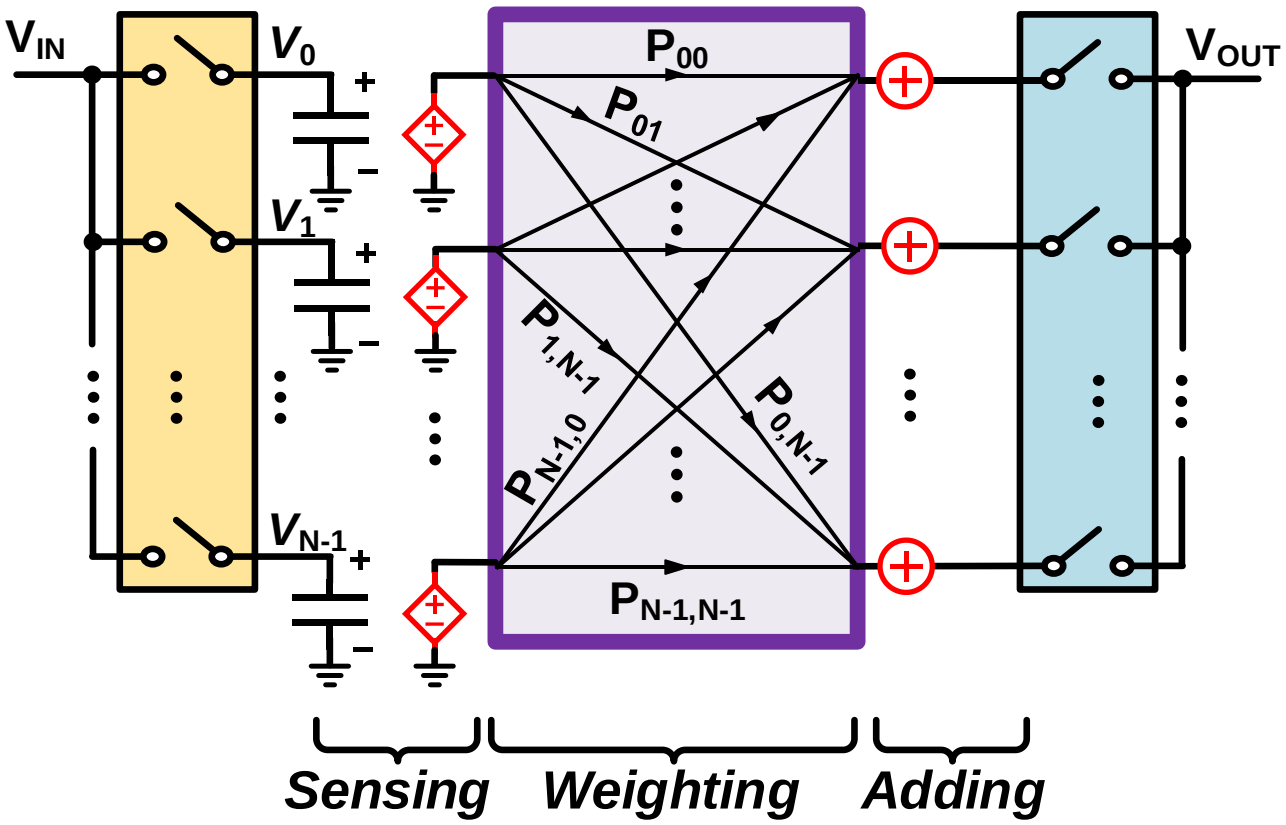
Direct implementation requires "delay" elements @ RF

Harmonic Rejection Filter



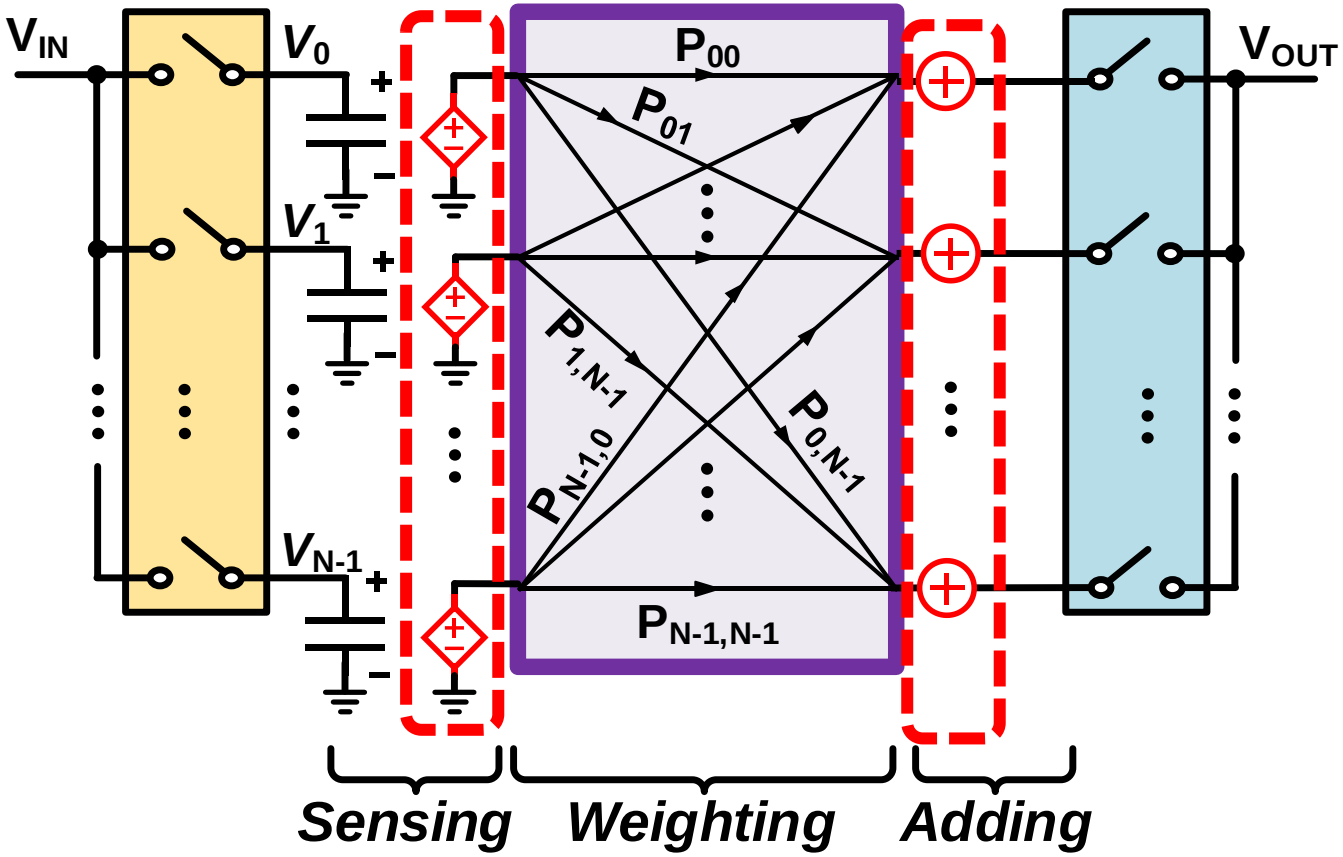
Desired: Harmonic Rejection FIR Filter

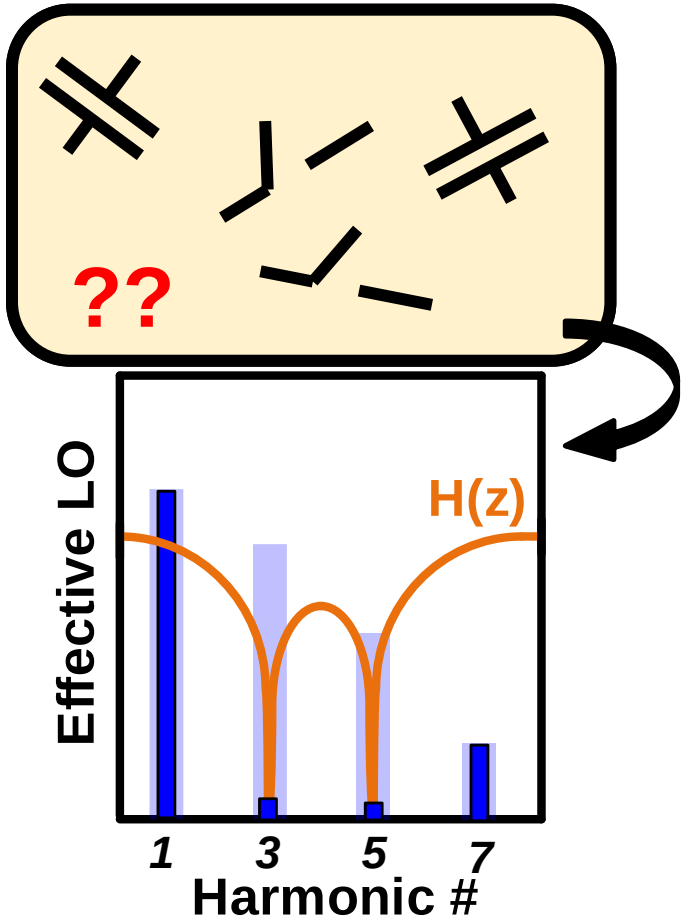
$$H(z) = 1 + \sqrt{2}z^{-1} + z^{-2}$$



[P. P. Vaidyanathan 1988]

Block Filtering with Switch-C



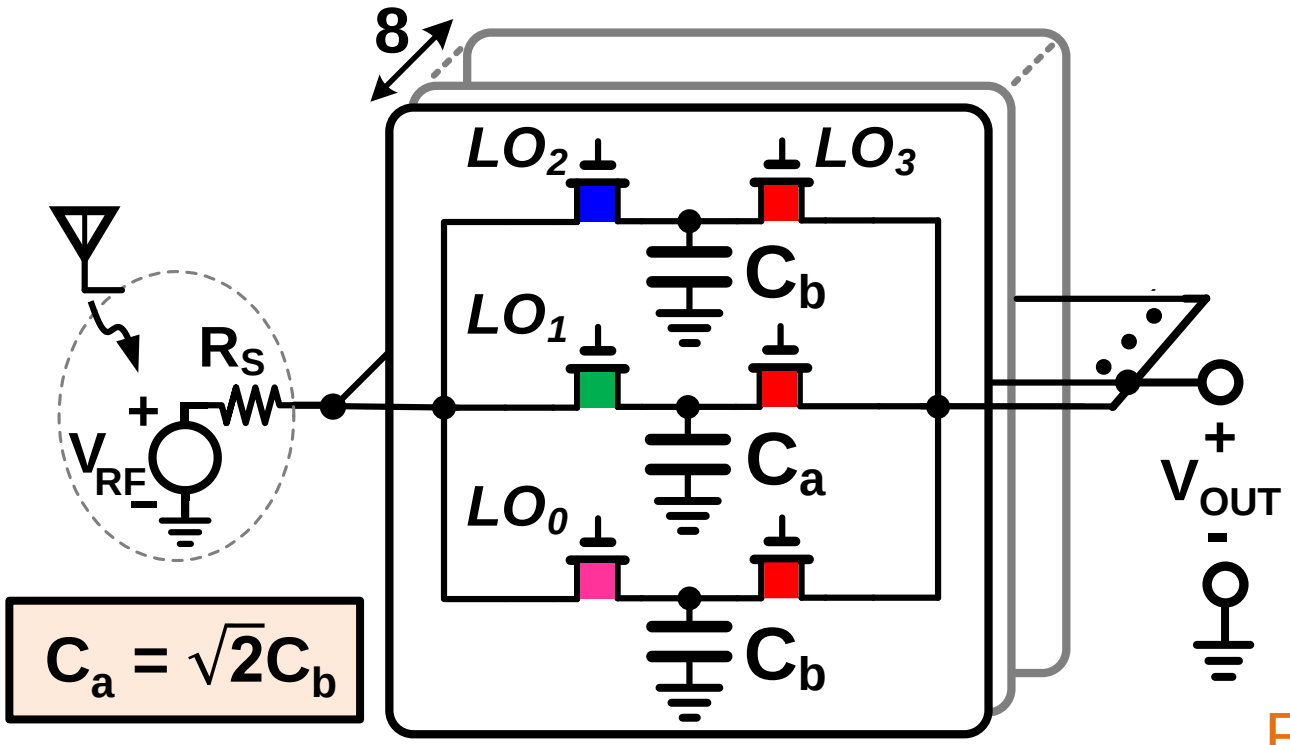


- Ideal **sensing** and **summation** of voltages stored on BB capacitors are required.
- Would it be feasible to implement them using only **passive** elements (Switch-C)?

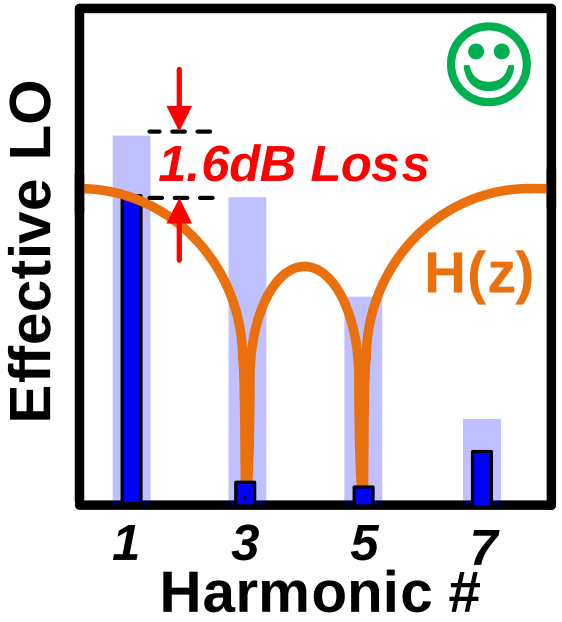
Outline

- Motivation and Introduction
- **Switch-Capacitor Harmonic Rejection Approaches**
- Circuit Implementation
- Measurement Results
- Conclusion

HR via Charge Sharing



$C_a = \sqrt{2}C_b$

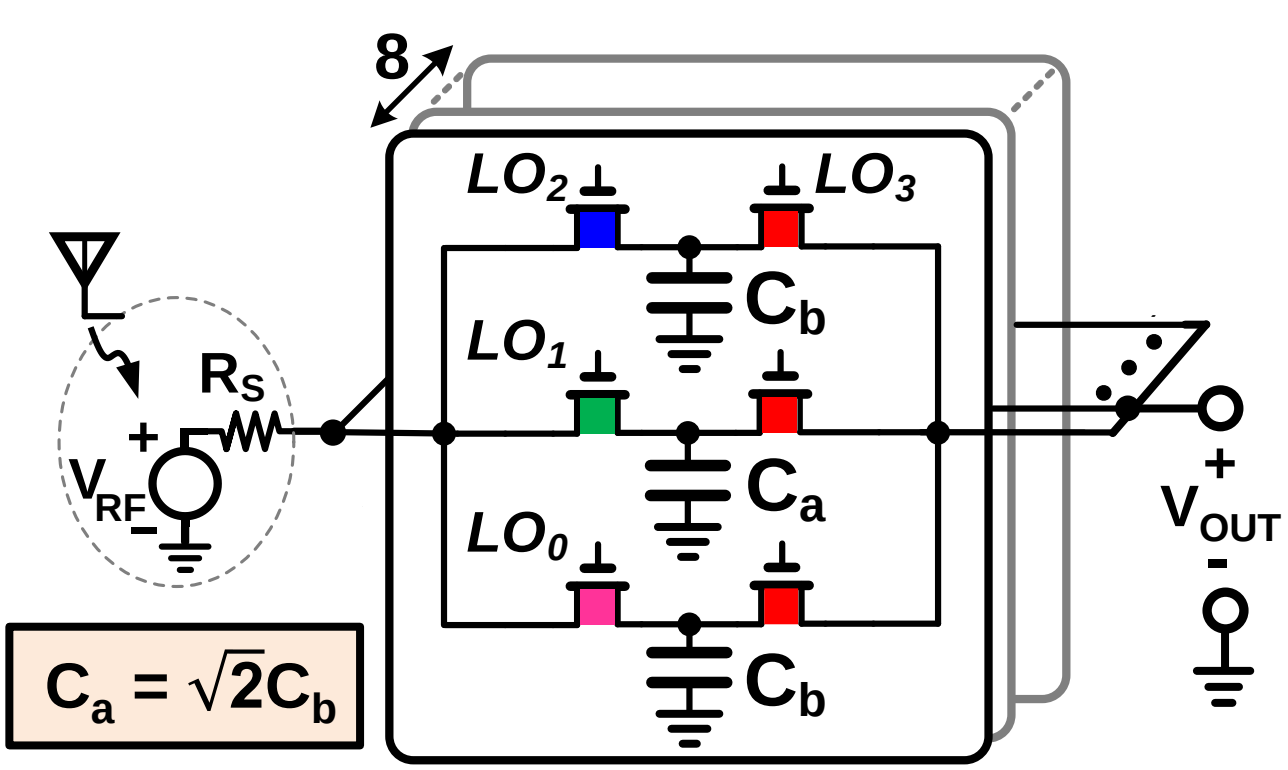


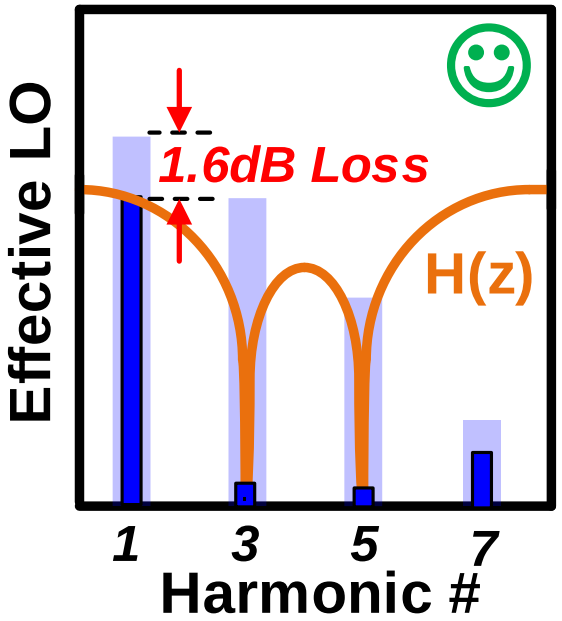
Realized FIR Filter

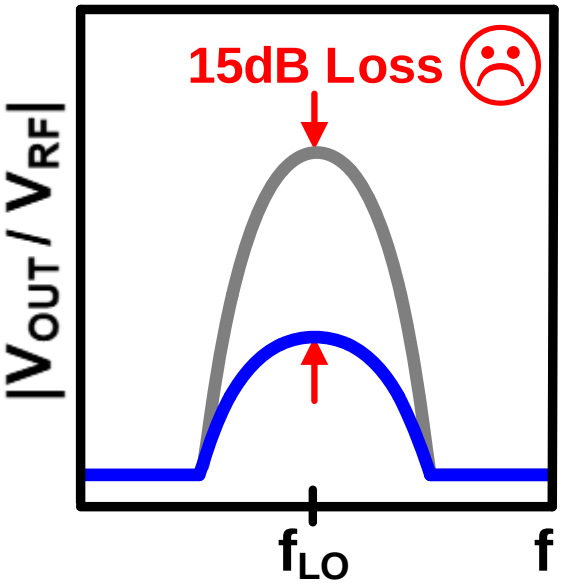
$$H(z)=\frac{1+\sqrt{2}z^{-1}+z^{-2}}{2+\sqrt{2}}$$

☺ HR is achievable with capacitor weighting.

HR via Charge Sharing

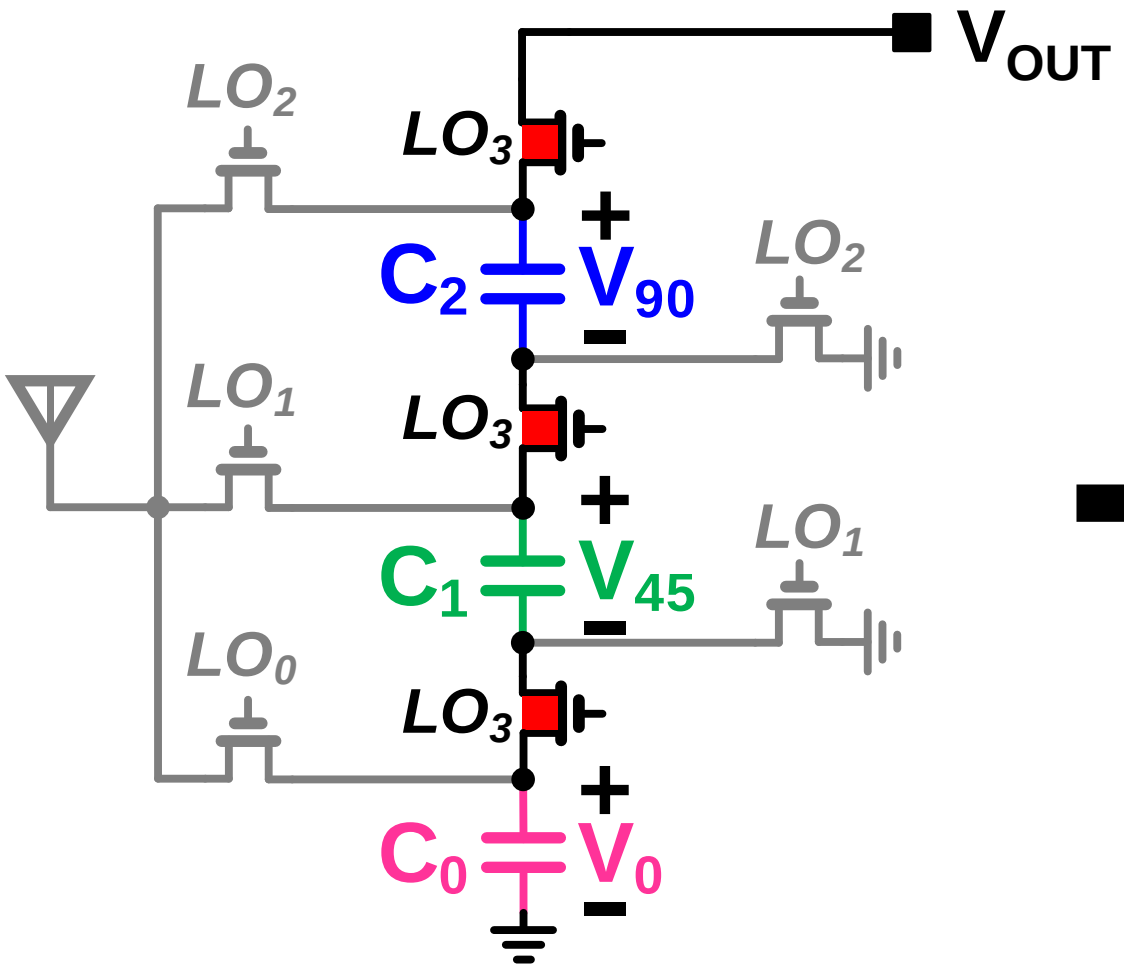


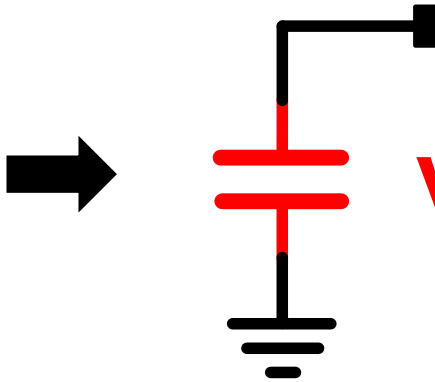




☺ HR is achievable with capacitor weighting.
☹ Extremely high insertion loss

HR via Capacitor Stacking

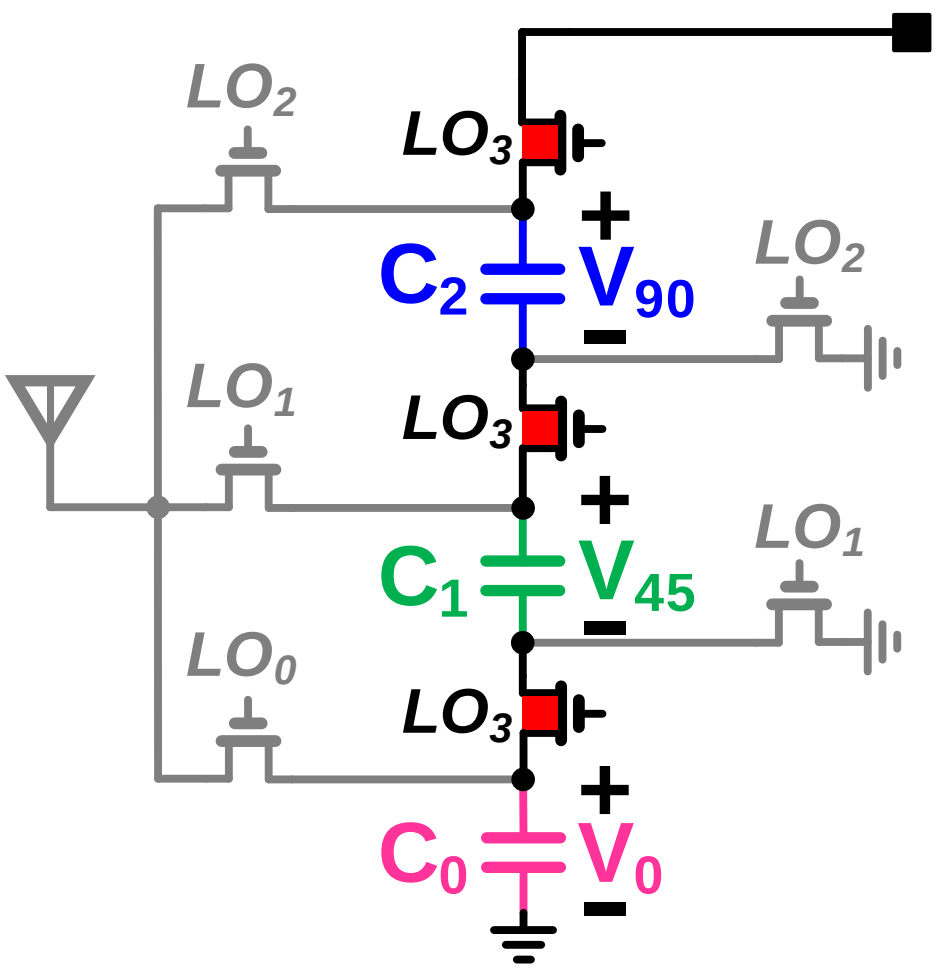




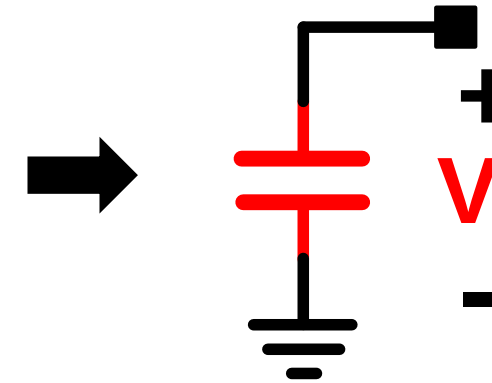
$$V_{eq} = V_0 + V_{45} + V_{90}$$

$$H_{FIR}(z) = 1 + z^{-1} + z^{-2}$$

HR via Capacitor Stacking



The 2nd tap should be $\sqrt{2}$ for the purpose of harmonic rejection

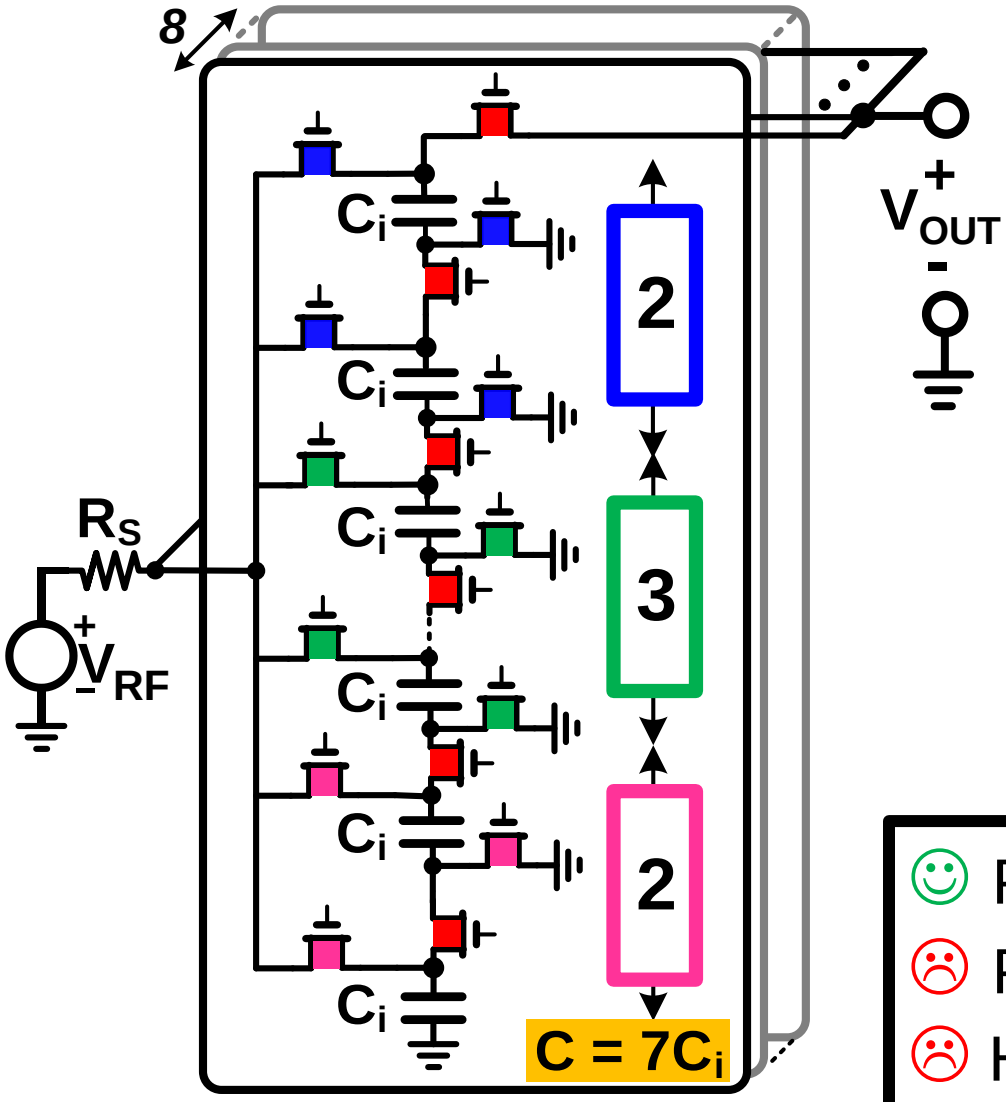


$$V_{eq} = V_0 + V_{45} + V_{90}$$

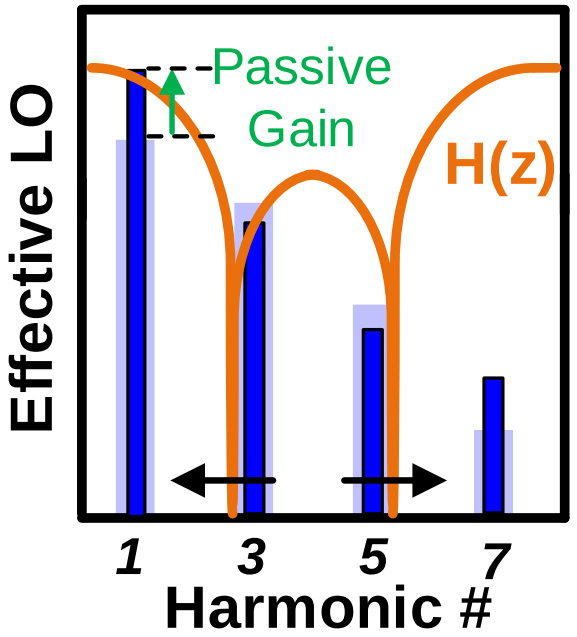
$$H_{FIR}(z) = 1 + z^{-1} + z^{-2}$$

The realized FIR filter is independent of capacitor values.

HR via Capacitor Stacking



1:$\sqrt{2}$:1 approximated by 2:3:2

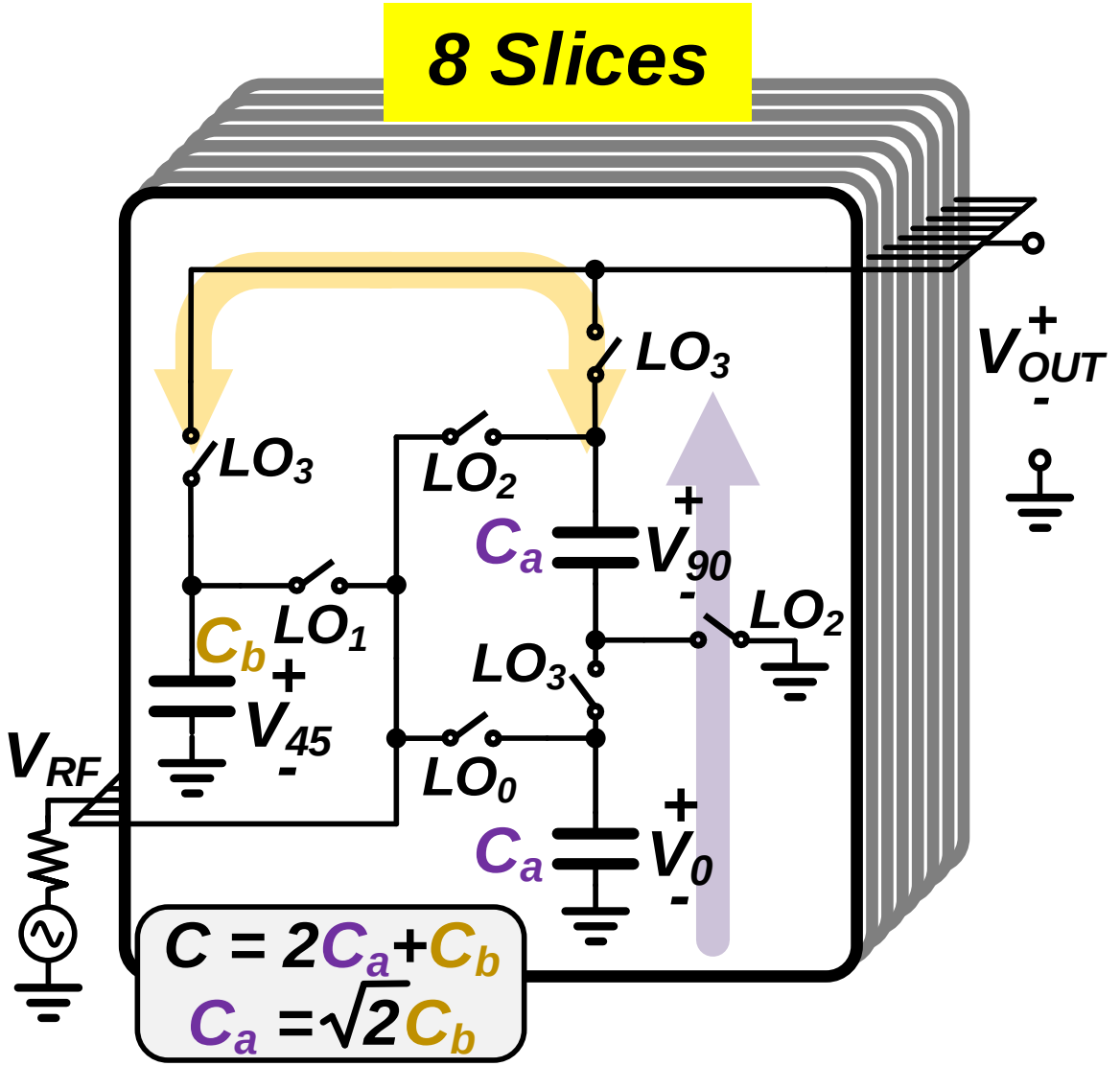


Realized FIR Filter $H(z) = 2 + 3z^{-1} + 2z^{-2}$

- ☺ Passive gain achievable
- ☹ Poor HR performance
- ☹ High susceptibility to intermediate parasitic caps

Hybrid Filtering Design

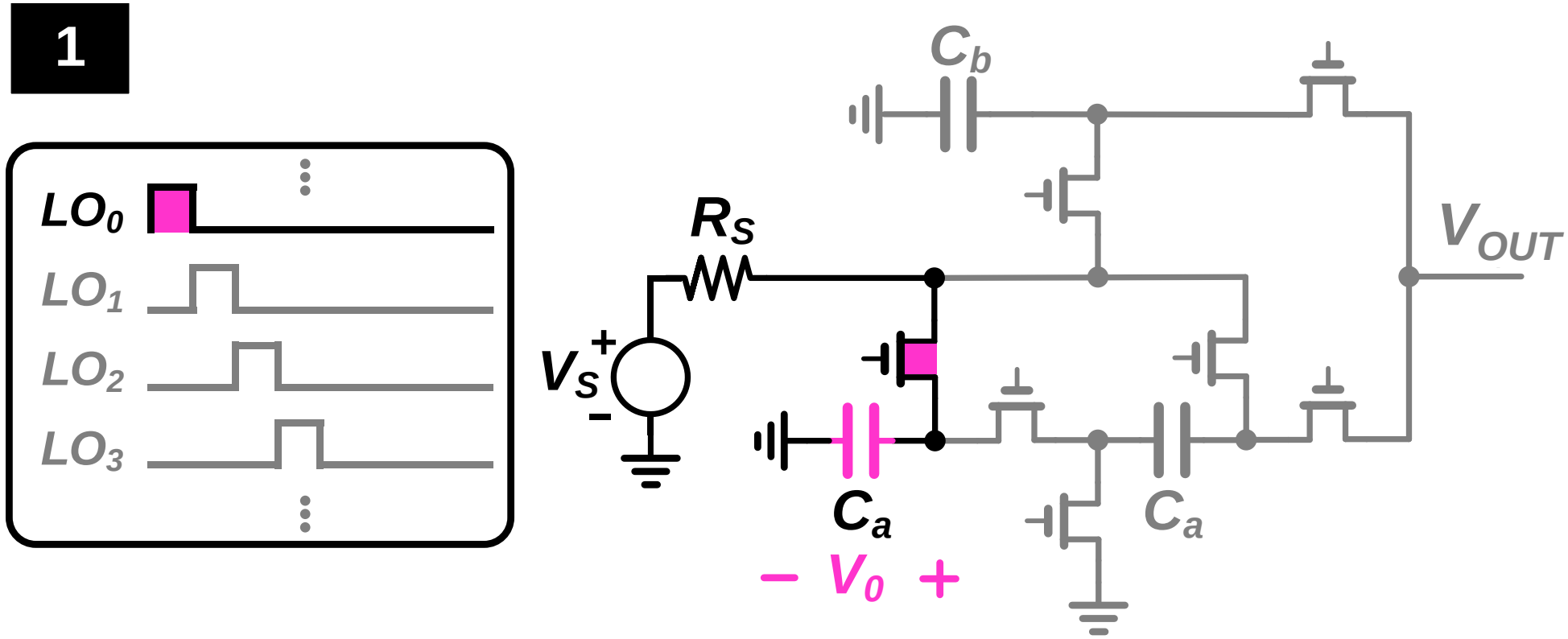
- **Charge Sharing**
  - Precise Harmonic Rejection
  - Lossy
- **Capacitor Stacking**
  - Poor Harmonic Rejection
  - Passive Gain



Outline

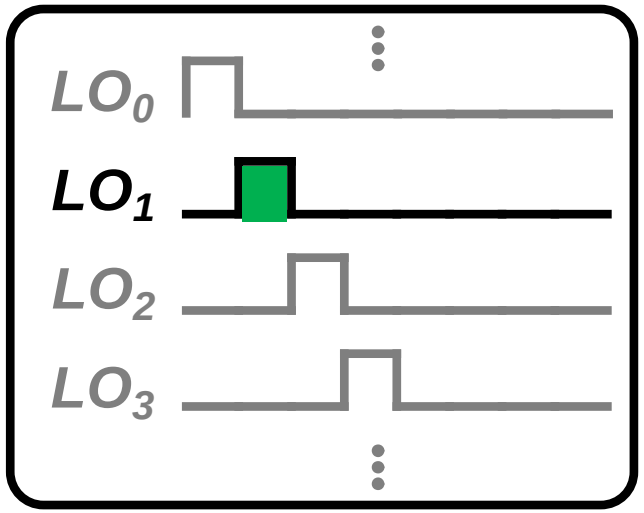
- Motivation and Introduction
- Switch-Capacitor Harmonic Rejection Methods
- **Circuit Implementation**
- Measurement Results
- Conclusion

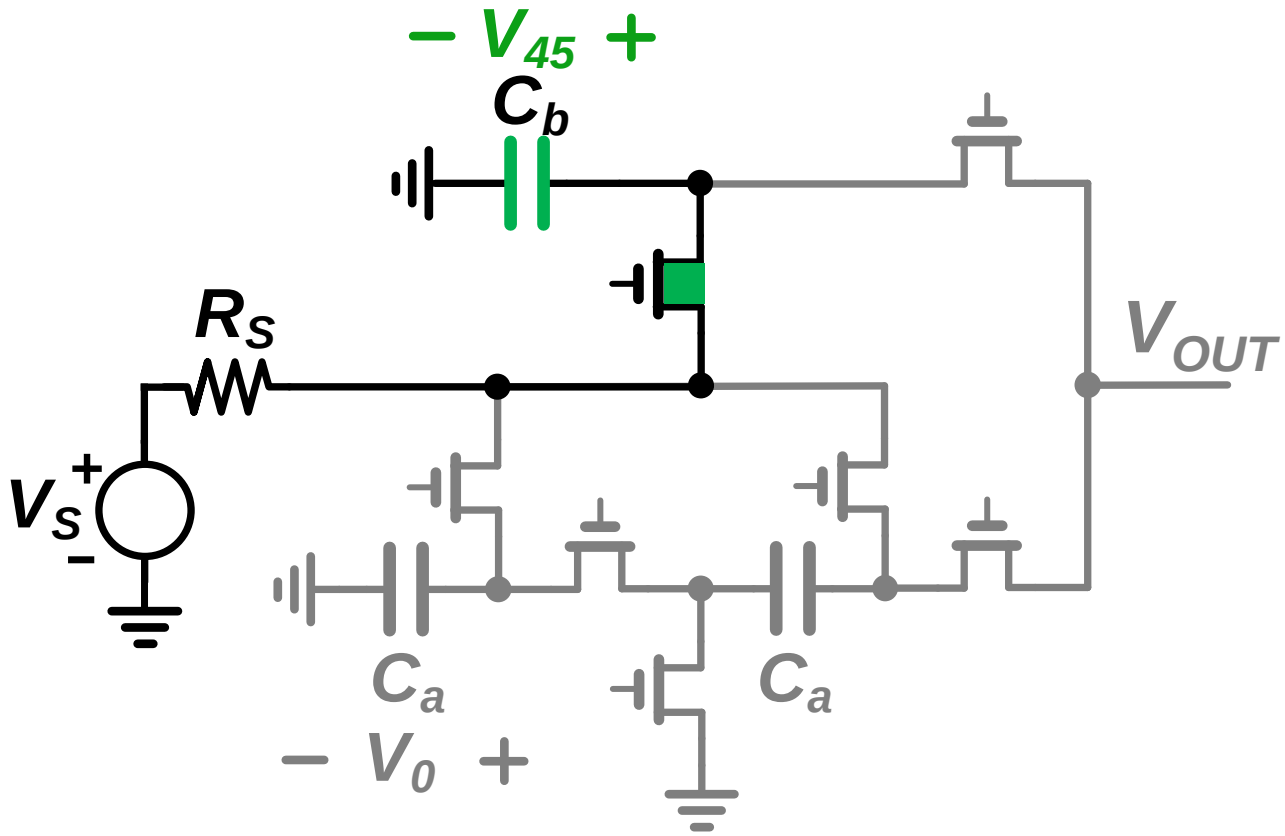
Sampling/Filtering Phase



Sampling/Filtering Phase

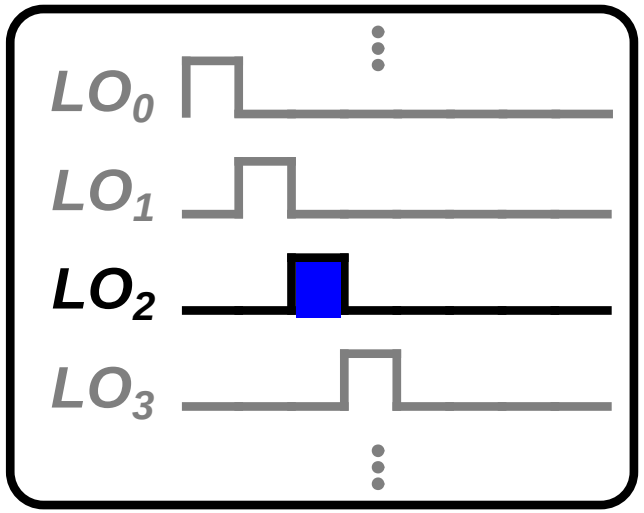
2

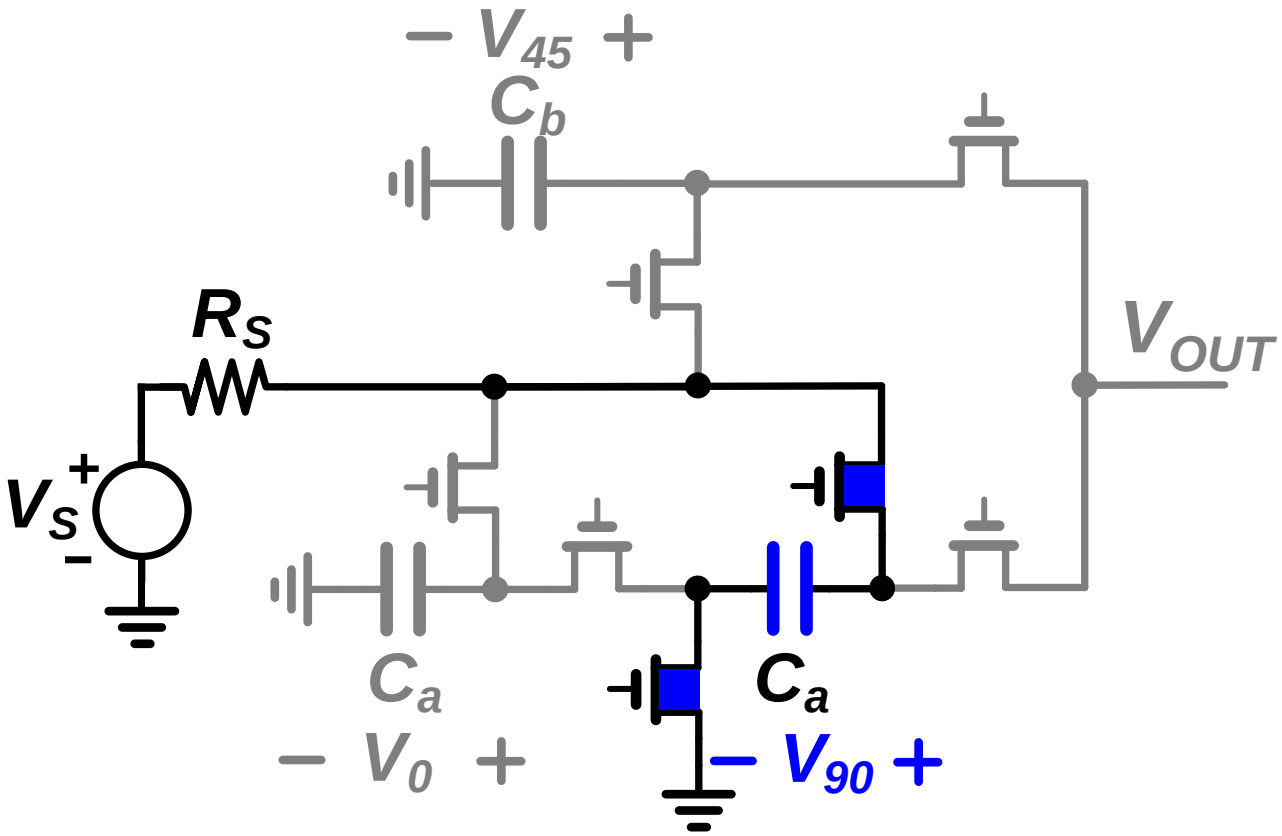




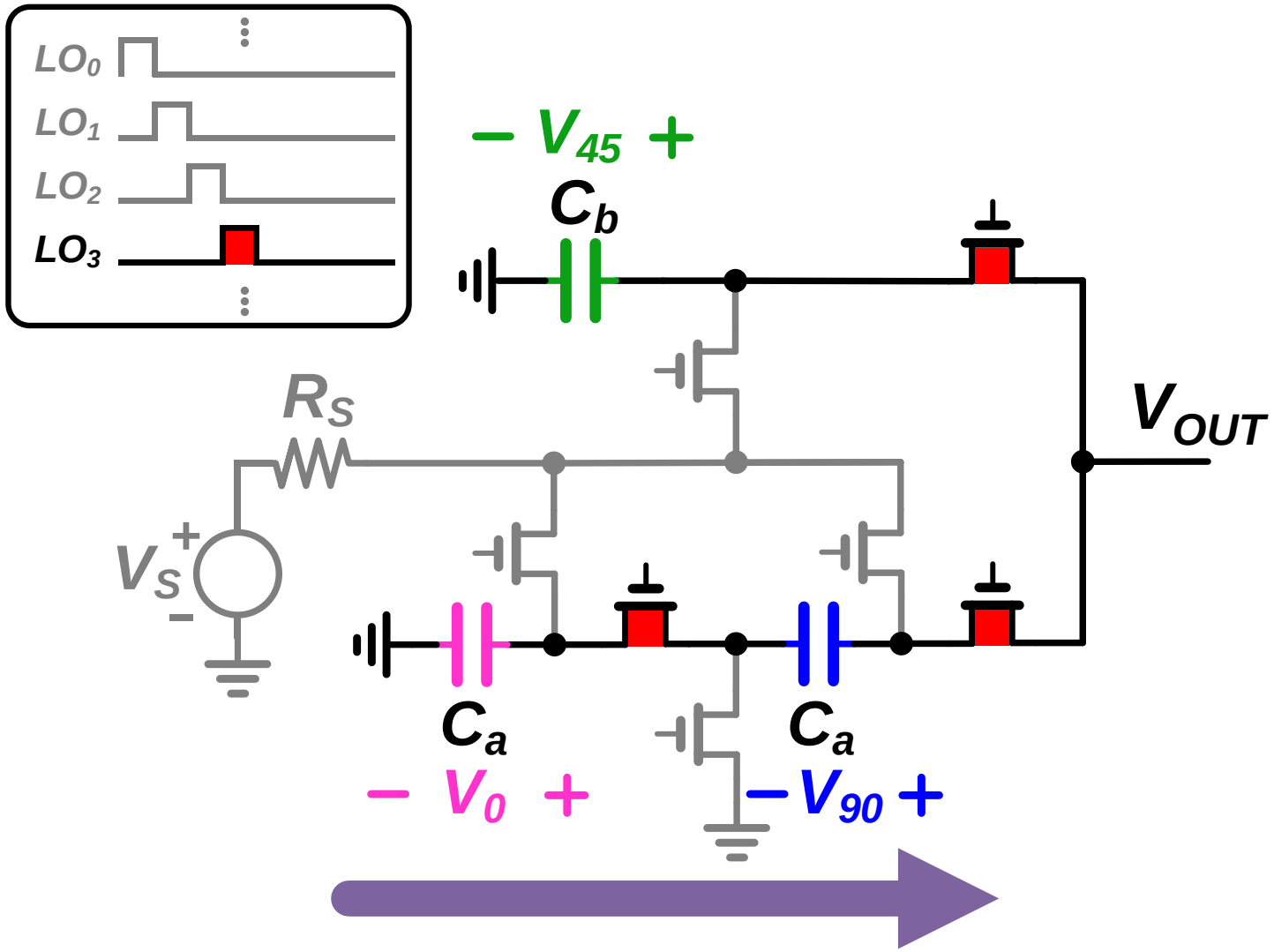
Sampling/Filtering Phase

3



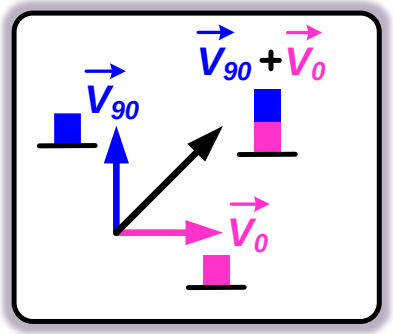


Read-out Phase



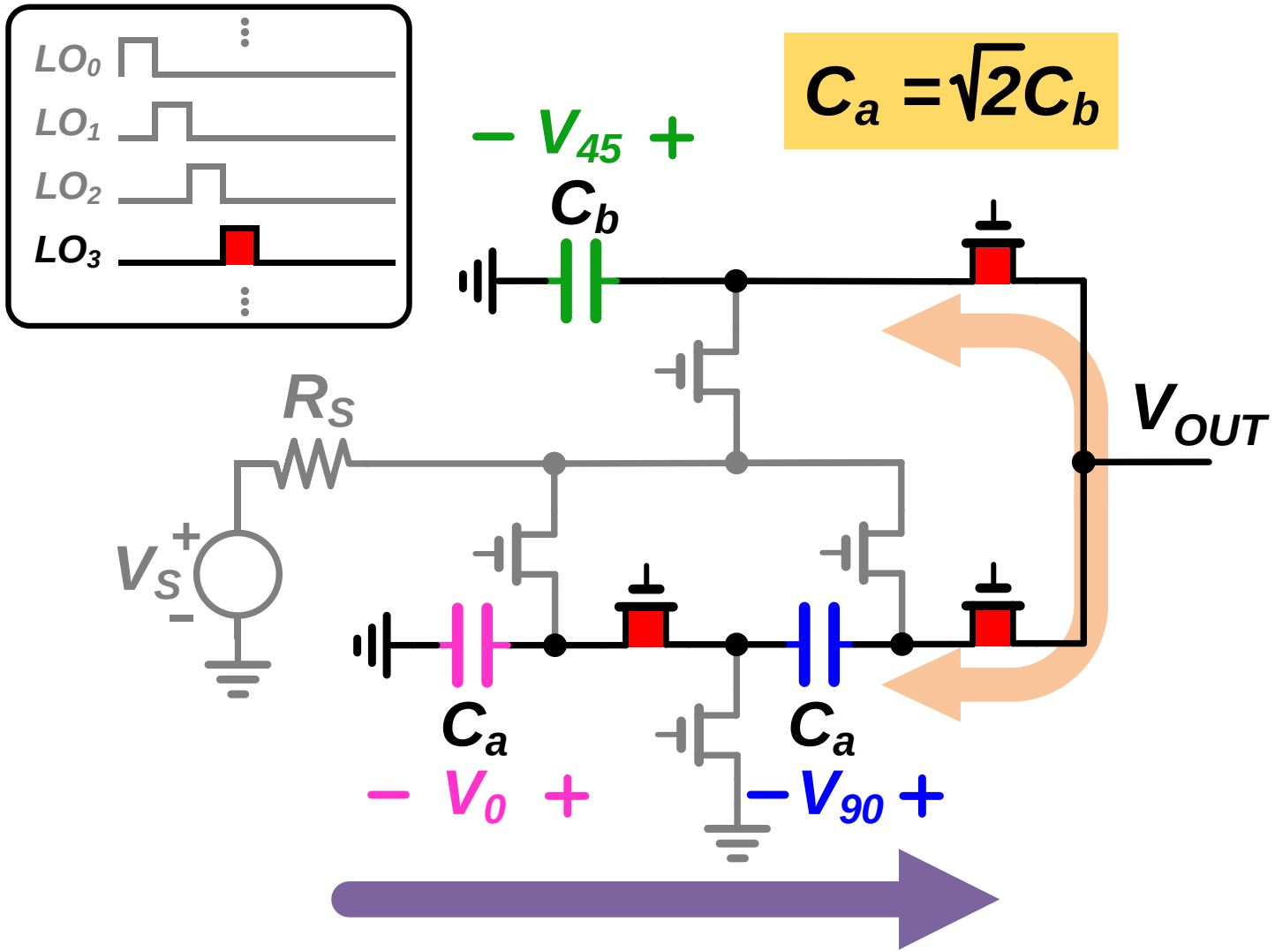
Capacitor Stacking

@ f_{LO}



$$H_{FIR}(z)=\frac{1+\sqrt{2}z^{-1}+z^{-2}}{1+\sqrt{2}}$$

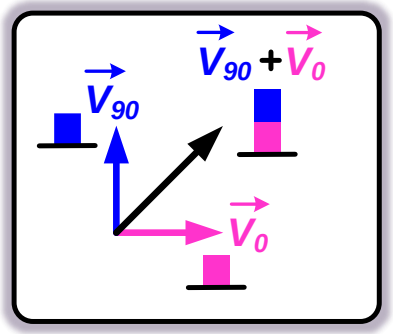
Read-out Phase

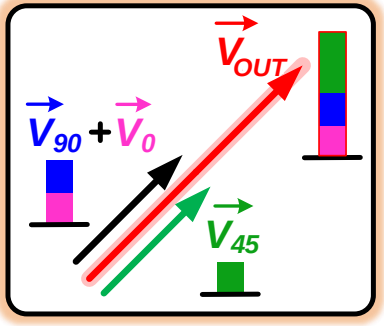


Capacitor Stacking

Charge Sharing

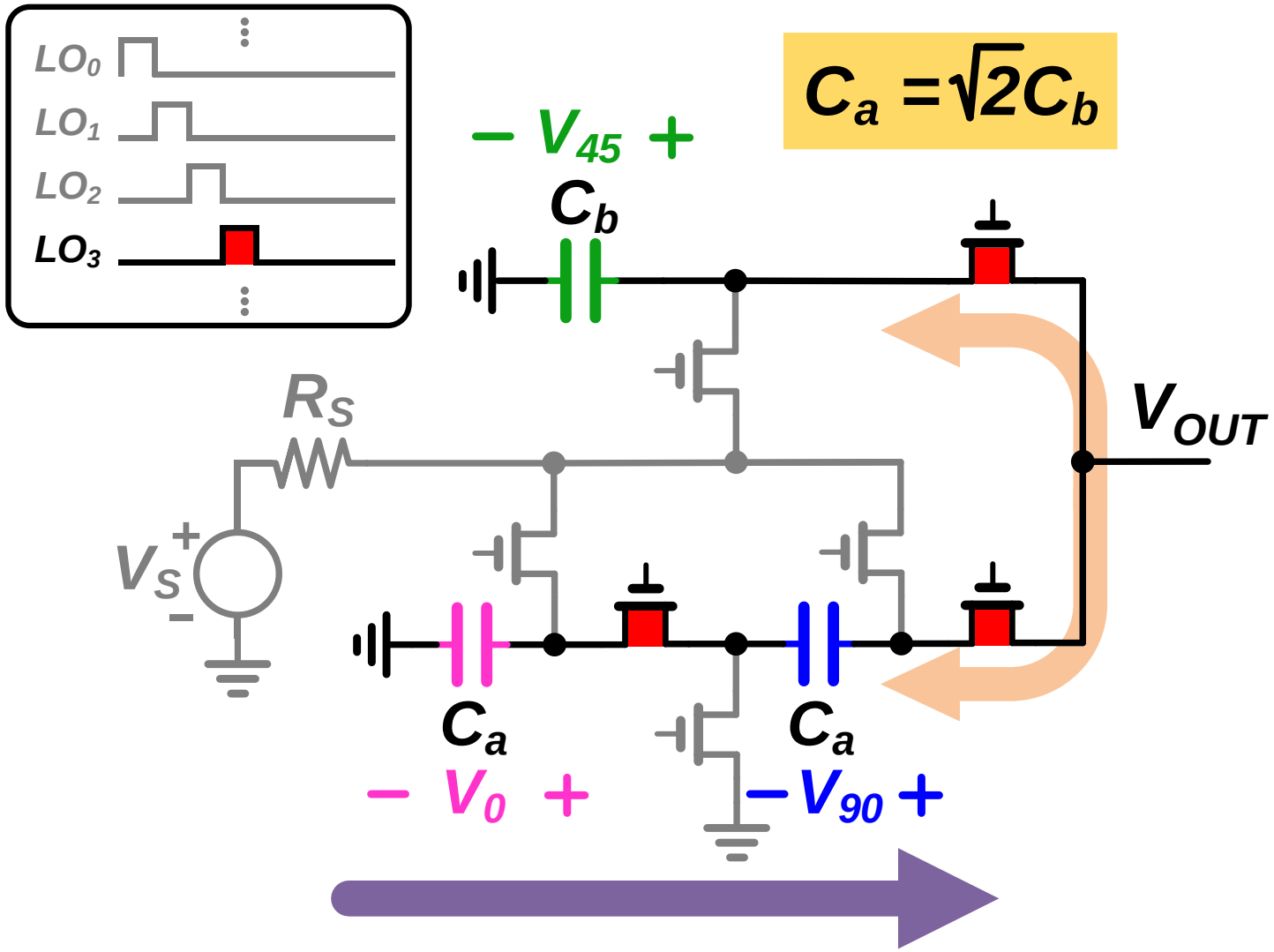
@ fLO

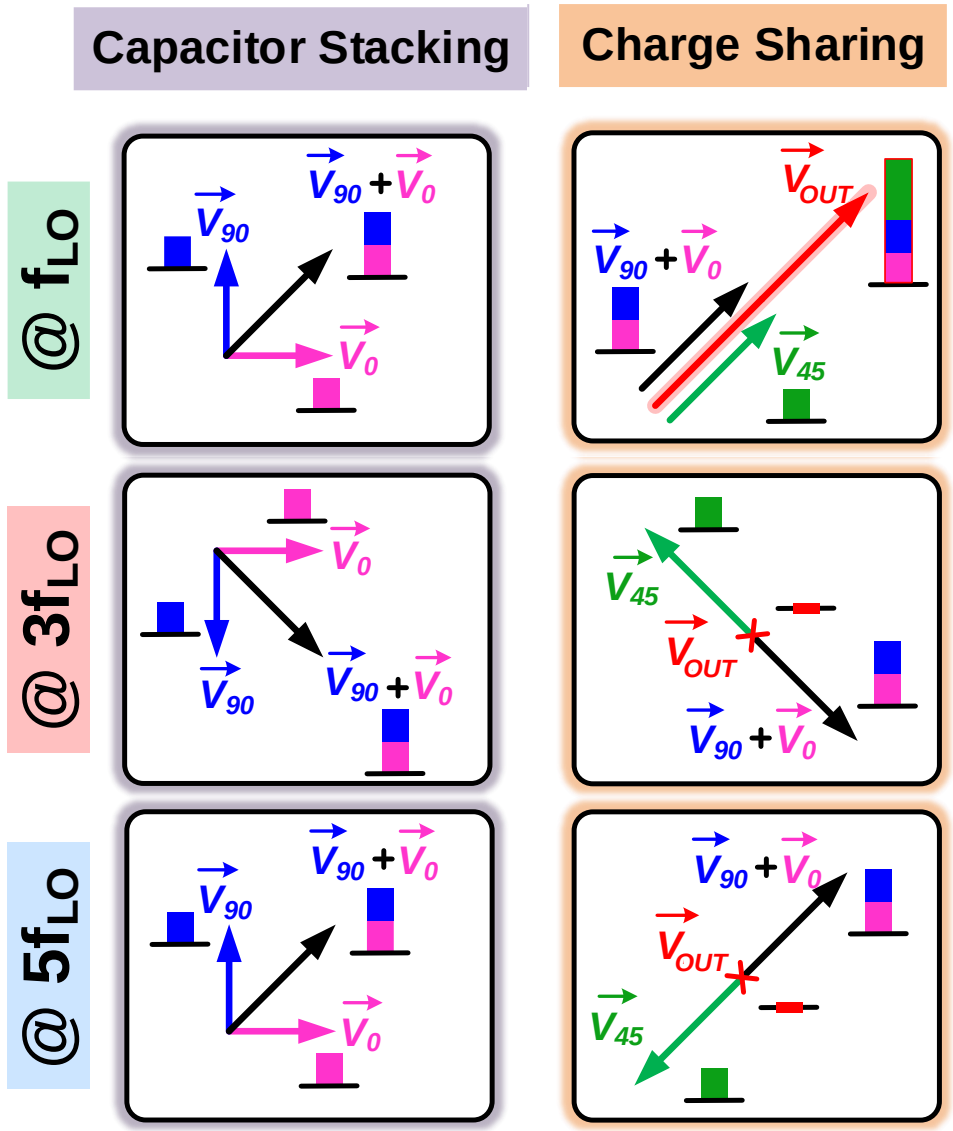




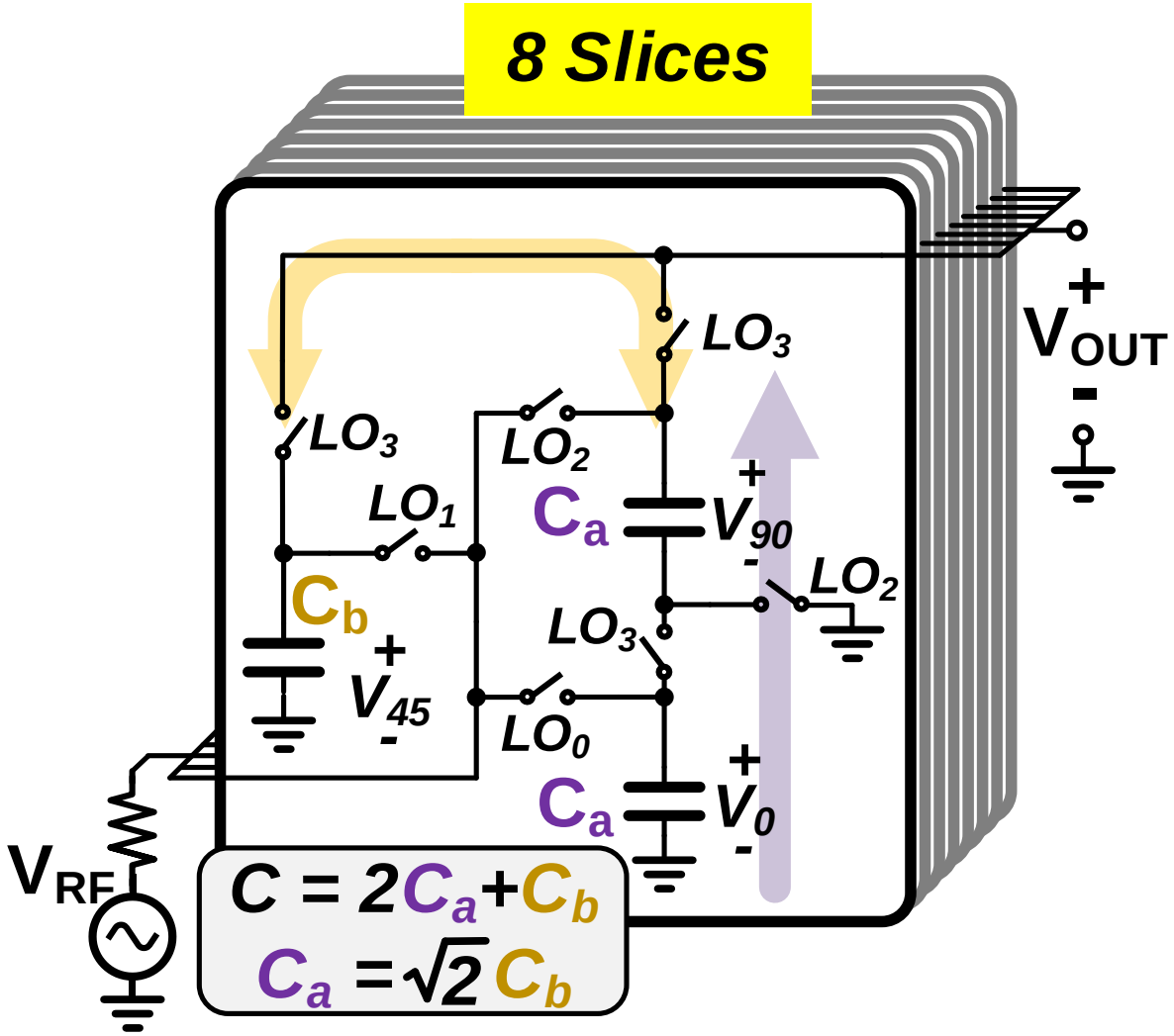
$$H_{FIR}(z)=\frac{1+\sqrt{2}z^{-1}+z^{-2}}{1+\sqrt{2}}$$

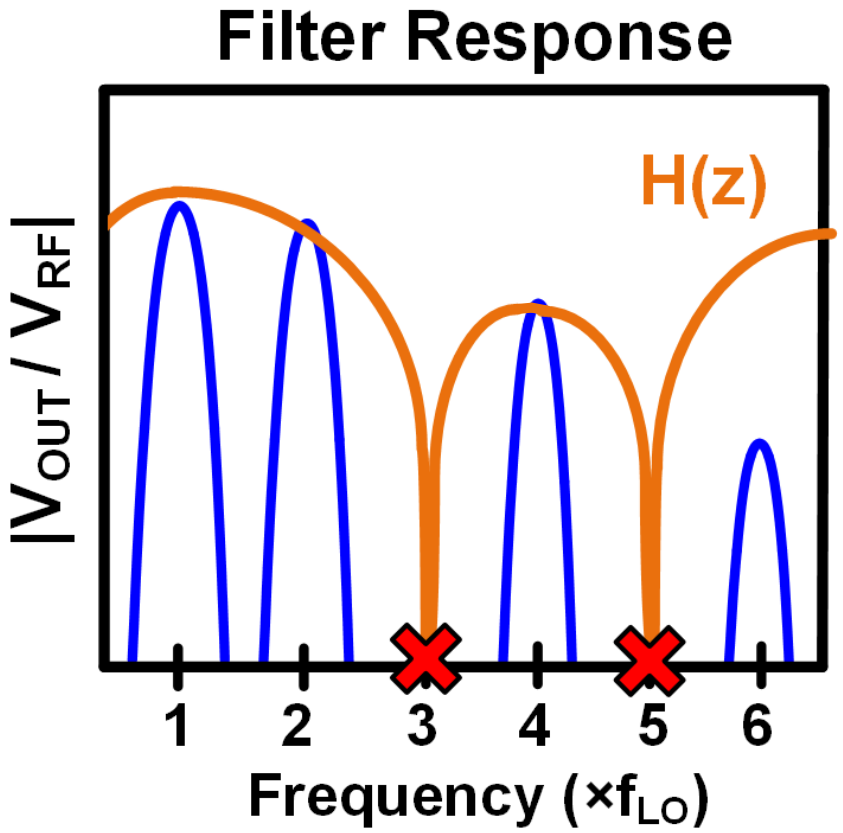
Read-out Phase





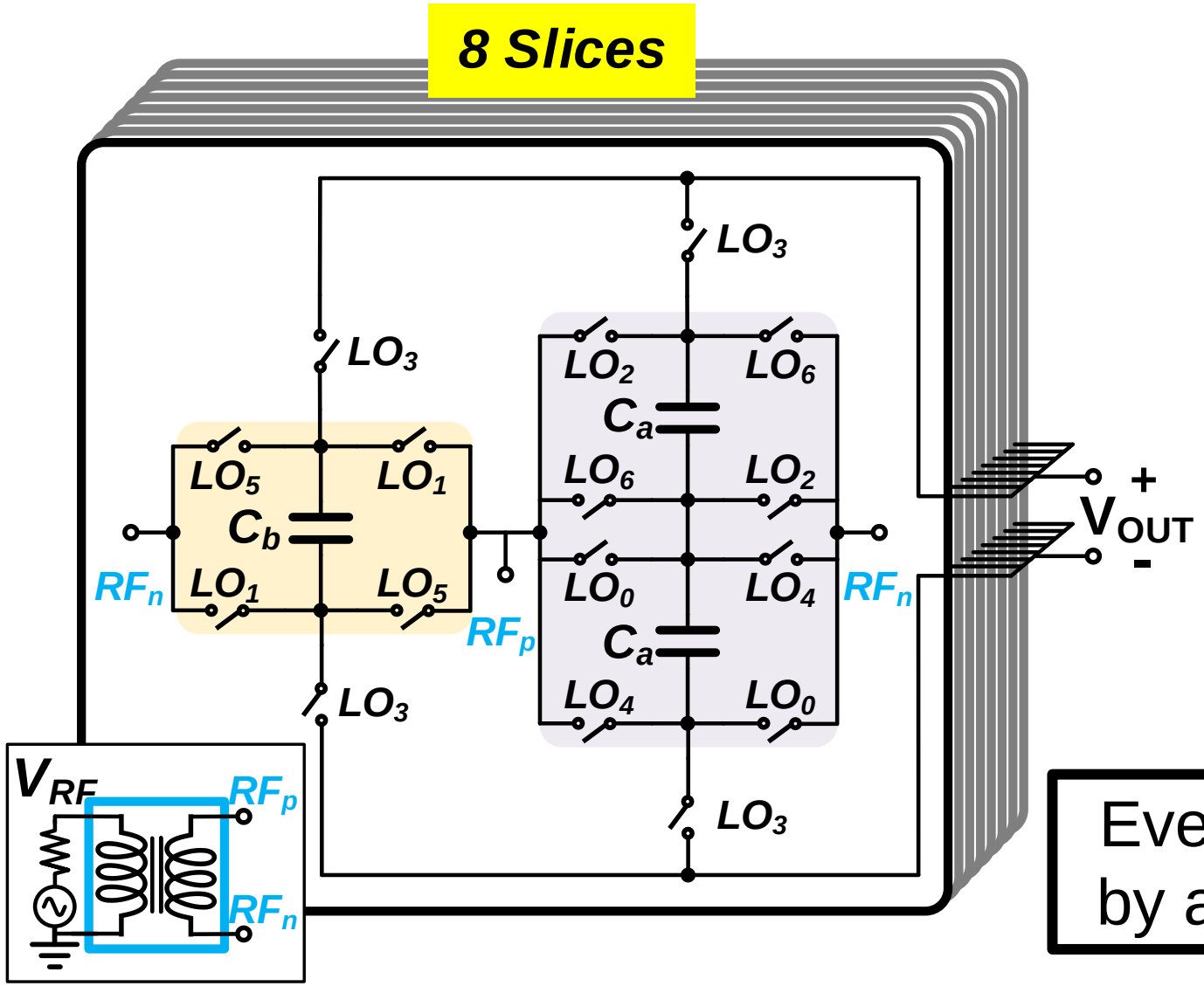
Proposed Architecture (I)

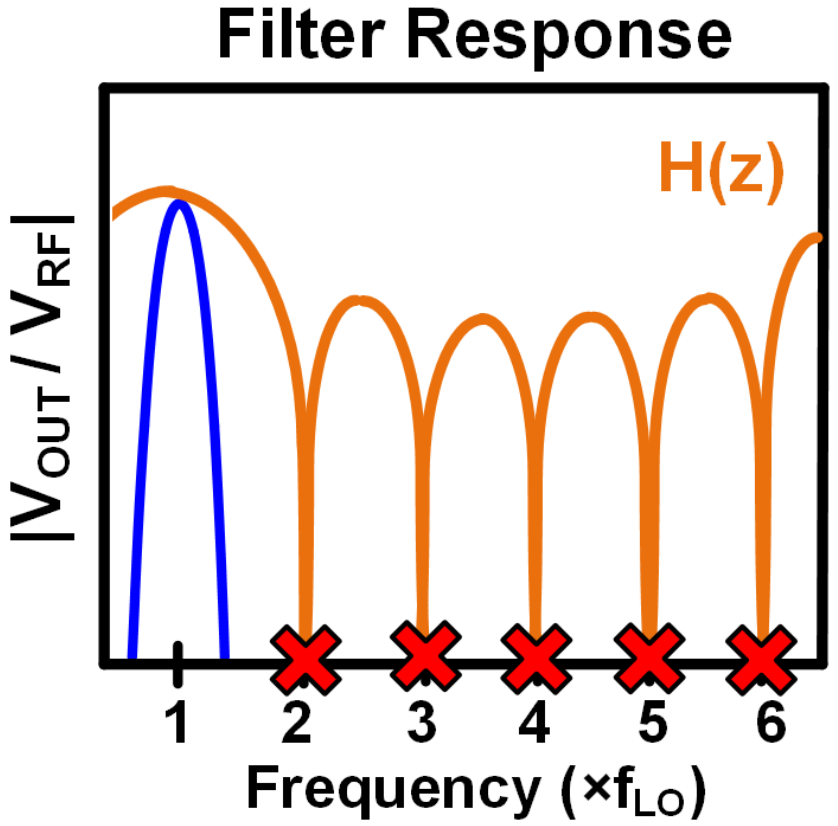




Even harmonics are still problematic.

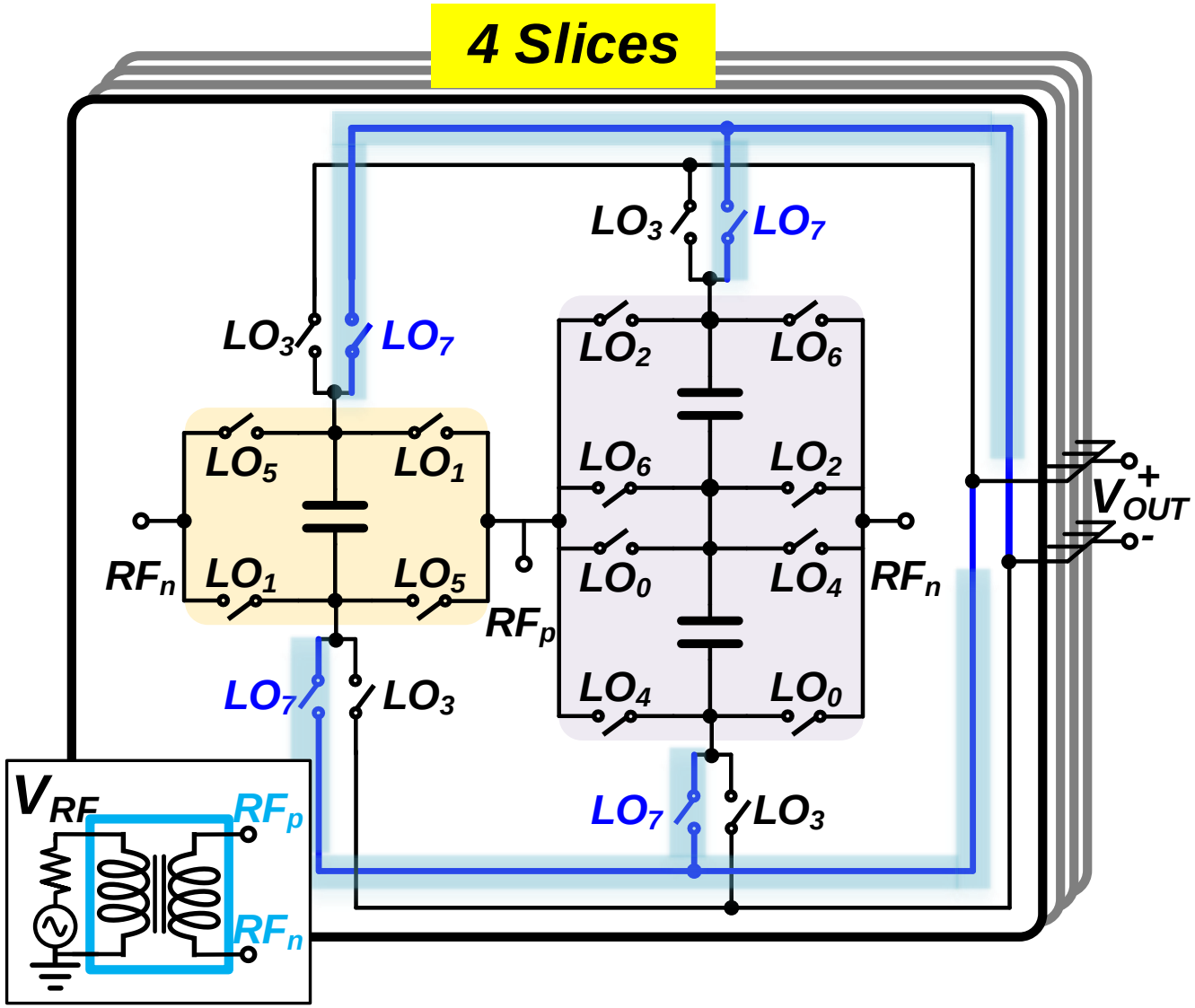
Proposed Architecture (II)

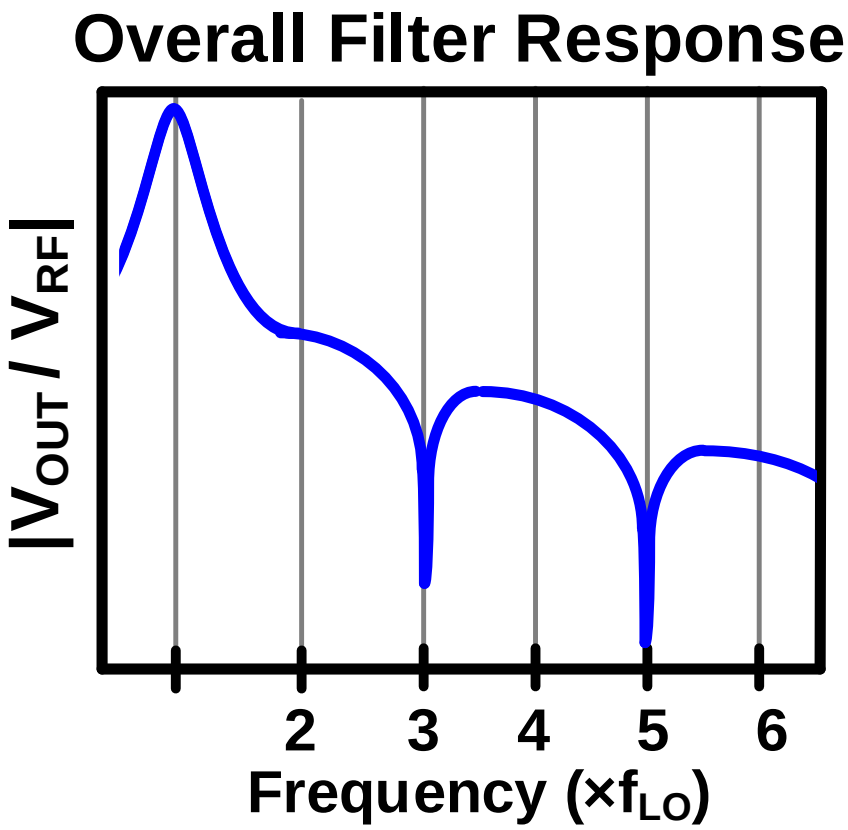




Even harmonic blockers are filtered by antiphase switching of diff. input.

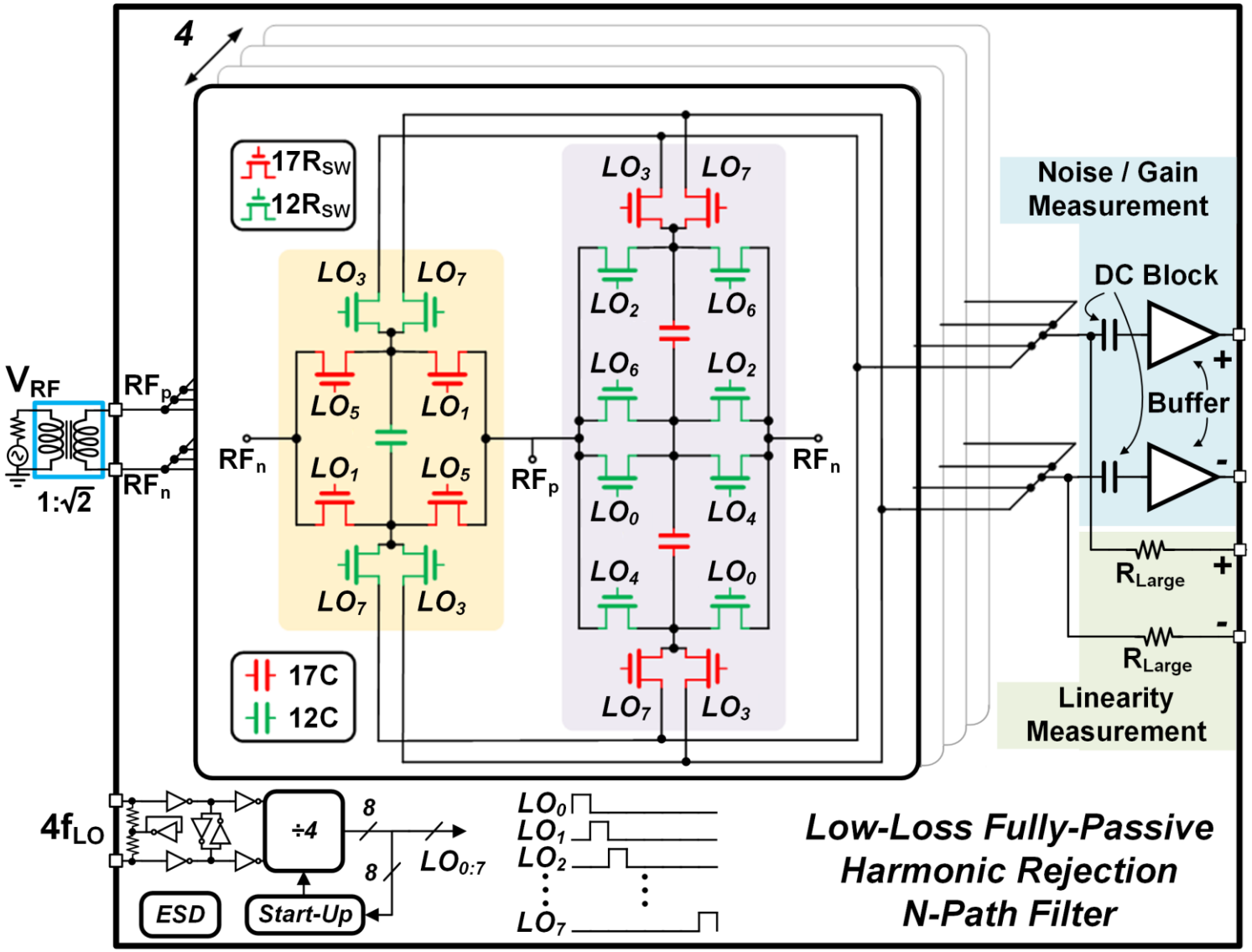
Proposed Architecture (III)





Share common Switches/Capacitors

System Block Diagram

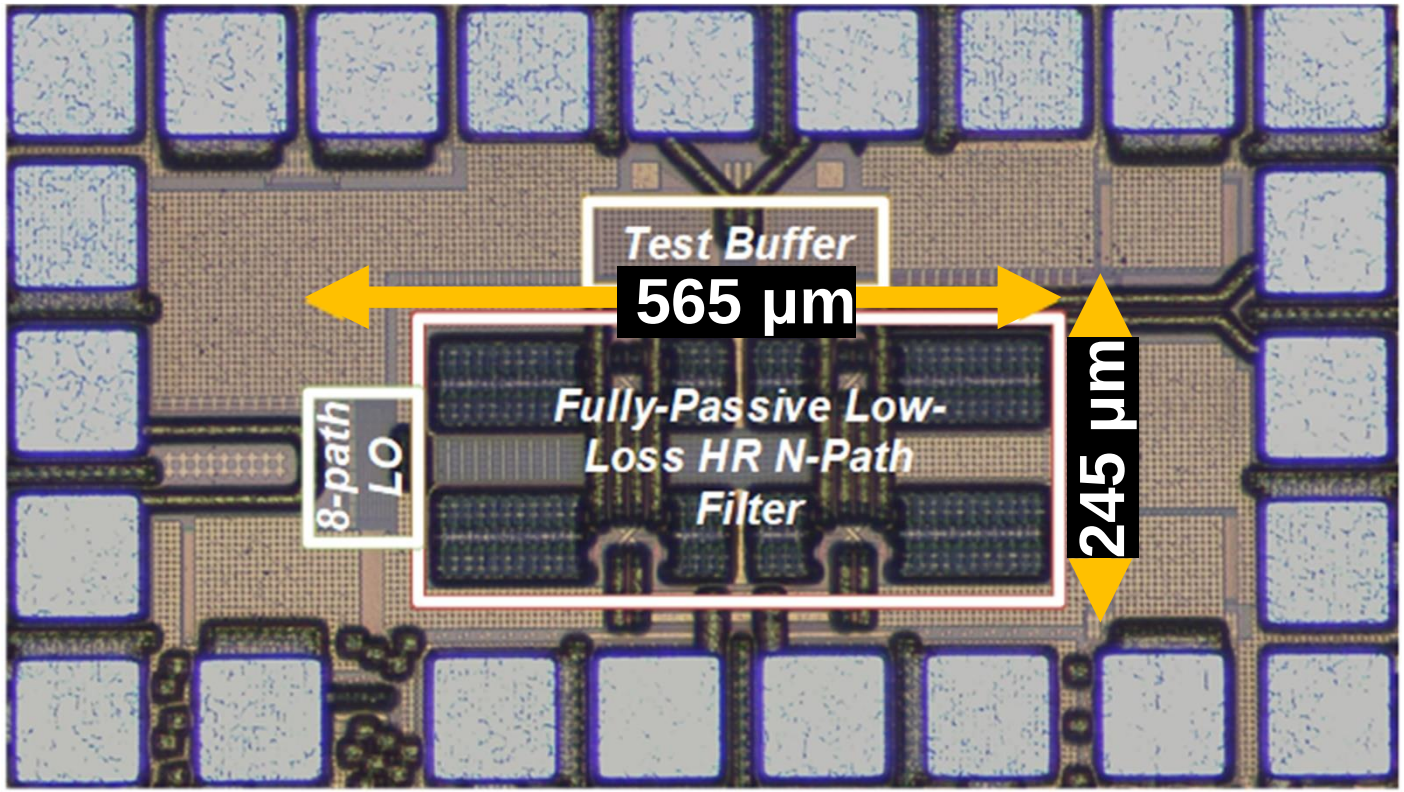


Outline

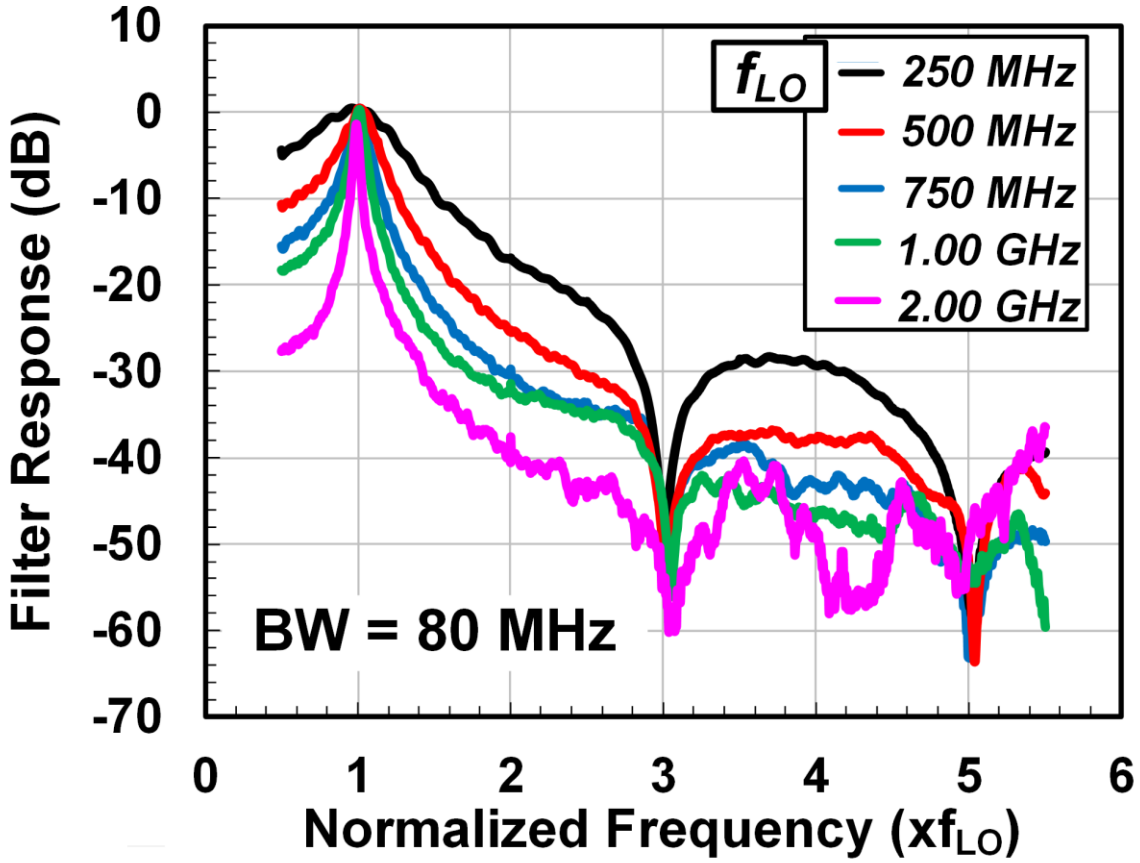
- Motivation and Introduction
- Switch-Capacitor Harmonic Rejection Methods
- Circuit Implementation
- **Measurement Results**
- Conclusion

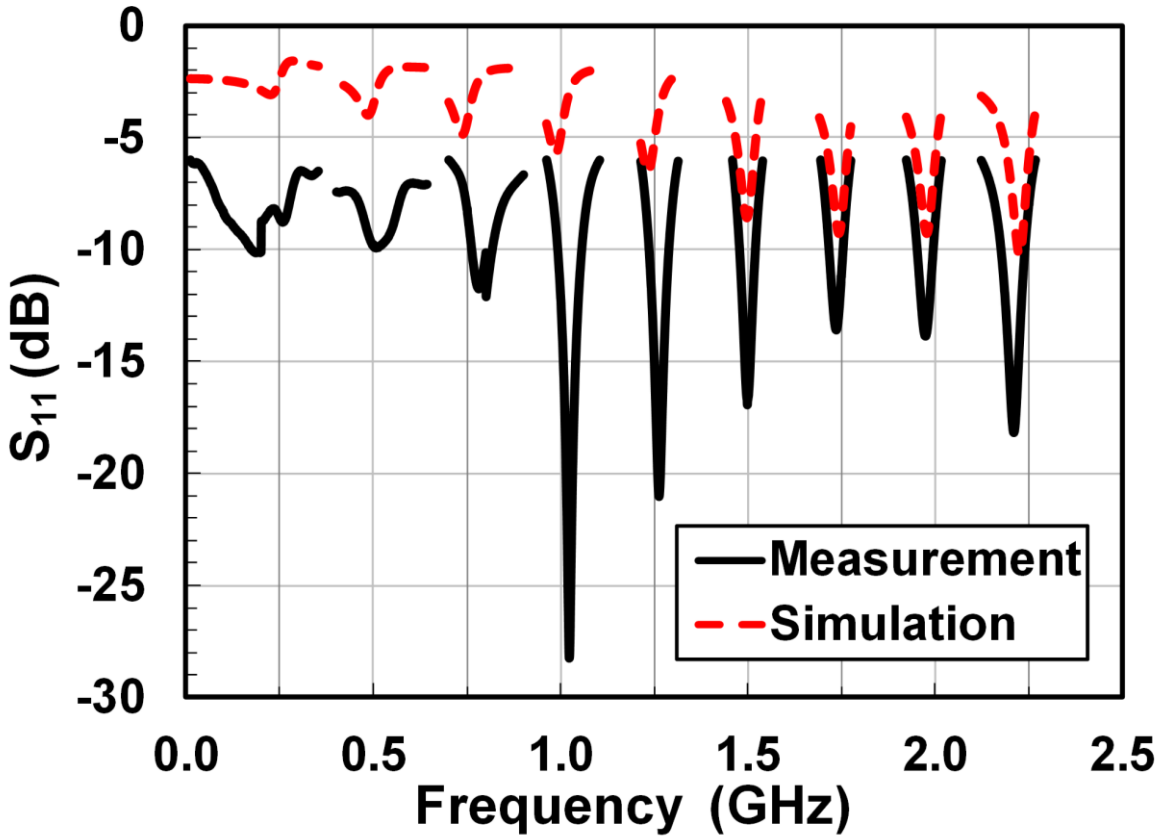
Die Micrograph

- **Technology**
  - 45nm SOI GlobalFoundries
- **Silicon Area**
  - 0.14 mm^2
- **Power Supply**
  - 1.1V



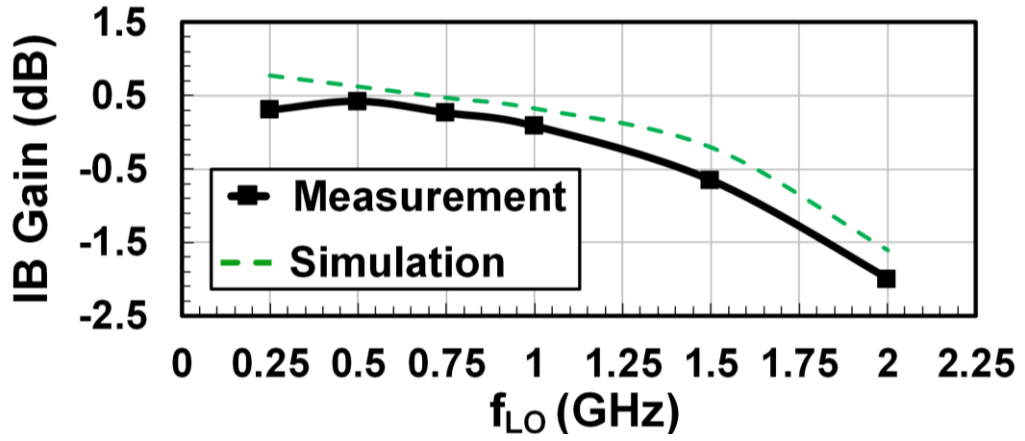
Measured Transfer Function and S_{11}

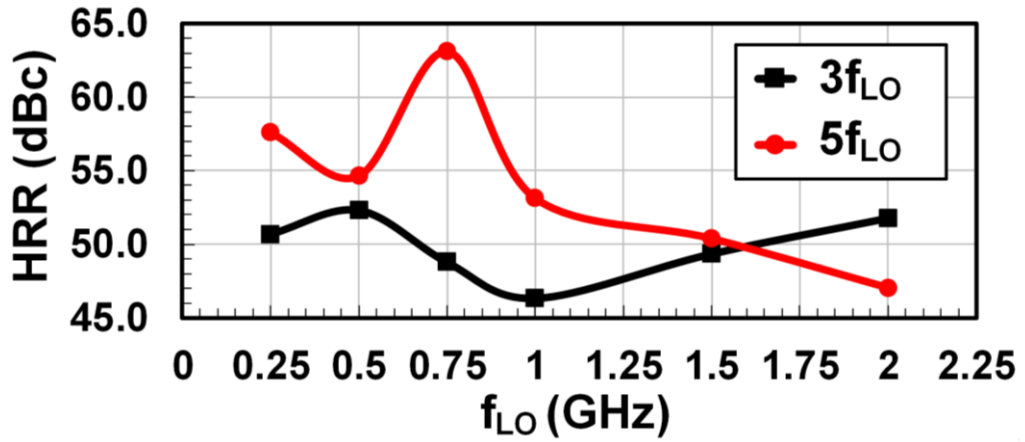


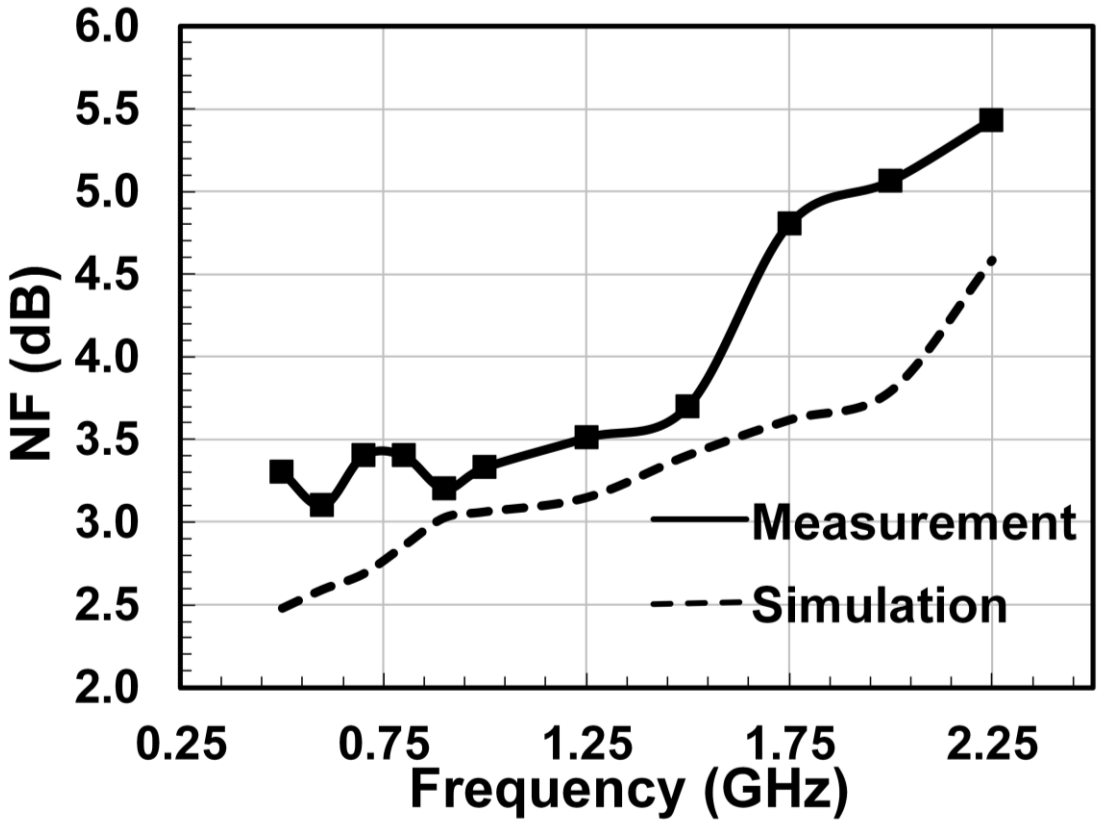


The receiver can be tuned across 250MHz-2.25GHz offering excellent 3rd/5th harmonic rejection

Measured Gain / HRR / NF



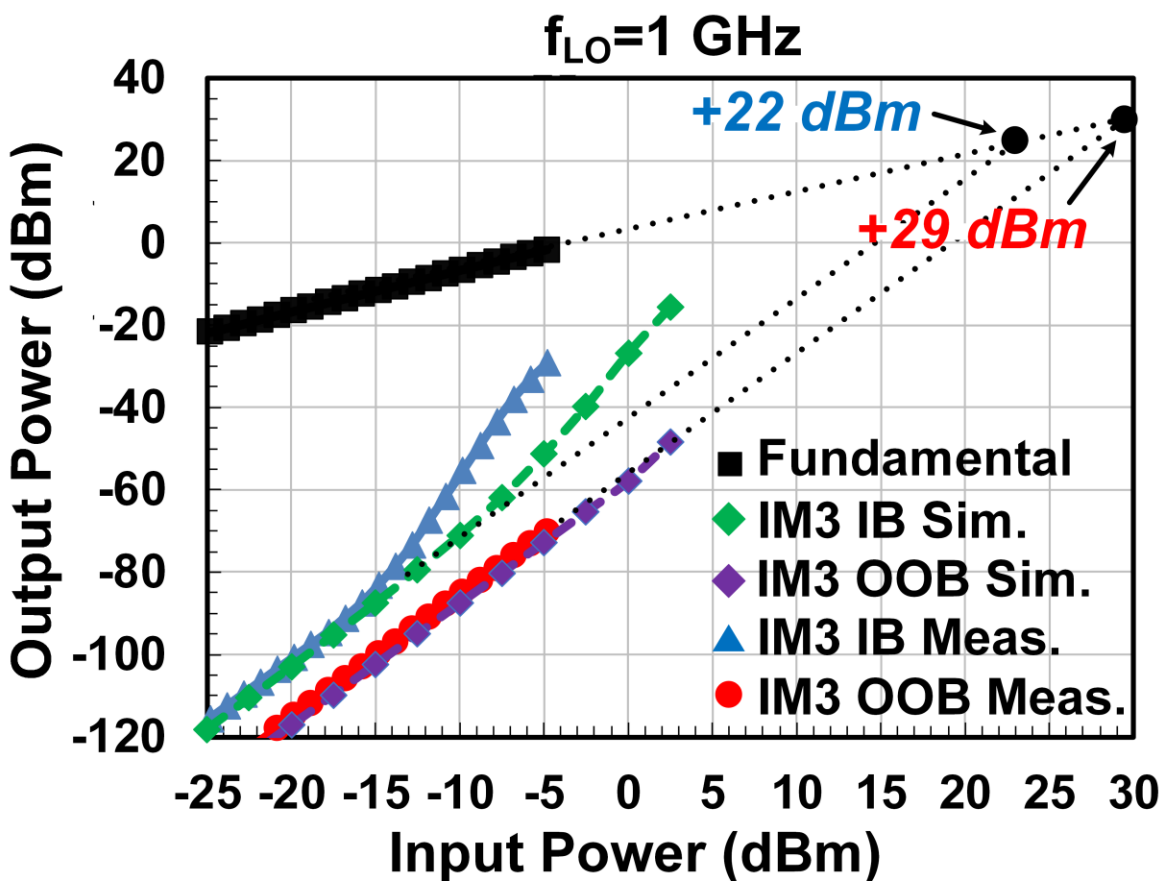


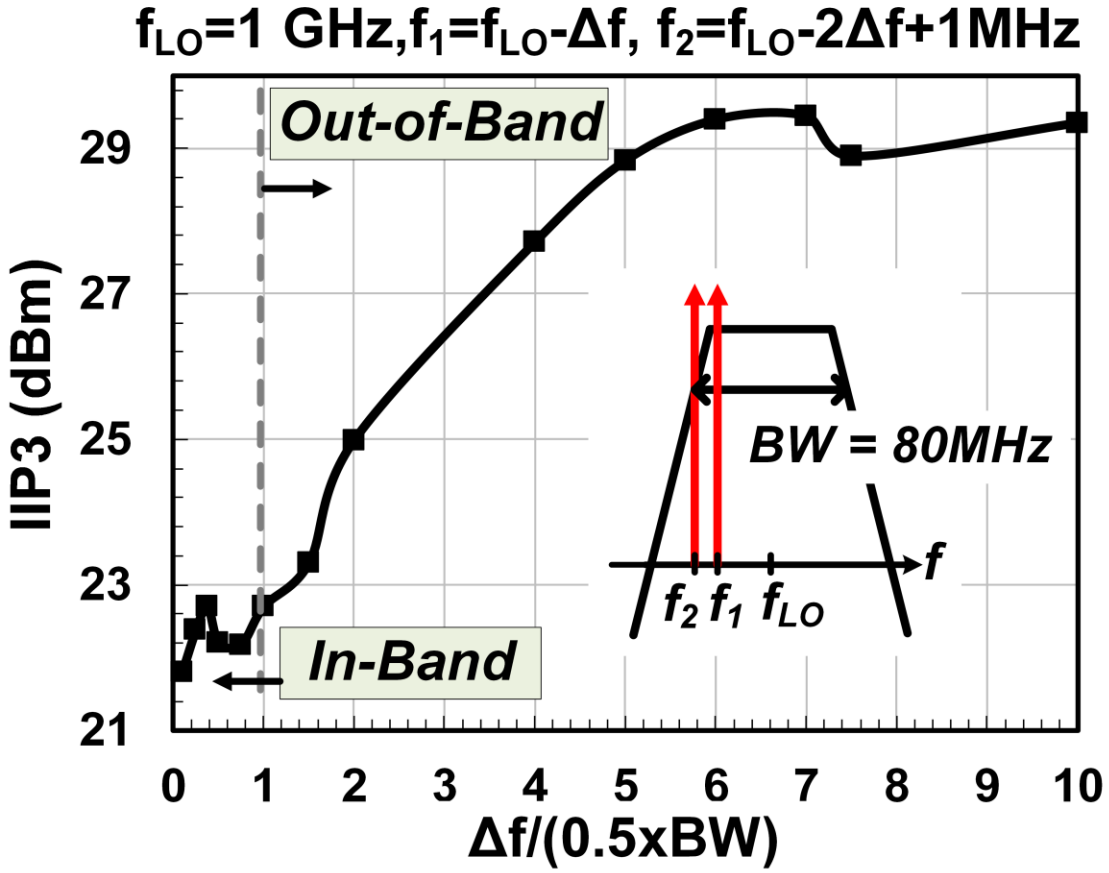


>46dB HRR3/HRR5 is obtained across operation frequency with low loss

The NF at 750MHz is 3.4dB and increases with frequency

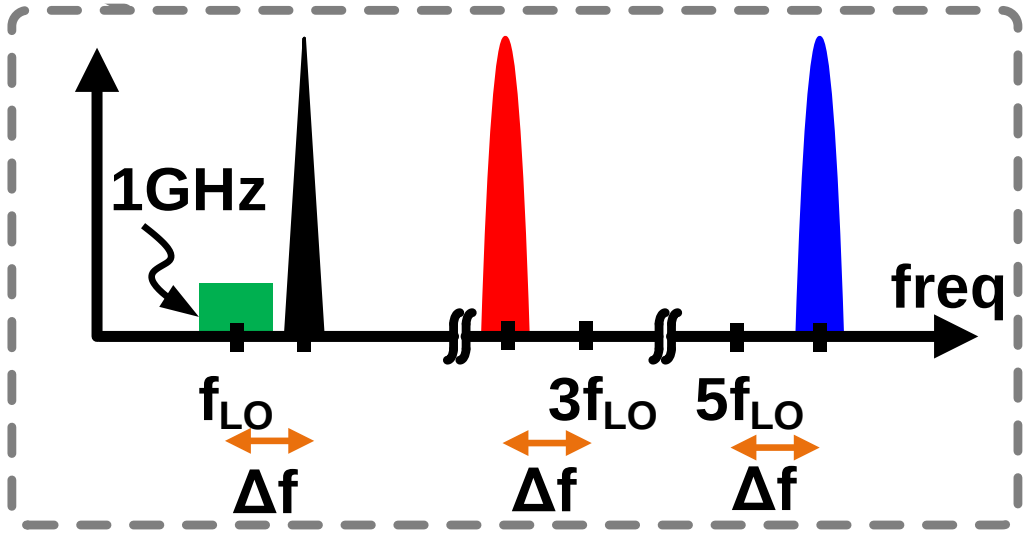
Measured IIP3

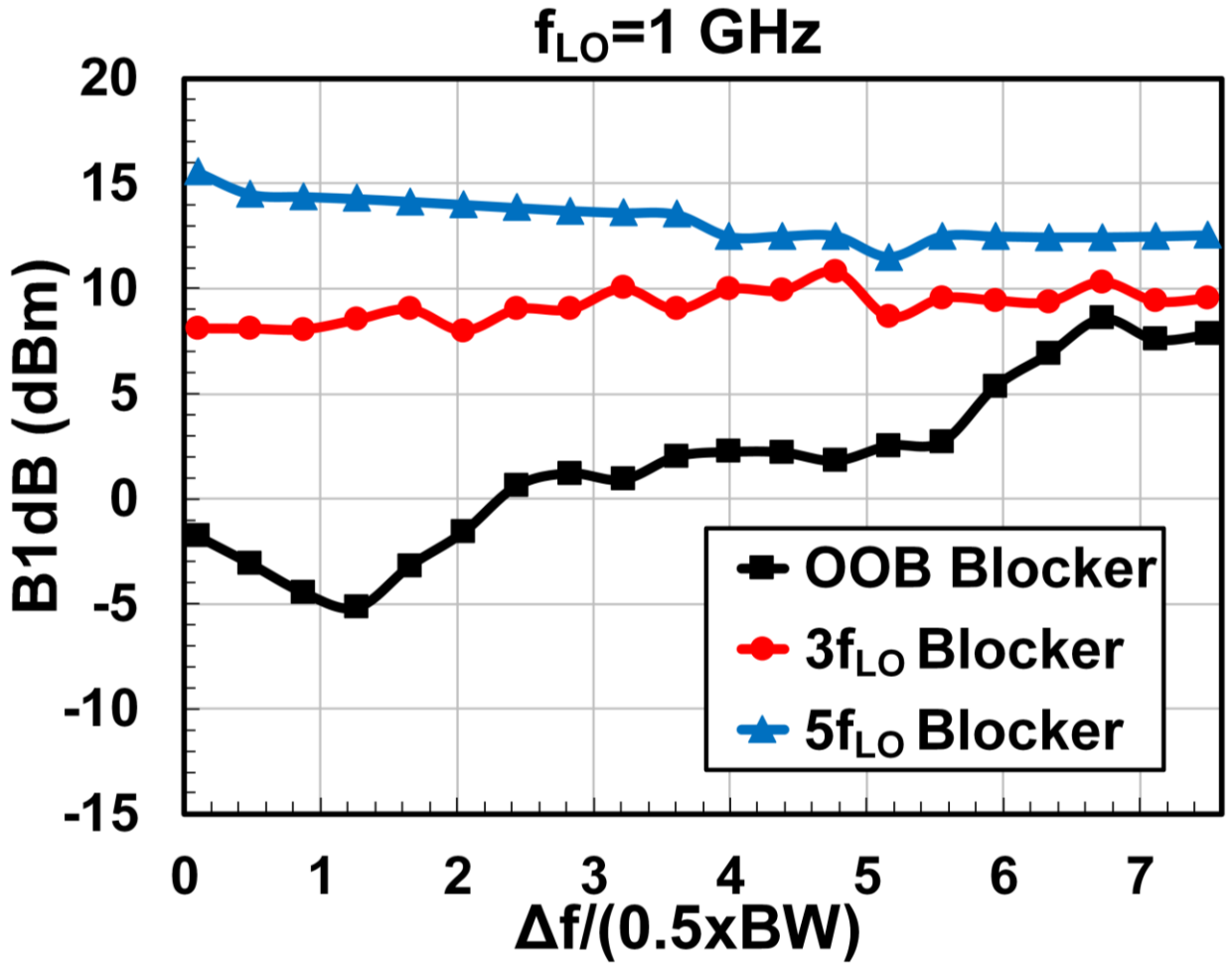




Out-of-Band IIP3 of 29.4dBm is achieved for f_{LO} = 1GHz and Δf/(0.5*BW) = 6

Blocker Tolerance





Result Summery and Comparison

	JSSC 2015	RFIC 2016	JSSC 2011	TMTT 2014	IMS 2016	JSSC 2019	IMS 2022	This Work
Type	Receiver	Receiver	Filter	Filter	Filter	Filter	Filter	Filter
Architecture	Noise-Cancelling Receiver with HR-TIAs	Filtering by Aliasing	N-Path Filter	λ/2 Resonator with Center-Tapped Open-Stub	Dual Adaptive TRZ Using N-Path Circuit	Coupled N-Path Resonators	Rotary Clocking N-Path Filter	Low-Loss Fully-Passive HR N-Path Filter
CMOS Technology	28nm	65nm	65nm	PCB Rogers 4350B	65nm	65nm	65nm	45nm SOI
RF Input	Differential	Differential	Differential	Single-Ended	Differential	Differential	Single-Ended	Differential
Frequency Range [GHz]	0.1-3.3	0-1	0.1-1.0	0.58-0.91	0.2-1.2	0.8-1.1	0.2-0.8	0.25-2
IB Gain [dB]	NR	NR	-2	-1.53	+21	-4.6 ~ -3.8	+10.2	-2 ~ +0.5
BW [MHz]	0.2-3	10, 20	35	115-315[1]	6.2	30-50	40	80
NF [dB]	1.7[2]	32	3-5	1.53	4.5-6.2	5.0-8.6	3.7-6.4[2]	3.1-5.0[2]
OOB Blocker P1dB [dBm]	0 (Δf/BW=40)	NR	+2	NR	+8	+9 (Δf/BW=1)	-1 (Δf/BW=2.5)	+2.5 (Δf/BW=1) +8 (Δf/BW=2)
IB/OOB IIP3 [dBm]	+11.5	+31 (Δf/BW=5)	+14	+13-+19[3]	-1[4] (Δf/BW=0.32) +18 (Δf/BW=7.25)	+24 (Δf/BW=1)	+4.5 +12.9 (Δf/BW=2.5)	+27.8 (Δf/BW=1) +29.4 (Δf/BW=2.5)
Power Consumption [mW]	36.8-62.4	8	2-16	0	30-70	80-97	5.5-38	2.3-15.7
Supply Voltage [V]	1	1.2/1	NR	0-28[5]	1.2	1.0/2.5	NR	1.1
Active Area [mm^2]	5.2	1.68	0.07	1338[6]	2.2	1.9	0.56	0.14
$3f_{LO}/5f_{LO}$ HR [dB]	60/60[7]	27 @$3f_{LO}$ 36 @$5f_{LO}$	10 @$3f_{LO}$[4] 17 @$5f_{LO}$[4]	3 @$3f_0$[4,8]	NR	22 @$3f_{LO}$[4]	NR[8]	>46 @$3f_{LO}$ >48 @$5f_{LO}$
Harmonic B_{1dB} [dBm]	-6.5 @$3f_{LO}$ -3 @$5f_{LO}$	NR	NR	NR	NR	NR	NR	>8 @$3f_{LO}$ >11 @$5f_{LO}$

[1] Tuning of seven separate varactors is required. [2] Buffer noise contribution is de-embedded. [3] Limited to the tuning varactors. Numbers are estimated based on datasheets of the varactors.
[4] Estimated from measurement plots. [5] Used for varactor tuning. [6] Estimated from fabrication plot. [7] Harmonic rejection is performed in two stages. [8] Filter is transparent around $3f_0$ and $5f_0$.

Outline

- Motivation and Introduction
- Switch-Capacitor Harmonic Rejection Methods
- Circuit Implementation
- Measurement Results
- **Conclusion**

Conclusion

- A low-loss fully passive HR N-Path filter has been proposed.
- The proposed HR N-path filter offers high linearity, tunability, and high rejection of harmonic blockers while operating with low power in a small form factor.
- The circuit requires no additional circuitry beyond extra switches and benefits from technology scaling.

Acknowledgment

- The authors would like to thank the MIT MTL faculty for equipment assistance.
- Also, the authors would like to thank Qingyun Xie and Eunseok Lee for their assistance with the measurement setup.

Thank you for your attention.