Tu4D-2

Real-time FPGA-based Implementation of Digital Predistorters for Fully Digital MIMO Transmitters

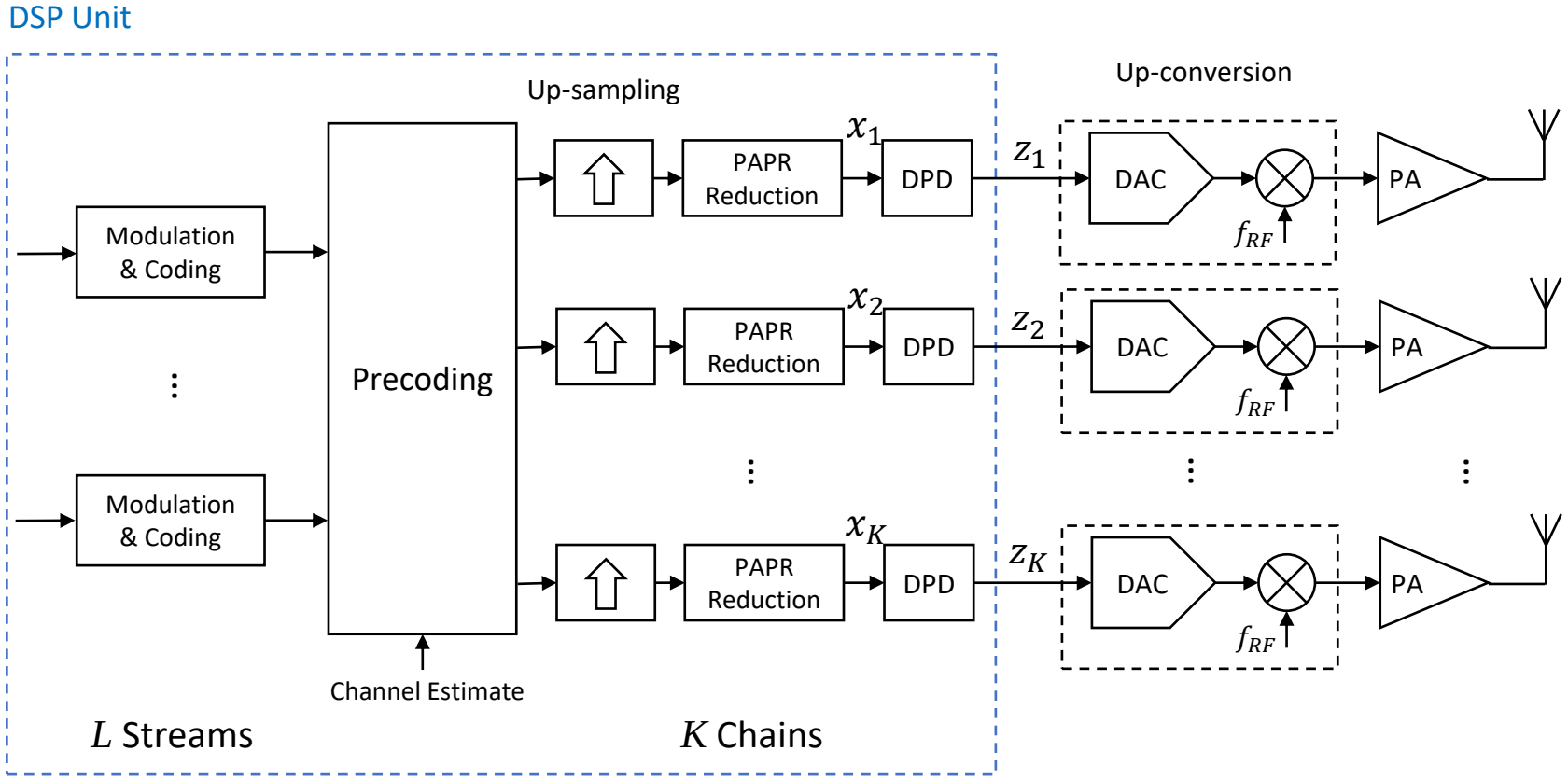
H. Barkhordar-pour, J. G. Lim, M. Almoneer,
P. Mitran and S. Boumaiza

Emerging Radio Systems Group (EmRG),
University of Waterloo, Waterloo, Canada

Outline

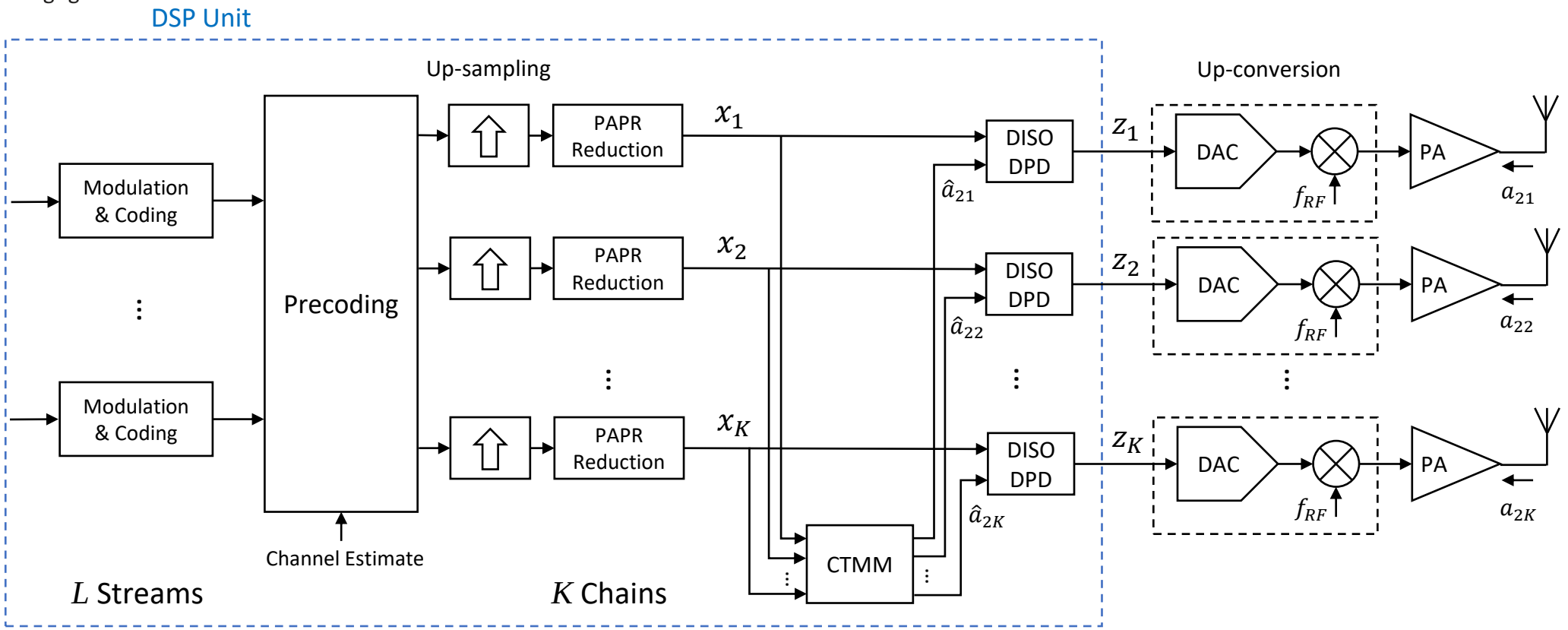
- Introduction
- Piecewise linear dual-input dual-output DPD model
- Hardware implementation results
- Measurement results
- Conclusion

Introduction



- *K*-chain fully digital MIMO transmitter with per-chain DPD.
- Everything is extendable to MIMO, except DPD.

Introduction

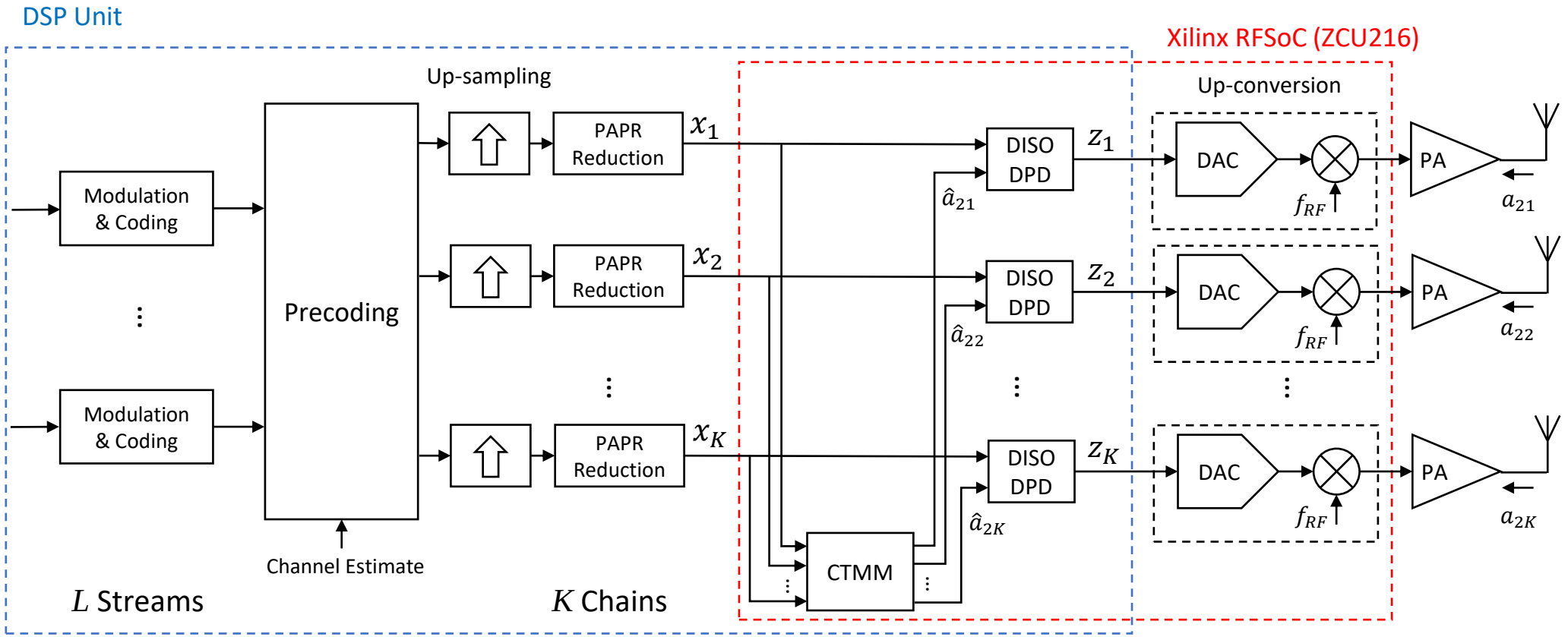


- Dual-input Single-output (DISO) DPD linearizes MIMO transmitters,
- Cross-talk and Mismatch Module (CTMM) predicts reflected waves from antenna array [1].

Introduction

- Exploring hardware implementation of DPD solutions for fully digital MIMO transmitters allows:
  - Evaluation of processing resources and power consumption of per-chain DPD.
  - Investigation of limits of these DPD solutions.
  - Research in low-complexity, scalable DPD solutions.

Introduction

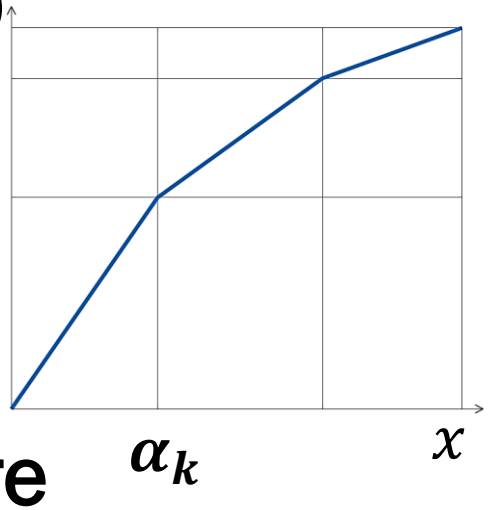


- The goal of this work is to implement the DISO DPD solution for fully digital 5G MIMO transmitters on an FPGA.

Piecewise Linear DISO DPD

- Define the piecewise-linear function as $f(x;\boldsymbol{\alpha},\boldsymbol{\phi})$, which consists of N linear intervals, between the points (α_k,ϕ_k) and $(\alpha_{k+1},\phi_{k+1})$ [2]:

$$f(x;\boldsymbol{\alpha},\boldsymbol{\phi}) = \left(\frac{\phi_{k+1}-\phi_k}{\alpha_{k+1}-\alpha_k}\right)(x-\alpha_k)+\phi_k = Ax+B\,, \qquad \alpha_k \le x < \alpha_{k+1} \tag{1}$$



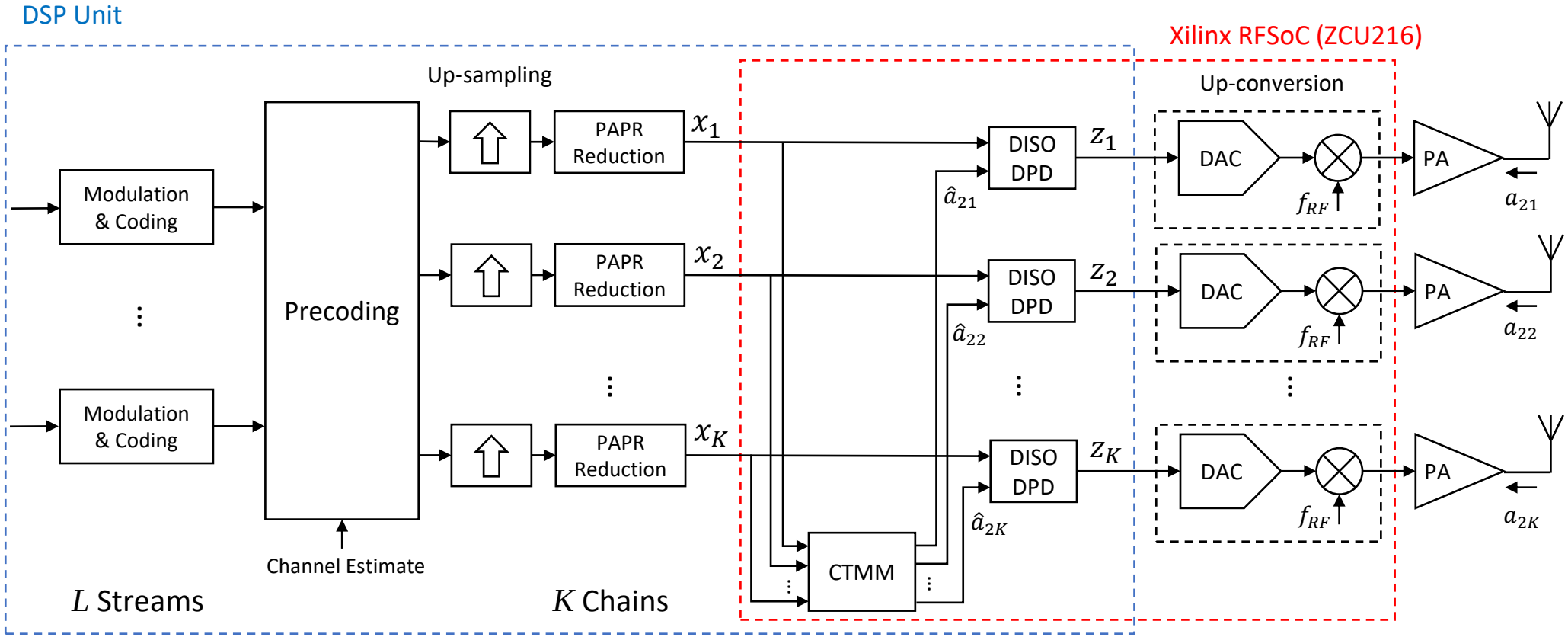
- To avoid using the square-root function in hardware implementation, we replace $f(|x[n]|;\alpha,\phi)$ with $f(|x[n]|^2;\alpha,\phi)$ [3]

Piecewise Linear DISO DPD

- In a MIMO system, the reflected wave from the antenna is a function of all input signals due to crosstalk [1].
- The reflected wave from each antenna can be predicted and used as a second input to the DPD module.

$$\hat{a}_{2k}[n] = \sum_{i \neq k} \sum_{q=0}^{Q-1} \lambda_{ki}[q] x_i[n-q] \qquad (2)$$

Piecewise Linear DISO DPD



$$\hat{a}_{2k}[n] = \sum_{i \neq k} \sum_{q=0}^{Q-1} \lambda_{ki}[q] x_i[n-q]$$

Hardware Implementation

- The processing hardware used was a Xilinx Ultrascale+ RFSoC ZCU216 evaluation board.
- DACs were operated at 9.6 GSps, with interpolation factor of 8.
- FPGA was operating at 300 MHz.
- The DISO DPD engine was parallelized [3] with a factor of 4 to allow up to 1.2 GHz linearization bandwidth with a clock rate of 300 MHz.

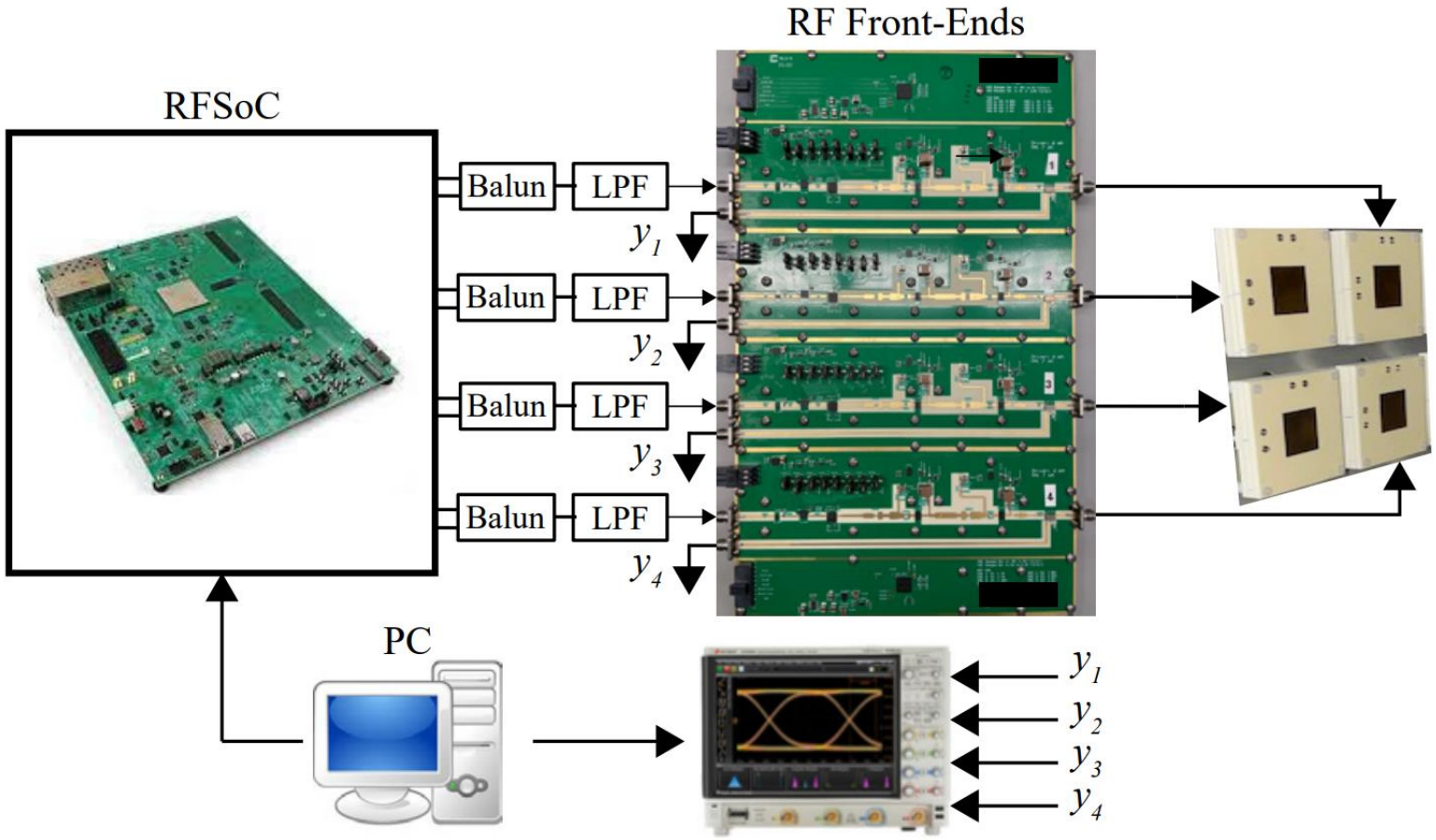
Hardware Implementation Results

- The FPGA resource utilization of the proposed DPD is reported.
- Power consumption of single RF chain was 7.5 W (for 34 dBm output power).

Linearization Bandwidth	1.20 GHz			600 MHz		
Number of Chains	1	4	8	1	4	8
DSP Slices (%)	5.8	44.5	89.1	2.8	22.2	44.5
Slice LUTs (%)	3.5	25.2	50.8	1.7	12.4	24.9
Slice Regs (%)	1.6	12.9	25.9	0.8	7.9	15.9
BRAMs	0	0	0	0	0	0
Power (W)	1.6	12.6	23.6	0.7	5.3	9.7

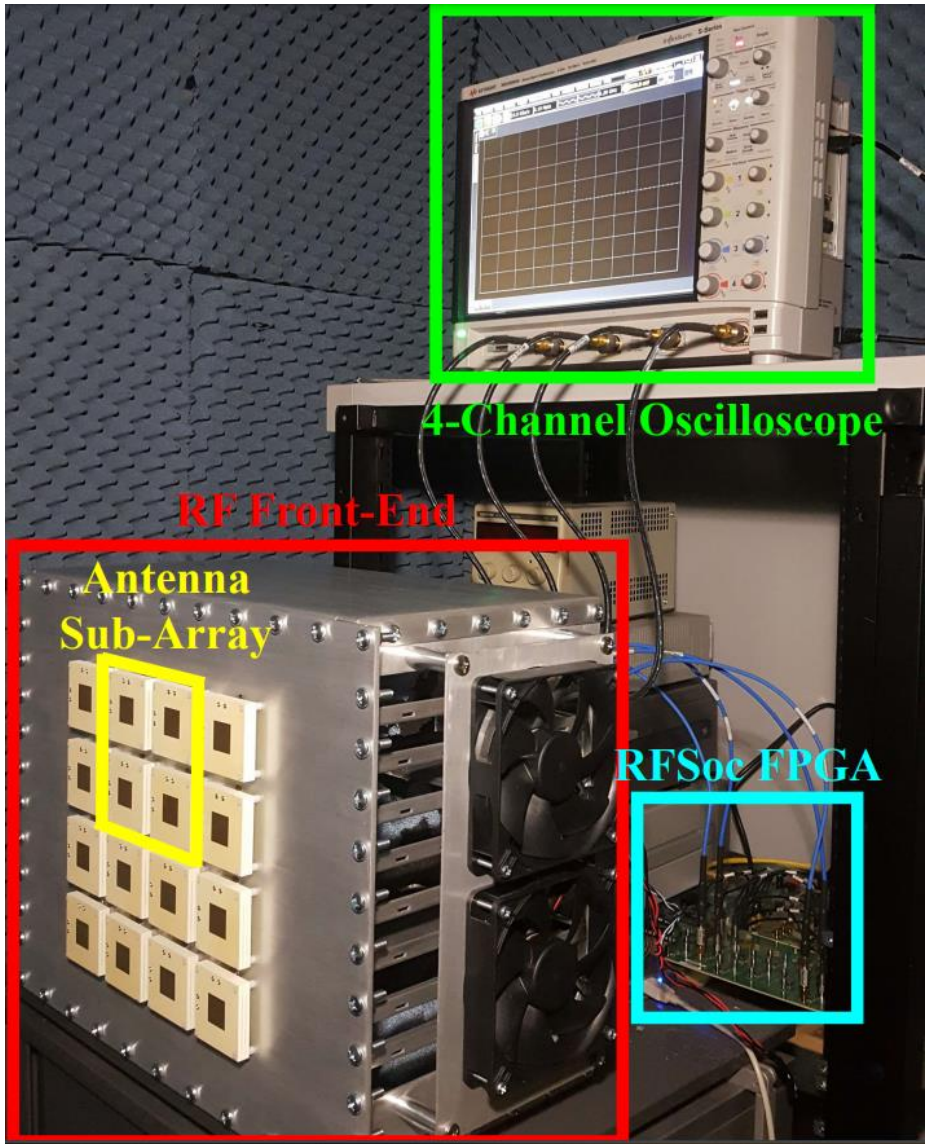
Measurement Setup

- Test signal: 75-MHz OFDM signal, 8 dB PAPR.
- DUT: 4 x custom two-stage PAs with two pre-driver stages @ 3.5 GHz, outputs connected to 2 x 2 antenna sub-array.



Measurement Setup

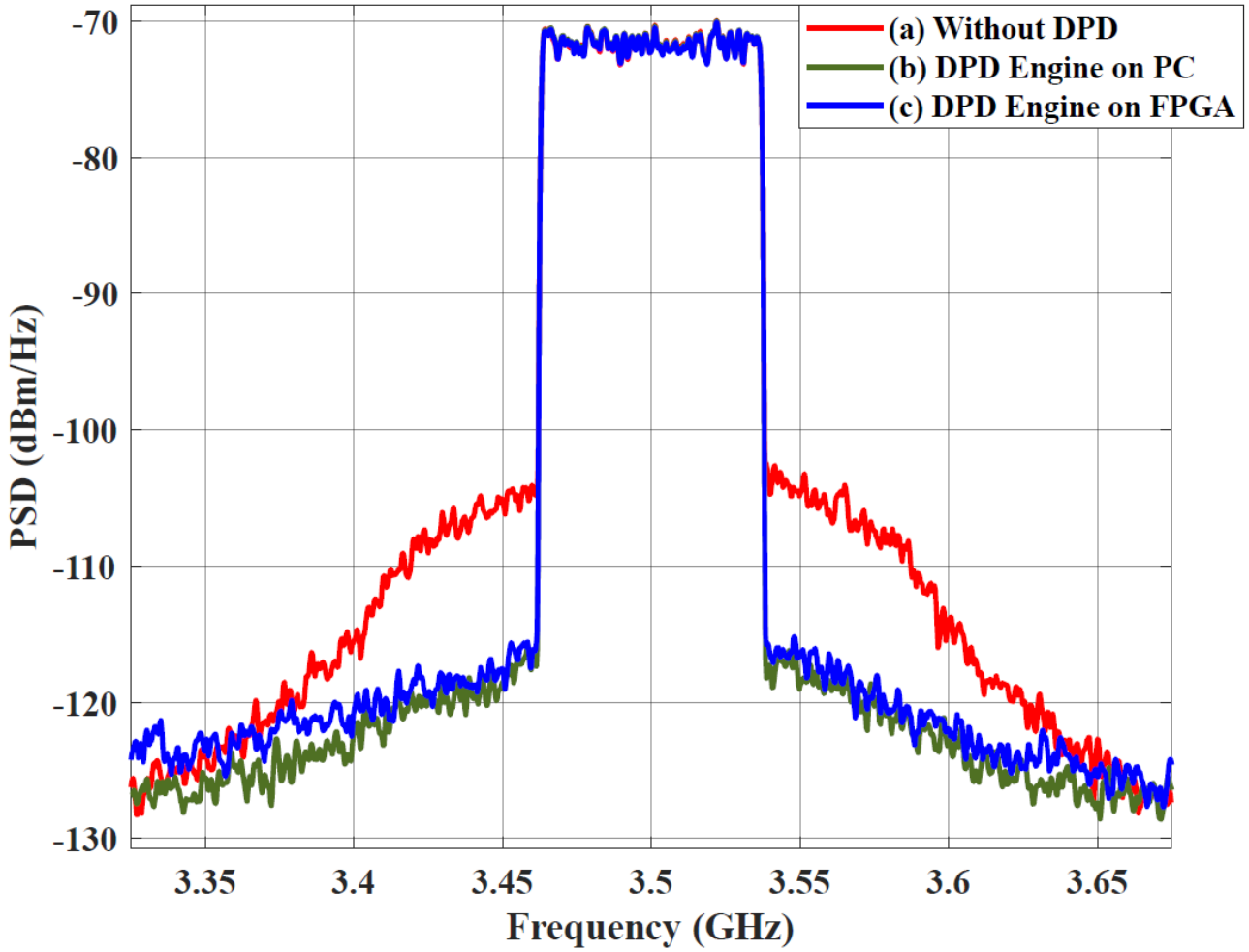
- Experiments were conducted inside anechoic chamber.
- DPD coefficients are updated on the PC and uploaded to the FPGA to be applied to the signal.



Measurement Results

- Spectrum comparison presented at an estimated over-the-air boresight receiver.

	RNMSE (%)	ACPR (dB)
Without DPD	7.7	-33.4
With PC DISO DPD	1.4	-48.3
With FPGA DISO DPD	1.5	-47.1



Conclusion

- A piecewise linear DISO DPD model was proposed and implemented in hardware to linearize MIMO transmitters.
- Hardware implementation results were presented for single chain, 4 chain MIMO and 8 chain MIMO.
- The FPGA-implemented DPD was evaluated at 3.5 GHz with a 300 MHz clock rate showing satisfactory results compared to the PC-based DISO DPD.

References

[1] K. Hausmair, P. N. Landin, U. Gustavsson, C. Fager, and T. Eriksson, "Digital predistortion for multi-antenna transmitters affected by antenna crosstalk," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1524–1535, 2018.

[2] A. Molina, K. Rajamani, and K. Azadet, "Digital predistortion using lookup tables with linear interpolation and extrapolation: direct least squares coefficient adaptation," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 3, pp. 980–987, Mar. 2017.

[3] M. Almoneer, H. Barkhordar-pour, P. Mitran, and S. Boumaiza, "Hardware-efficient implementation of piece-wise digital predistorters for wideband 5G transmitters," in *IEEE MTTS Int. Microw. Symp. Dig.*, 2022, pp. 514–517.

Acknowledgments

Financial co-sponsors:

NSERC
CRSNG

ERICSSON

KEYSIGHT

FPGA board donation:

XILINX