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Early Career Paper Finalist

A 3-Way GaN Doherty Power Amplifier for 28GHz 5G FR2 Operation

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Politecnico di Torino

Outline

- Introduction
- Motivation
- Theory review
- Design
- Results
- Comparison with state of the art
- Conclusion
- Acknowledgements

Introduction

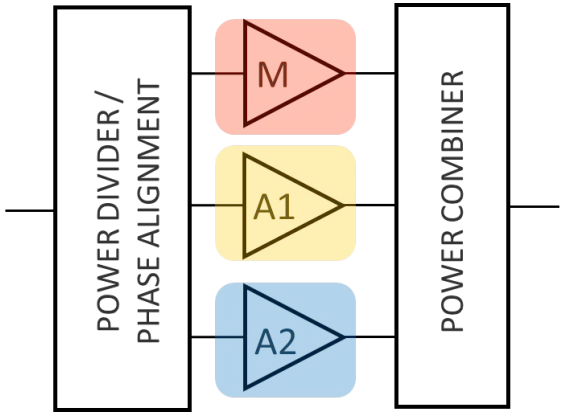
- Wireless communication systems:
  - High-PAPR signals (9-12 dB)
  - FR1 band well-established
  - Foreseen extension towards FR2 bands
- Power amplifiers:
  - Back-off efficiency enhancement
  - Gain requirement vs. achievable bandwidth
  - Single-stage vs. multi-stage implementation

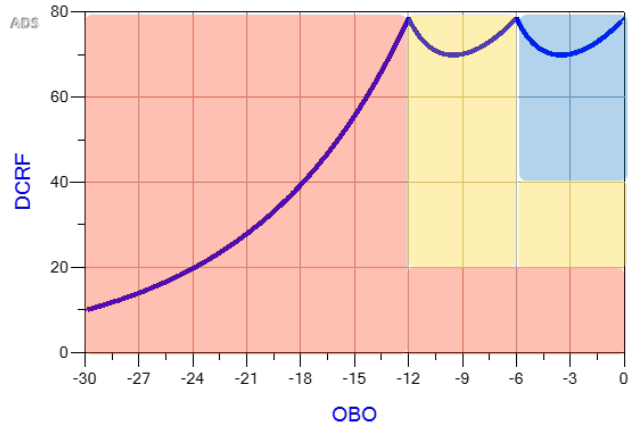
Introduction

- Load-modulated PAs for deep back-off:
  - Doherty (asymmetric, multi-way)
  - DEPA
  - S-LMBA
- Challenges:
  - Gain penalty (DPA, S-LMBA)
  - Reliability (DEPA, S-LMBA, DPA?)
  - Number of active devices (DEPA)
  - Bandwidth

Motivation

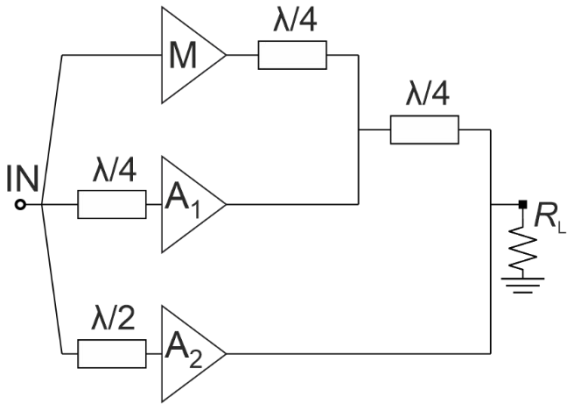
- 2-way DPA: 6-dB back-off
  - Popular and established at < 6 GHz
  - Recently demonstrated at > 6 GHz (18 GHz, 28 GHz)
- *N*-way Doherty PA architecture : deep back-off
  - Combiner design for improved reliability
    - no Main overdrive
  - Deal with gain penalty
    - Multi-stage implementation
  - Extension towards FR2 bands

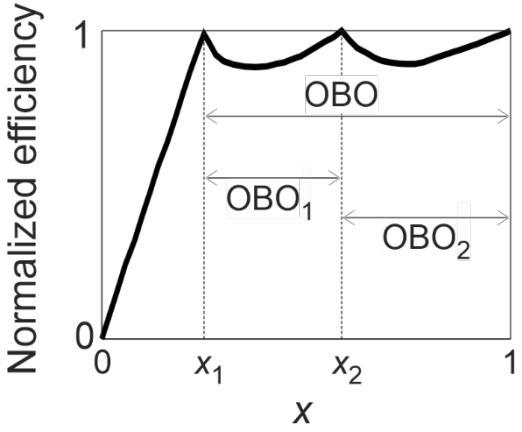


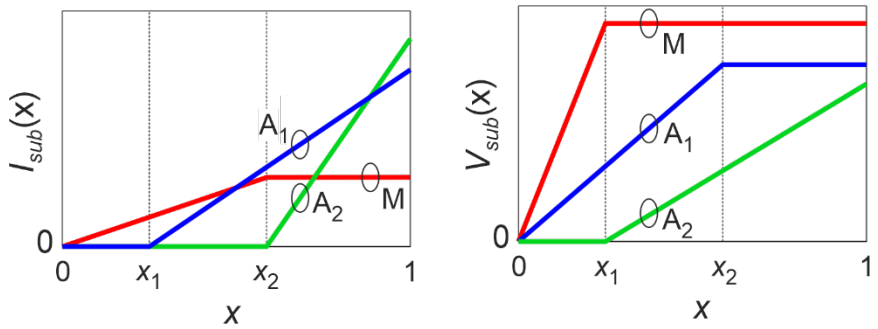


Theory review

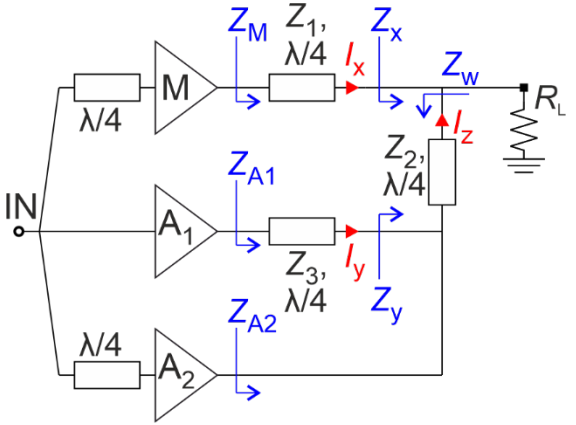
- Combiner topology and required driving

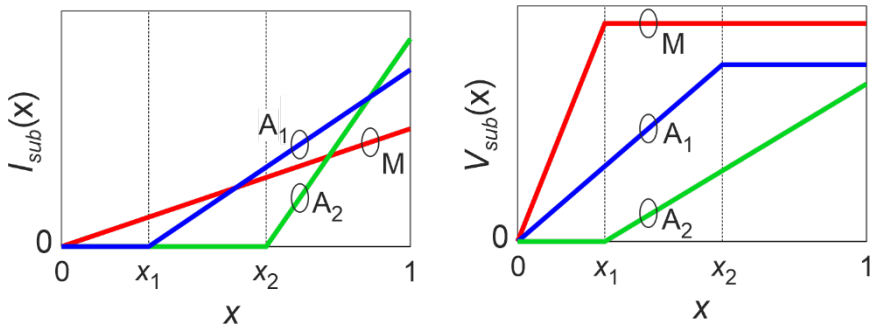






Others





This work

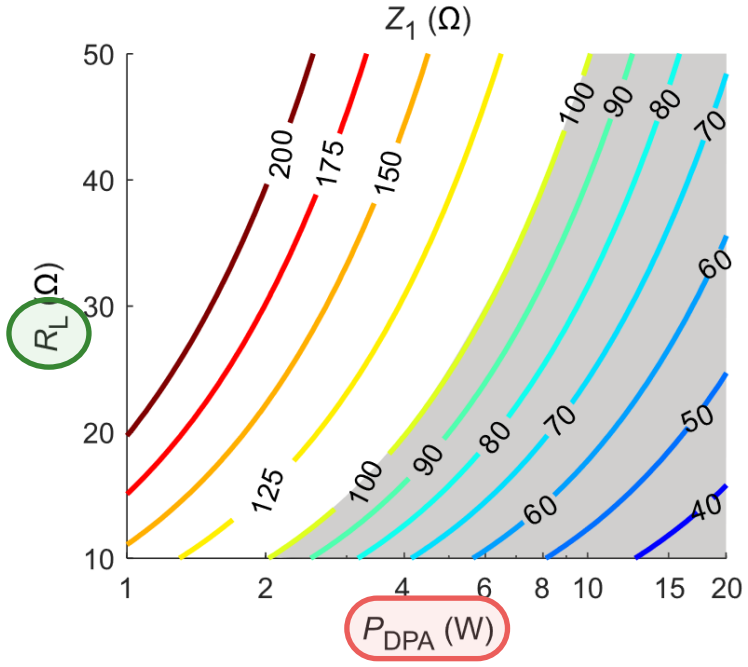
Theory review

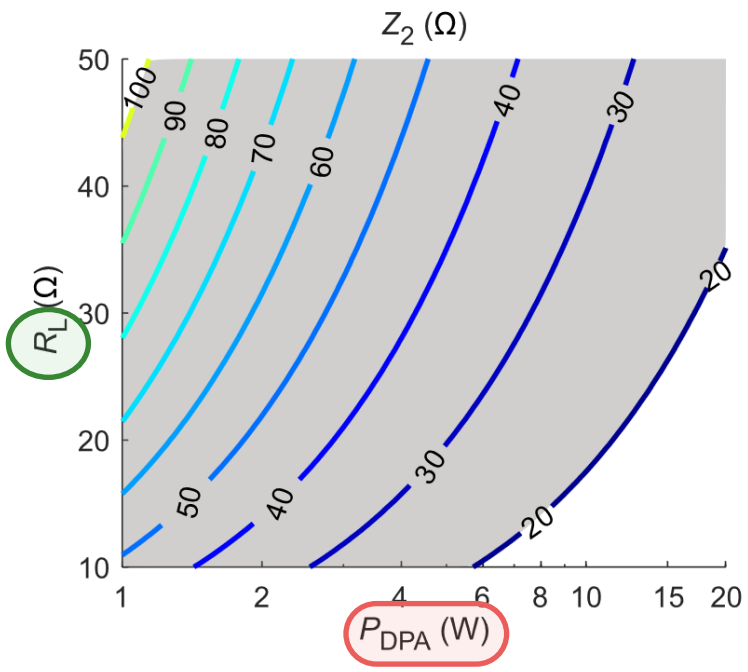
- Design space

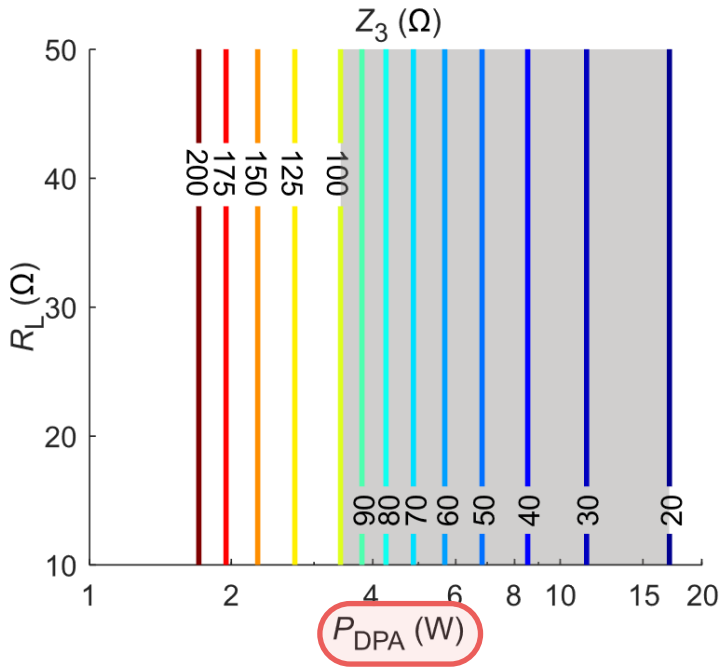
$$Z_1 = \frac{V_{\mathrm{Max,M}}}{I_{\mathrm{x}}(1)} = \frac{V_{\mathrm{Max,M}}}{\alpha_1} \cdot \sqrt{\frac{R_{\mathrm{L}}}{2\,P_{\mathrm{DPA,sat}}}}$$

$$Z_2 = \frac{V_{\mathrm{Max,A_2}}}{I_{\mathrm{z}}(1)} = \frac{\beta_2 \cdot V_{\mathrm{Max,M}}}{1-\alpha_1} \cdot \sqrt{\frac{R_{\mathrm{L}}}{2\,P_{\mathrm{DPA,sat}}}}$$

$$Z_3 = \frac{V_{\mathrm{Max,A_1}}}{I_{\mathrm{y}}(x_2)} = \frac{\beta_1 \cdot \beta_2 \cdot V_{\mathrm{Max,M}}^2}{2 \cdot \alpha_2(1-\alpha_1) \cdot P_{\mathrm{DPA,sat}}}$$

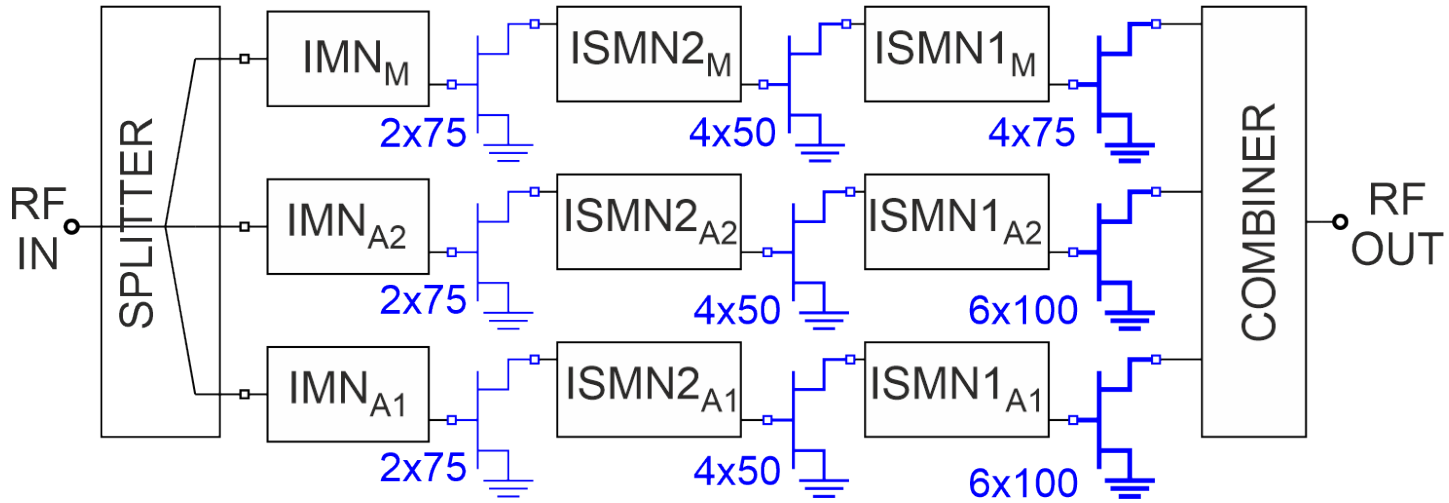






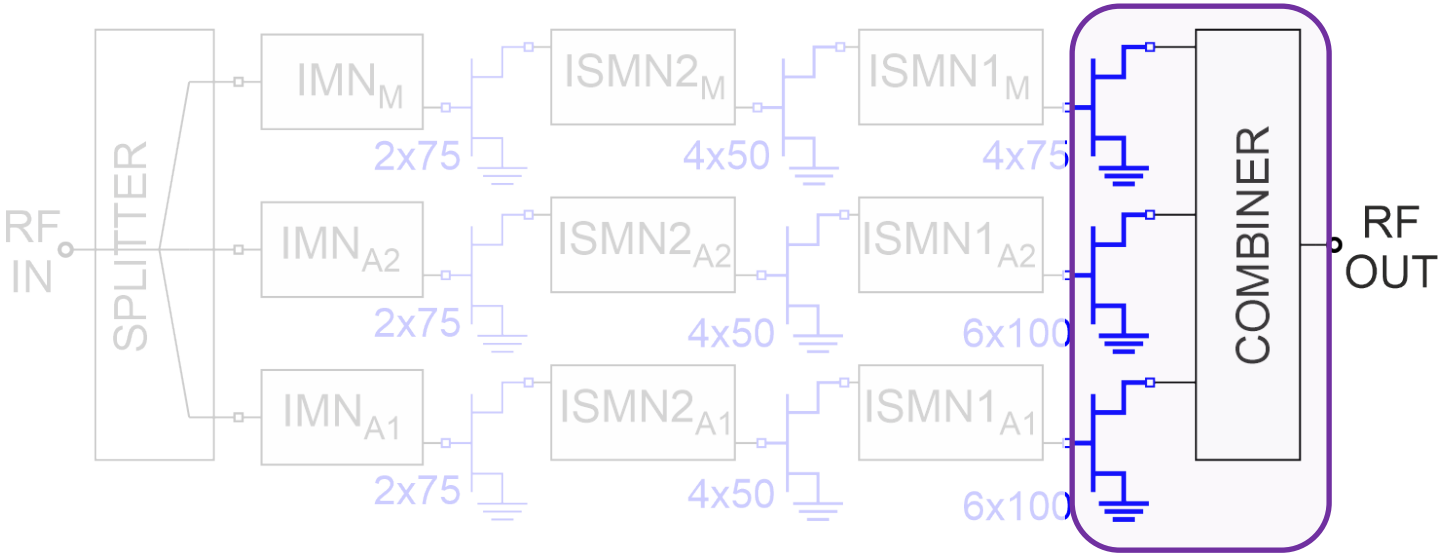
Design

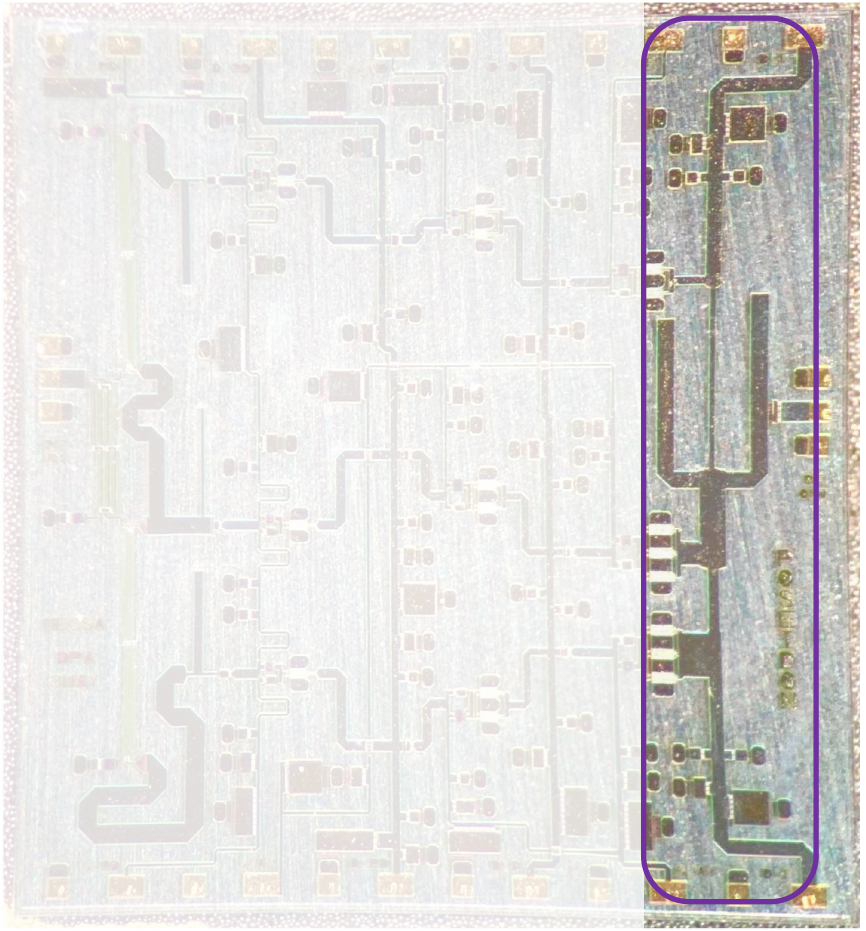
- Technology
  - WIN Semi's NP15 (150 nm GaN/SiC HEMT)
- Specifications
  - Sat. output power: 3 W
  - Linear gain: 20 dB
  - OBO: 6dB / 12dB
- Architecture
  - 3-stage (pre-driver + driver + final)



Design

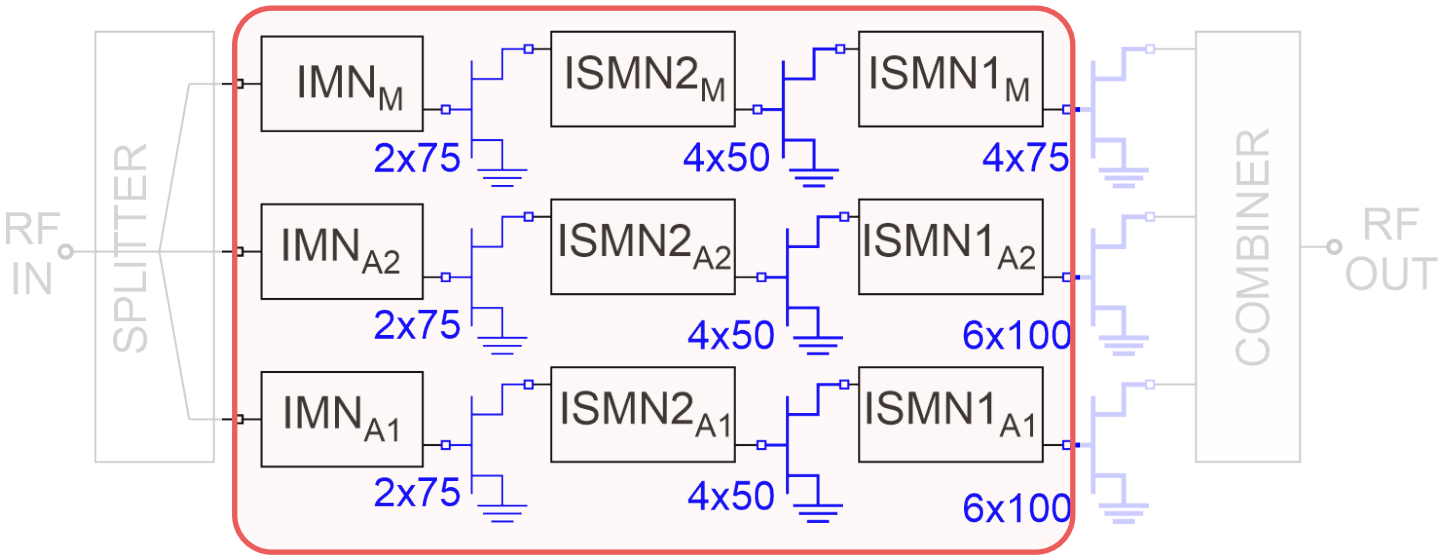
- Combiner
  - Semi-lumped λ/4
  - Line-stub post-matching
    - from ≈11 Ω to 50 Ω

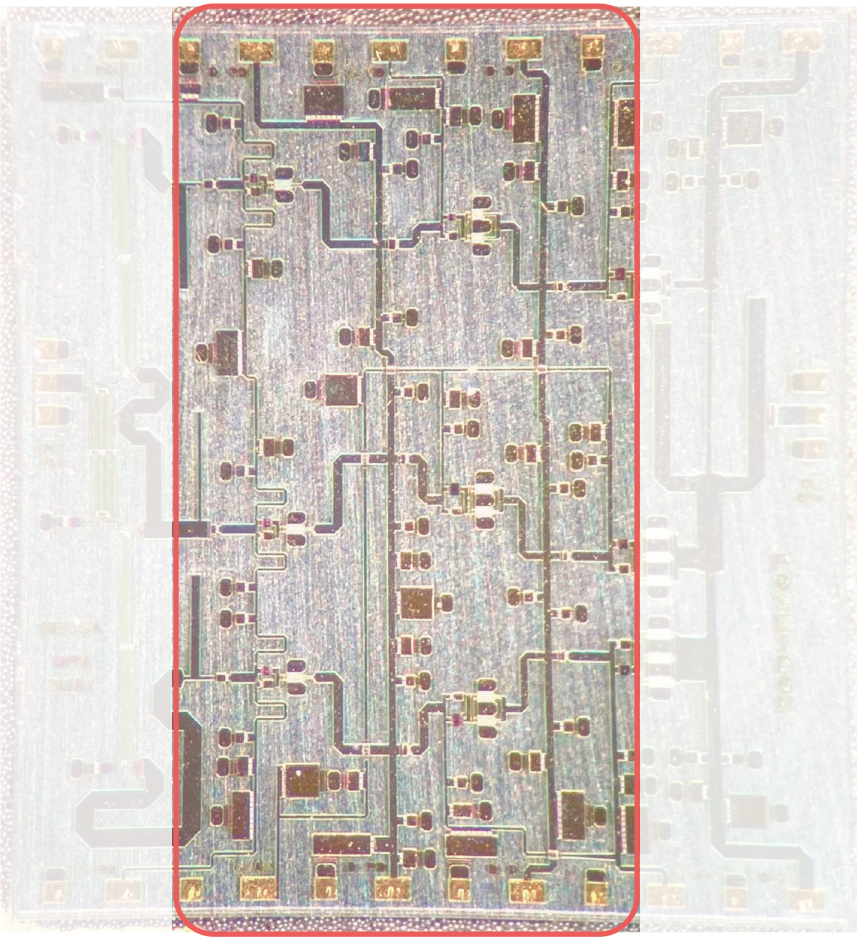




Design

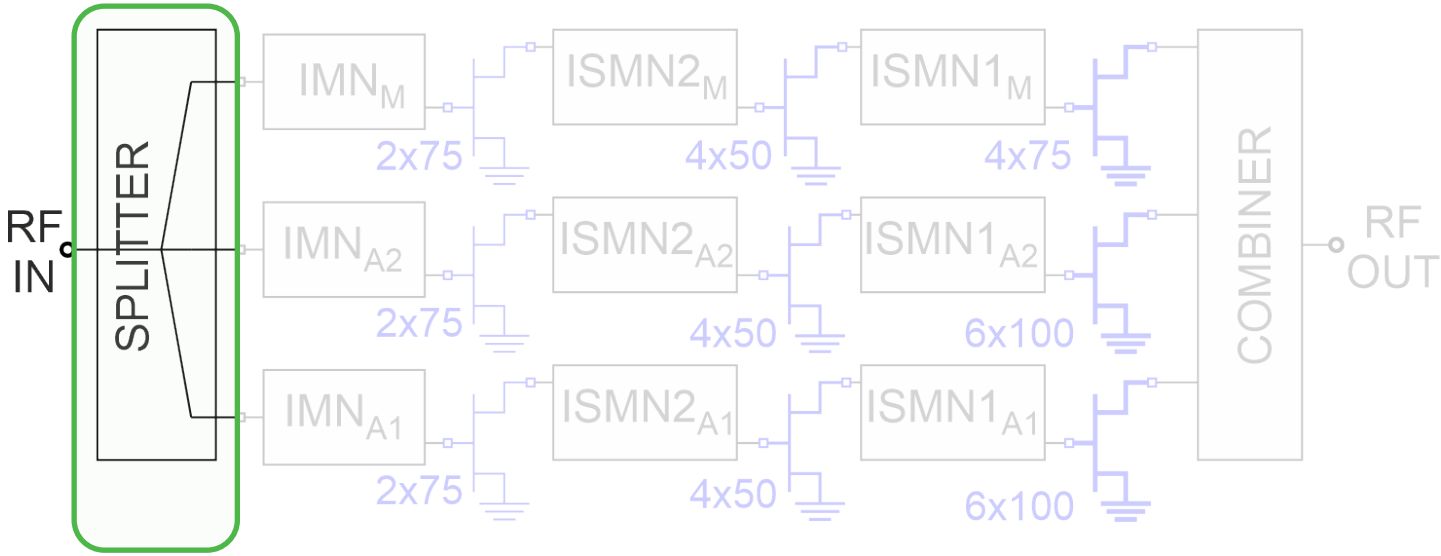
- Symmetric MNs
  - Simple routing
  - Trade-off with degrees of freedom

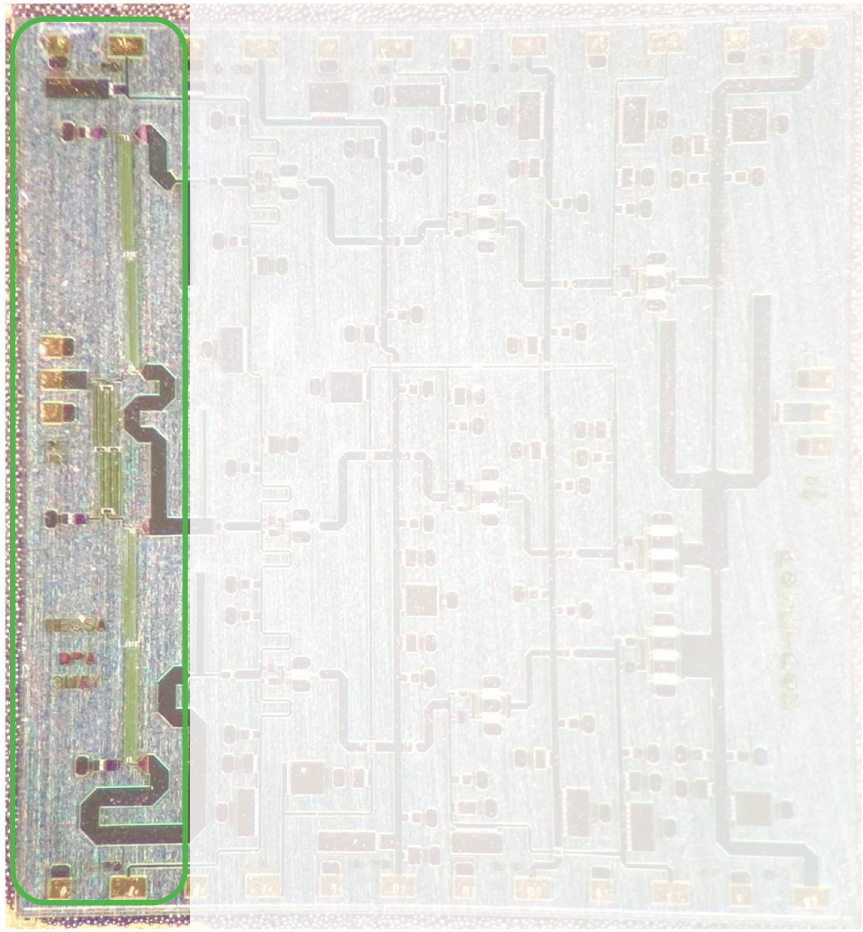




Design

- Input splitter
  - 3-way
  - Isolated
    - 2 levels of Lange couplers

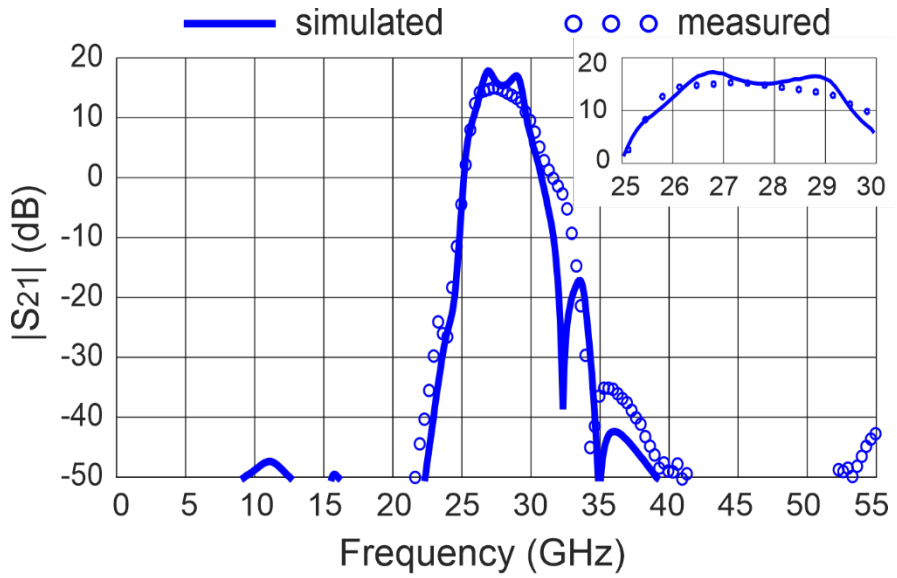


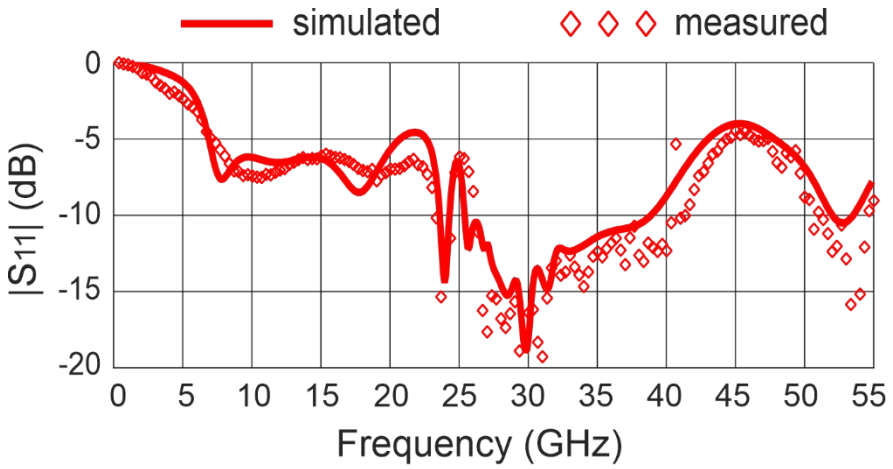


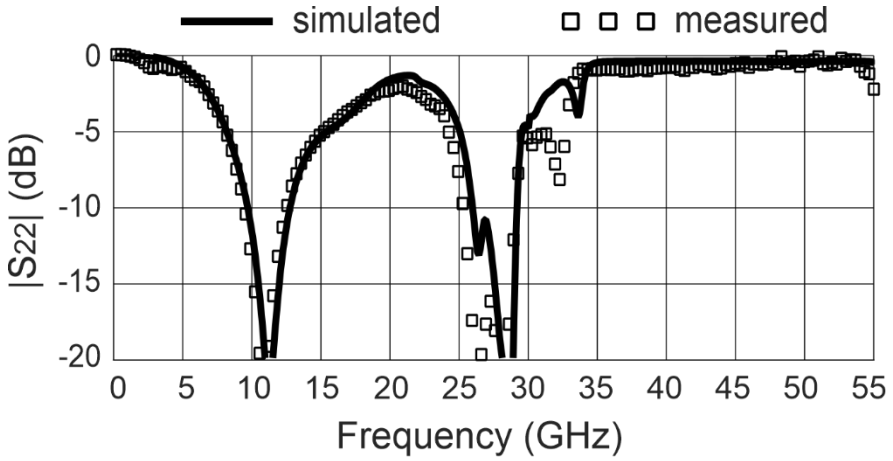
Results

- Small signal

V_{DD}=20 V
$V_{G,pd}$= $V_{G,dM}$= $V_{G,M}$= -2 V → $I_D \approx$ 30 mA
$V_{G,dA1}$= $V_{G,A1}$= -2.2 V → I_D = 0 mA
$V_{G,dA1}$= $V_{G,A1}$= -3.4 V → I_D = 0 mA



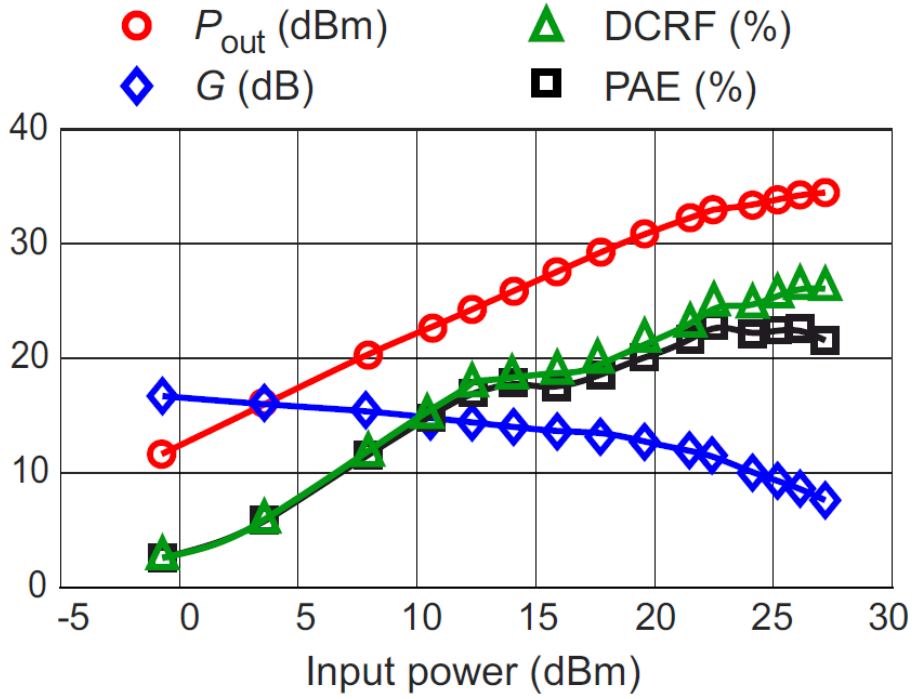


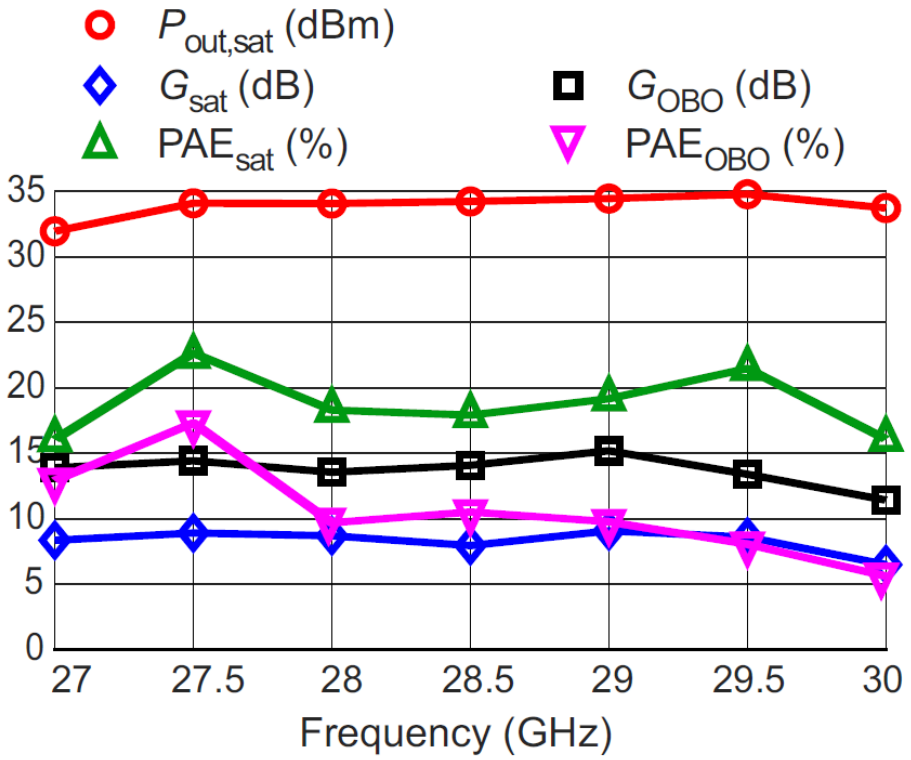


Results

- Large signal: 1-tone CW

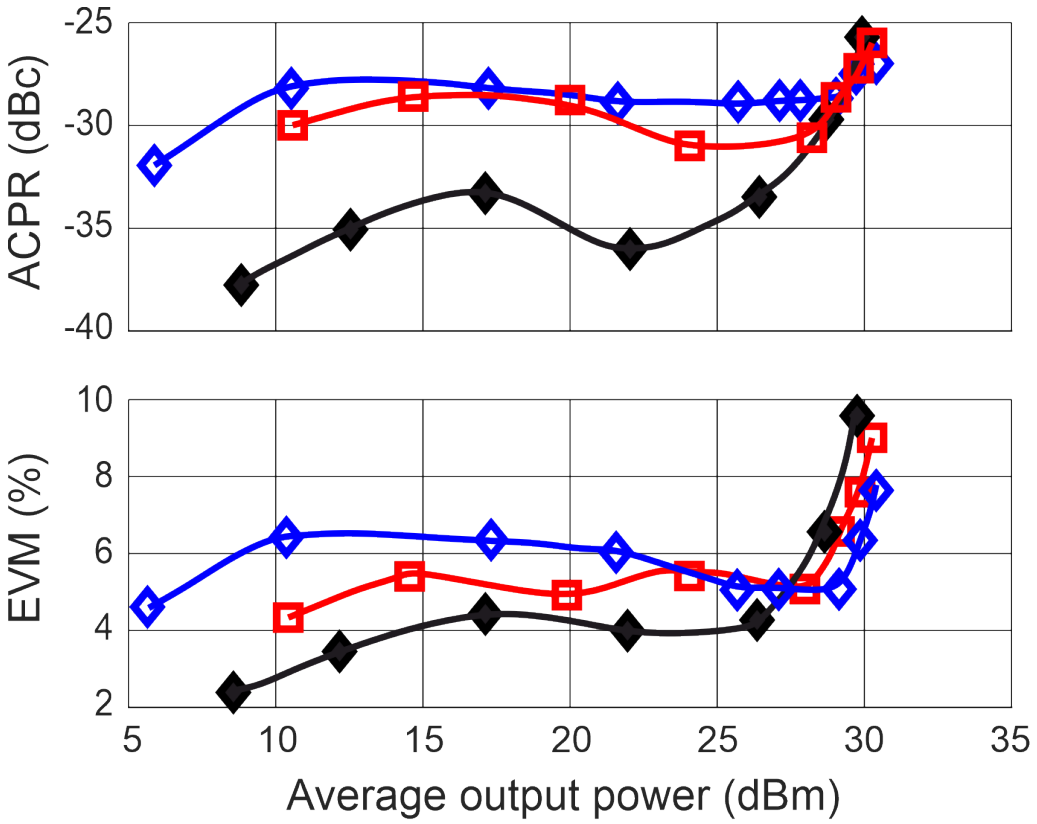
27.5 GHz

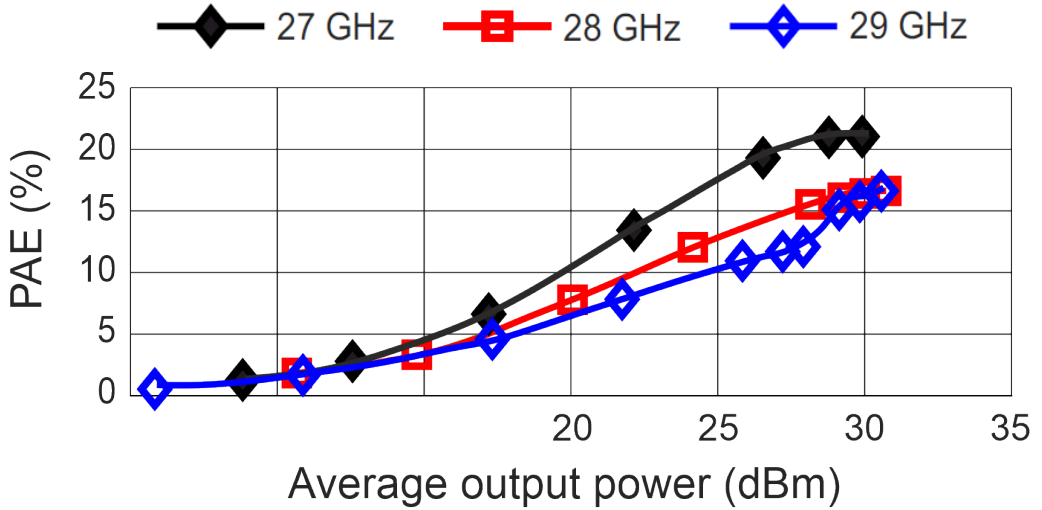




Results

- Large signal: modulated
  - 64-QAM standard NR downlink signal, 50 MHz BW, 10 dB PAPR





Comparison with SoA

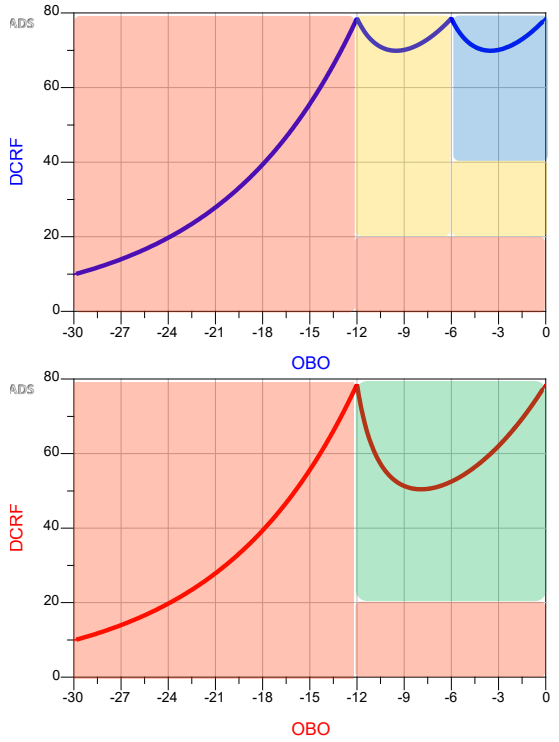
Techn.	Freq. (GHz)	$P_{out,sat}$ (dBm)	PAE_{sat} (%)	$PAE^{\#}_{OBO}$ (%)	G_{sat} (dB)	Ref
Si	28	22.4	40*	18*	10*	[10]
Si	26	18.7	32*	8*	12.5*	[11]
GaAs	27.25–29.75	27	37	12*	18	[9]
GaAs	28	30	38	10*	15*	[12]
GaN	26–30	36.1	26.7	15*	7	[13]
GaN	24–28	34	23	-	18	[14]
GaN	28.5–29.5	29*	30*	18*	4*	[15]
GaN	28–29	34	20	12	8	[8]
GaN	**27.5–29.5**	**34**	**18–23**	**8–16**	**8–9**	**T. W.**

PAE at 10 dB OBO
* Value extrapolated from graphs

Conclusion

- Theory and design space
  - 3-way DPA for deep back-off efficiency enhancement
    - Extension to N>3 possible
  - No Main overdrive
- Implementation
  - MMIC 3-stage 3-way DPA
  - Challenge of FR2 frequencies: gain
  - Good efficiency, but can be improved
  - High intrinsic linearity

3-way
vs.
2-way
asymmetric
DPA?



Acknowledgements

- Technology:
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