We1D-4

Low Insertion Loss Sub-6GHz Heterogeneous GaN/RF-SOI SPDT Switch for High Power Applications

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Outline

- 5G-NR requirements and how X-FAB address them
- Co-integration technique presentation
- SPDT switch design and characterization results
- Thermal issue and proposed solution
- Conclusion

5G-NR: Requirements for higher data rate

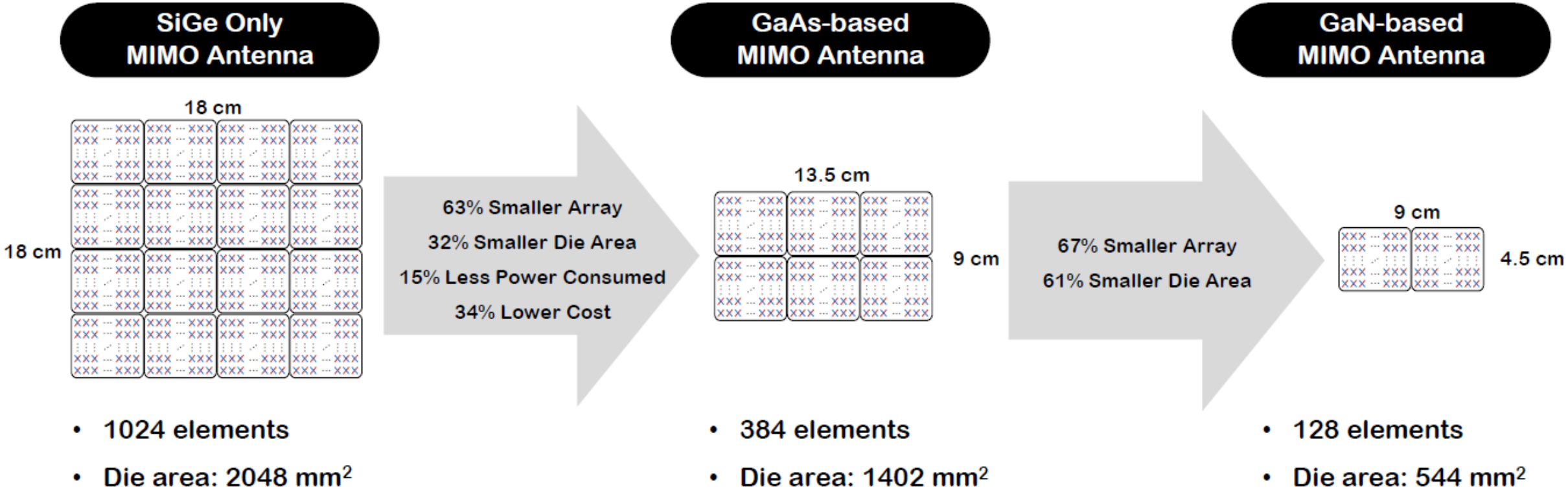
Higher bandwidth (up to 400MHz)
↓
Use of mm-wave frequencies
↓
Technologies with high Ft/Fmax

Use of MIMO & beamforming
↓
smaller circuit footprint
↓
Higher power density & efficiency
(+ lower DC consumption)

Increase number of subcarriers
↓
Higher linearity & more selective and complex filters (→ more losses)
↓
Higher power for PA & switches

Use 256 QAM modulation
↓
Required EVM < 3%
↓
Lower noise & Higher linearity

5G-NR: Choice of the right technology



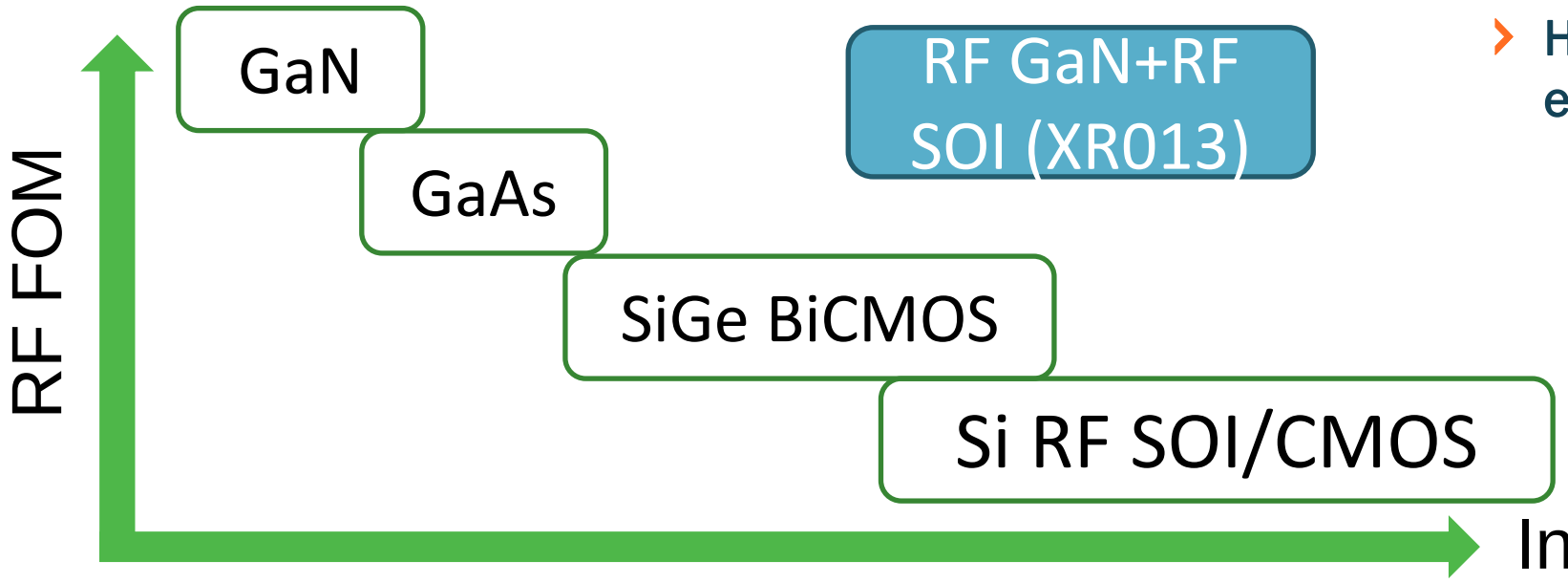
III-V and especially GaN simplifies the base station Architecture.

Limitation of full GaN circuit : Tech. Maturity, Switch performances and integration capabilities.

Everything you need to know about 5G today, Tuan Nguyen, Qorvo, Webinar 2019

X-FAB proposal to address 5G

- X-FAB aims to serve the need for high-performance RF Front-End solutions



- **Highly performant, compact & cost-effective technology :**
  - **RF GaN HEMT** where needed
  - **RF-SOI** → analog, digital & some RF elements

- GaN: highest cost with GaN/SiC. Maturity of GaN/Si improving
- GaAs: mature and available at medium cost
- SiGe: medium power, good integration with moderate cost
- Si: lowest power, highest integration at lowest cost for high volumes

Inspired by MACOM

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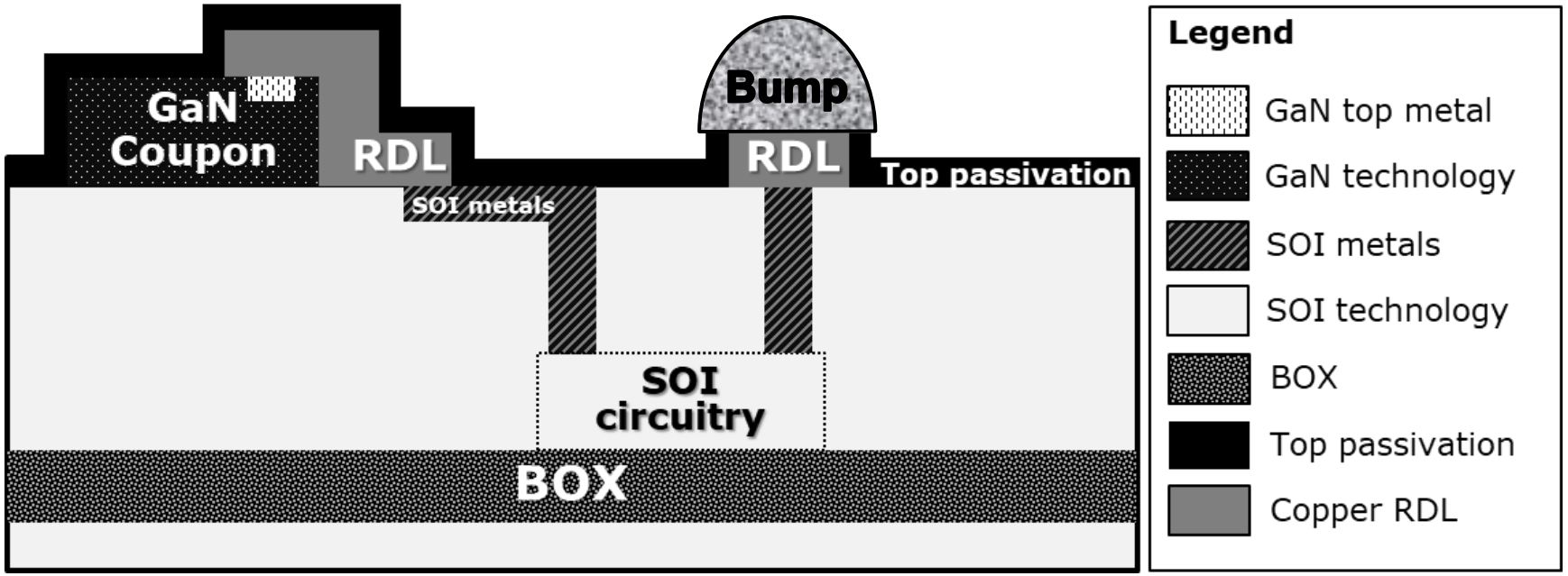
RF GaN micro-transfer printing on RF-SOI



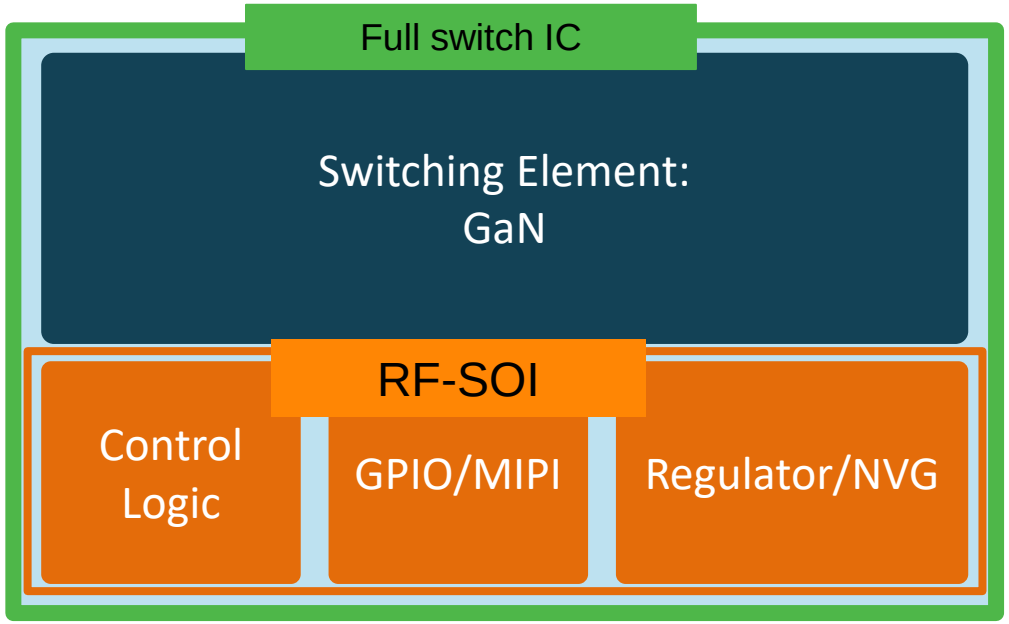
Schematic cross-section of the co-integration method

Photograph top view

- 3D Integration technique: ***micro-transfer printing (µTP)***
  - Singulated RF GaN coupon printed face-up on top of a finished RF-SOI 8" wafer
  - Redistribution Layer (RDL) making the interconnection between RF GaN HEMT and RF-SOI devices

µTP Advantages for RF switch application

1. High power handling (GaN)
2. Integration and area reduction (SOI)



→ GaN/SOI transistors as switching elements.
→ Control logic, GPIO/MIPI, Regulator and NVG on SOI.

No need for Multi-Chip Module → area ↘↘

3. Improvement of the vertical coupling/isolation to substrate (SOI)
   - See reference [1]

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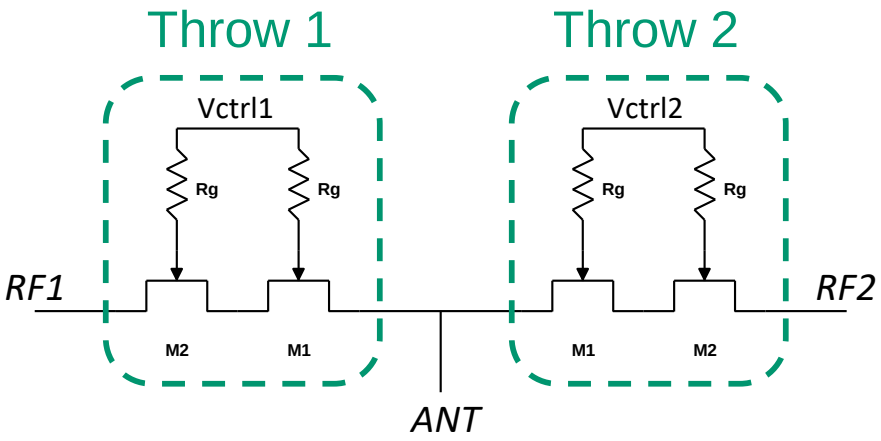
SPDT Specifications and architecture



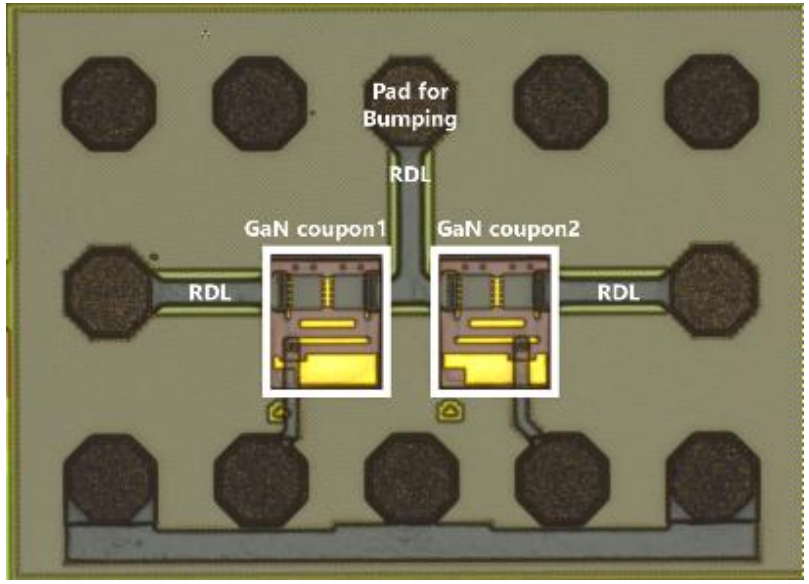
GaN/RF-SOI SPDT architecture

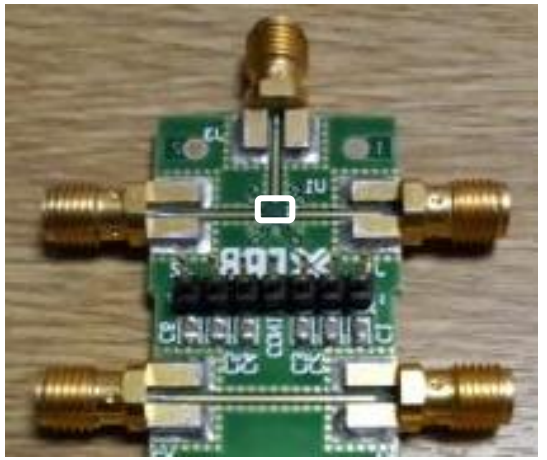
- Architecture: reflective SPDT switch
- Targeted application: antenna tunning & infrastructure
- Specifications
  - Frequency band: DC – 6 GHz
  - **Power handling: 48 dBm (80 V)**
  - Insertion loss <0.9 dB
  - Isolation > 17 dB

- Main switching element is a µTP GaN/SOI HEMT
- One transistor breakdown = 50 V → to reach 48 dBm, two transistors are stacked

SPDT design and implementation

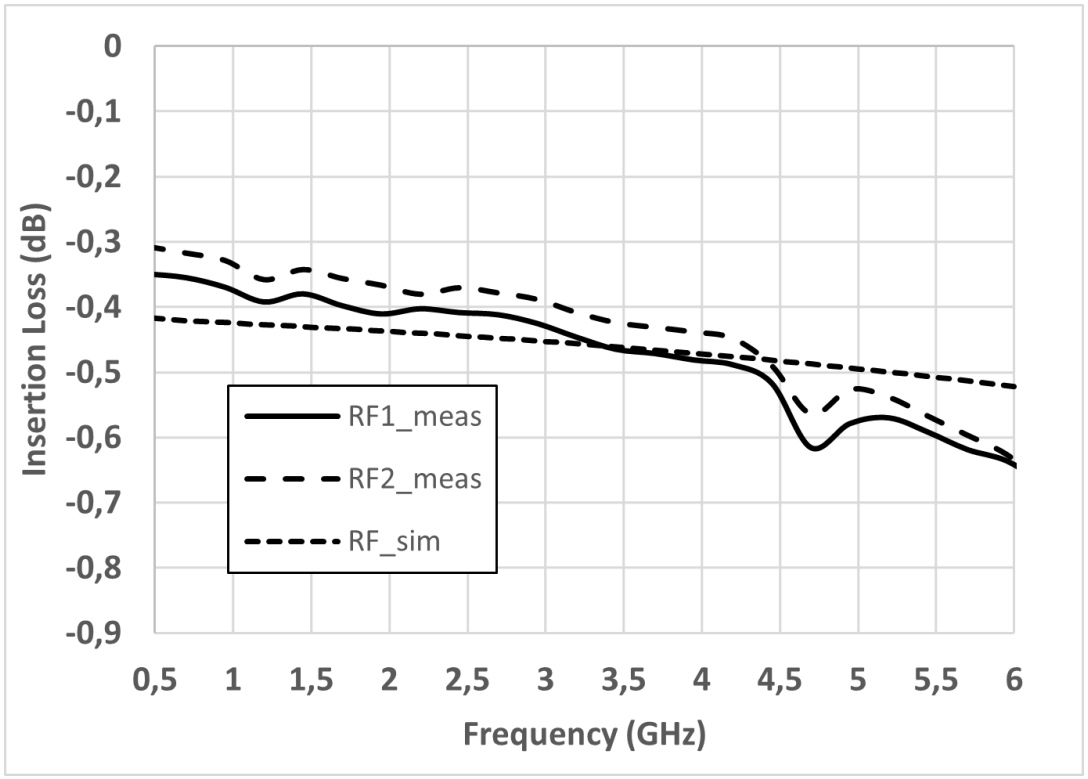
- Symmetrical SPDT with two GaN/SOI coupons
- Each GaN coupon contains:
  - 2 stacked HEMT: 10 fingers of 80 µm each, gate length = 100 nm.
  - Each HEMT has a 20 kΩ resistor on its gate
- Chip bumped on the Cu-RDL pads and mounted on PCB
- A scalar de-embedding is performed using a thru line





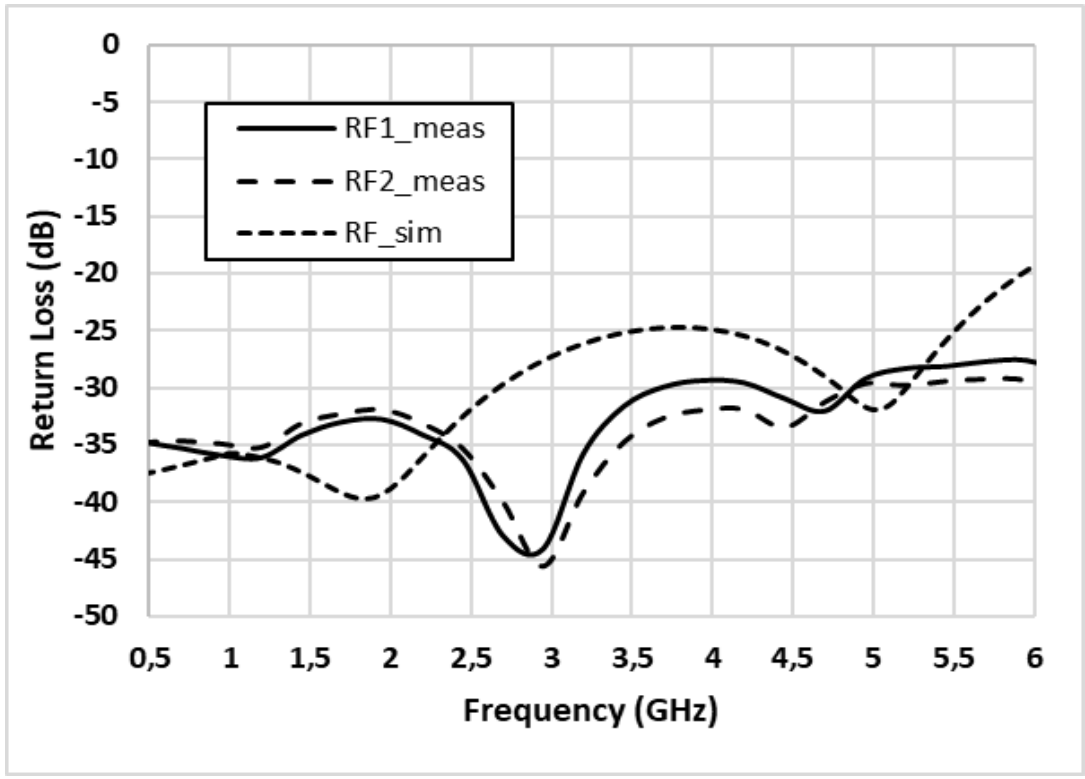
Photograph of the SPDT die (top) and PCB (bottom)

Small-signal characterization results



Insertion loss as function of frequency

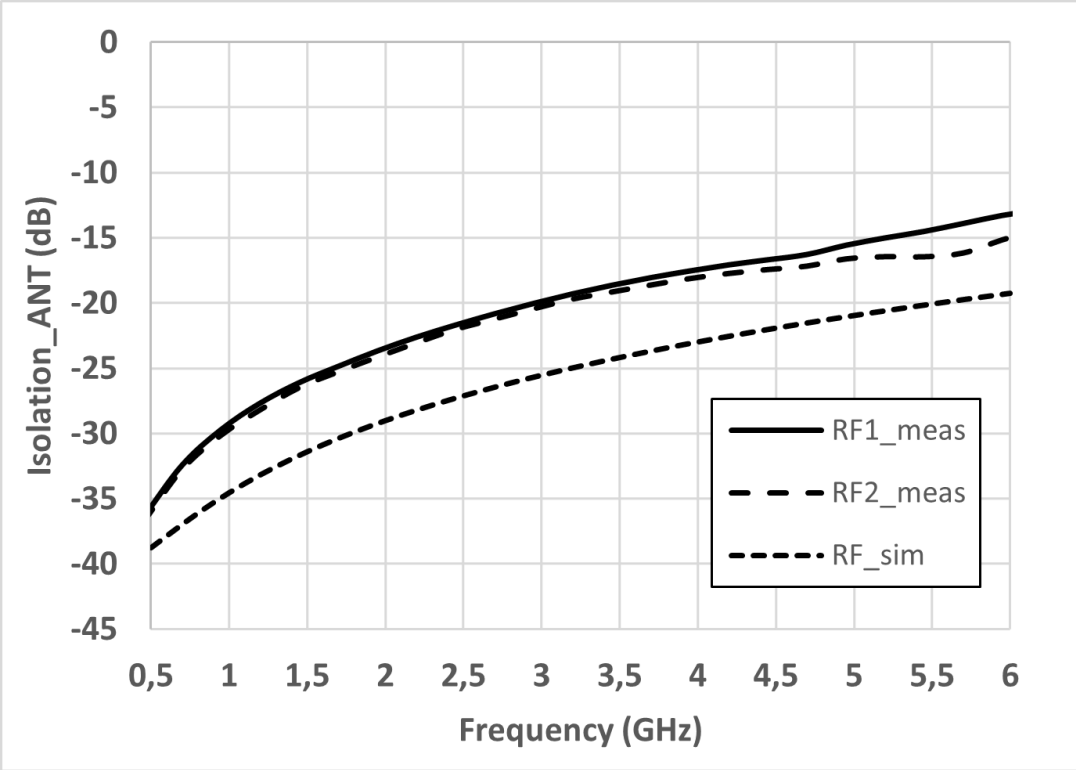
- Insertion loss < 0.65 dB up to 6GHz
- Good agreement with simulation



Return loss as function of frequency

- Return loss < 20 dB up to 6GHz

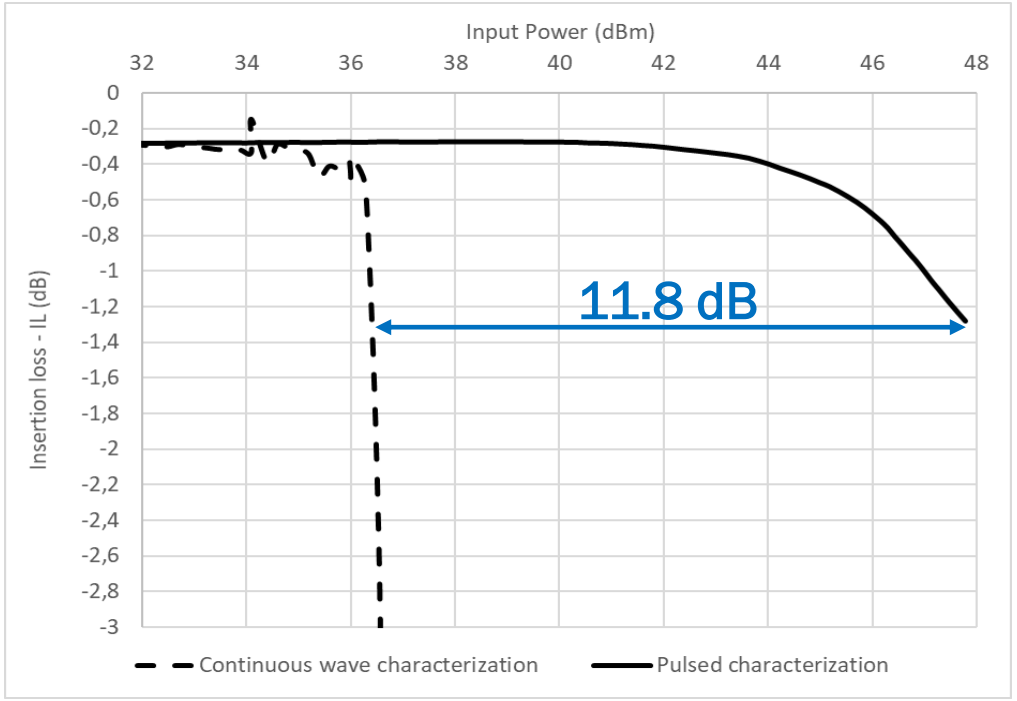
Small-signal characterization results



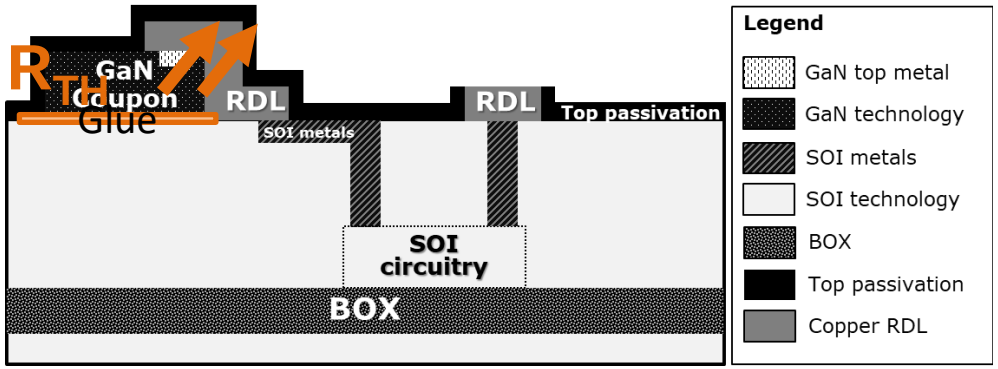
Isolation as function of frequency

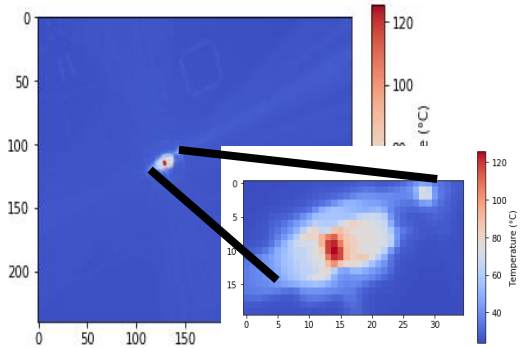
- Isolation ~ 35 dB @0.5GHz & 14 dB @ 6GHz
- 2.5 dB to 5 dB difference with simulation
- Root cause: Coupling to PCB (not simulated & could not be de-embedded)

Large signal characterization results



Insertion loss as function of input power in CW & pulsed modes





Surface temperature characterization with an Infrared camera of a µTP GaN/SOI, dissipated power = 1 W

- Hard breakdown @ 36.2 dBm in CW
- Cause: heat accumulation in the GaN coupon due to underlying adhesive layer & dielectrics
- **1dB compression point in pulsed mode = 48 dBm → main specification achieved**

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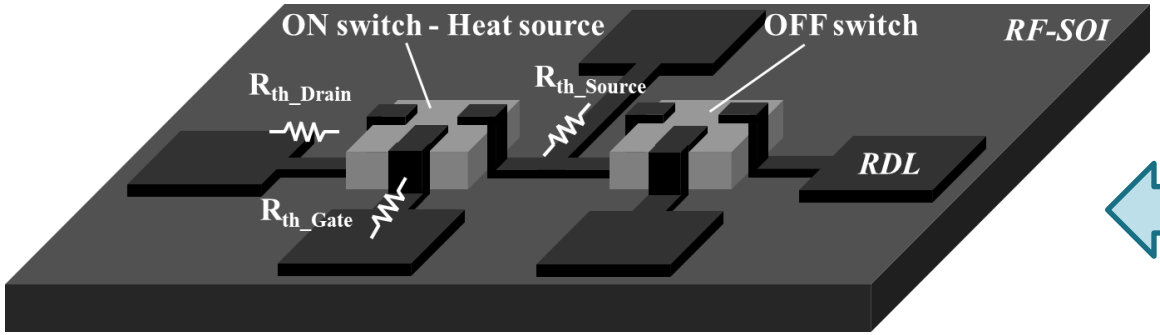
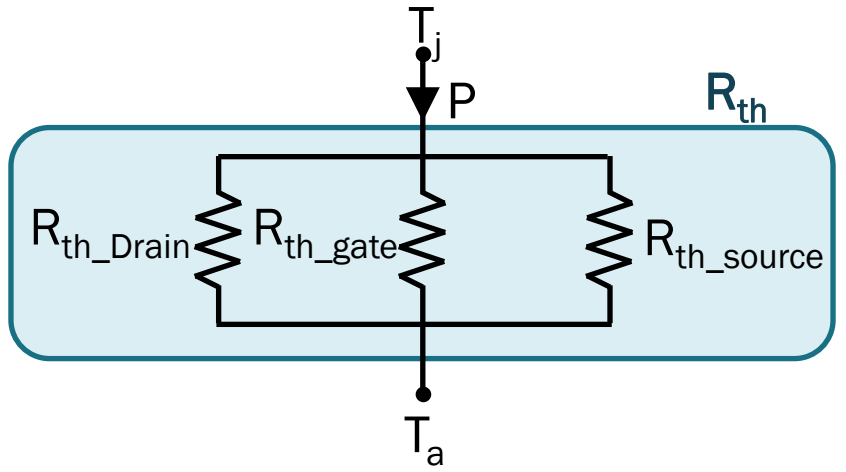
Heat accumulation issue



3D drawing of the GaN/RF-SOI SPDT

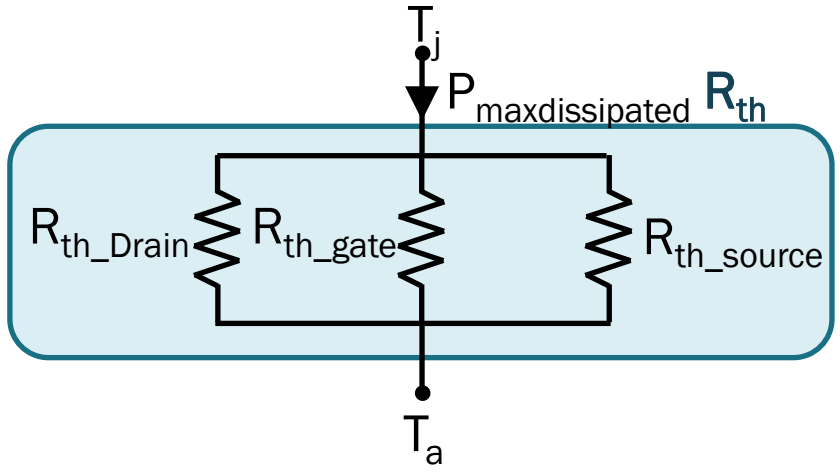


- To model the thermal behavior:
  - Calculation of the GaN coupon R_{th}.
  - Three parallel RDL paths going from the GaN coupon to the PCB I/O's , i.e., drain, source, and gate
- **Calculated R_{th} = 1590 K/W !!**

Copper thermal conductivity = 398 W/(m.K)
Tj: junction temperature
Ta: ambient temperature

Heat accumulation issue

- To confirm the validity of the thermal model,
  - Maximum input power that would cause the destruction of the GaN transistor is calculated



Thermal Ohm's law: $P_{maxdissipated} = (T_j - T_a)/R_{th}$

- Calculated maximum dissipated power is 0.19 W =36.2 dBm
- ***Simulated power matches measurements***

→ This mathematical model can be used for heat accumulation solutioning

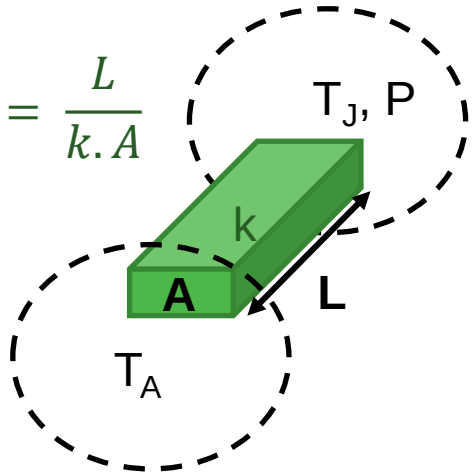
Tj: junction temperature for which the GaN transistor is destroyed
Ta: ambient temperature

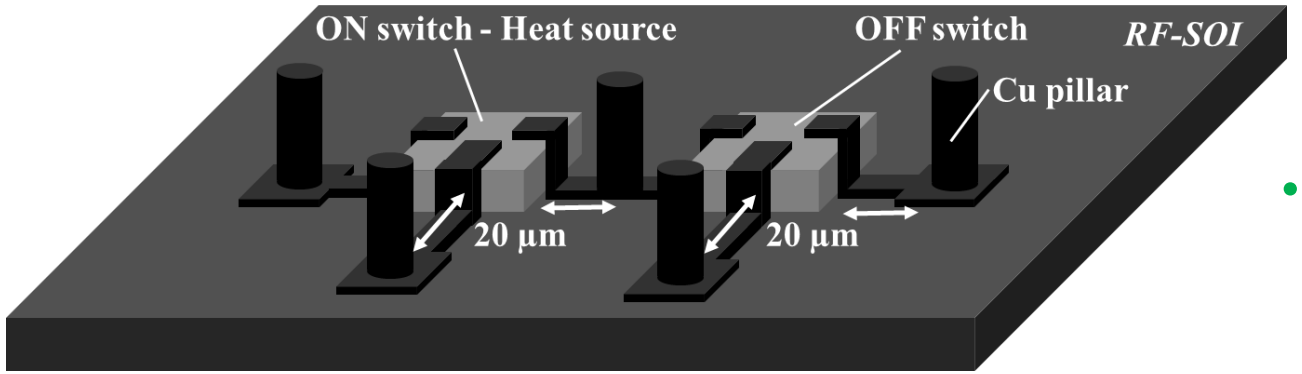
Heat issue solutionning

- Major contributor to Rth is the length (L) of RDL traces
  - L= hundreds of µm, section A= 5µm*36 µm

- To decrease Rth,
  - L (RDL) is decrease to 20µm thanks to copper pillar use
  - Thermal conductivity copper pillar is ~ 6 times higher than bumps
  - Thick SOI metal layers stacked with RDL: new A = 14.5 µm*36 µm

$$R_{th} = \frac{L}{k.A}$$





3D drawing of the GaN/RF-SOI SPDT with optimized layout for thermal dissipation

- New Rth = 40 K/W !!

→ Achieving 48 dBm in CW become possible

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Conclusion

- A state of the art high power SPDT switch presented
- Benchmark with a commercially available GaN SPDT from Tagore

	Insertion loss (dB)			Return loss (dB)			Isolation (dB)			Power Hand-ling (pulsed)
	0.8GHz	2.6GHz	6GHz	0.8GHz	2.6GHz	6GHz	0.8GHz	2.6GHz	6GHz	
This work	0.33	0.4	0.64	35	40	29	32	22	14	48
TS7225FK [2]	0.35	0.45	0.9	25	25	13	45	32	17	45

- SPDT performance design takes advantage of µTP of RF GaN on RF-SOI

Conclusion

- µTP offers excellent electrical isolation but limits the GaN coupon heat dissipation
- A solution based on mathematical model presented, allows achieving 48dBm in CW
- On-going activities: thermal model and simulation flow development [references 2-3]
- Next steps: cooling techniques evaluation and implementation

References

1. F. Drillet et al., RF Small and large signal characterization of a 3D integrated GaN/RF-SOI SPST switch. *International Journal of Microwave and Wireless Technologies*, 2021, *13*(6), 517-522.

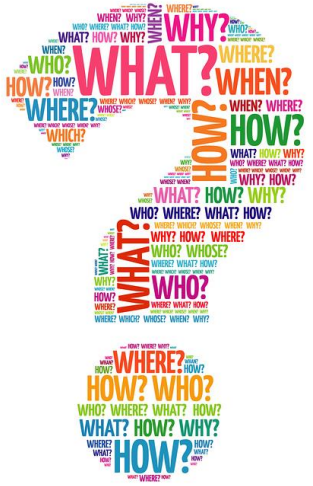
2. https://www.tagoretech.com/PartNumber/ts7225fk.pdf

3. T. -D. Nguyen et al., *Measurement and simulation of the three-dimensional temperature field in an RF SOI chip.* 27th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC). IEEE, 2021. p. 1-5.

4. I. H. Dunn et al., *Experimental three-dimensional thermal mapping of a GaN on RF-SOI chip. 28th International* Workshop on Thermal Investigations of ICs and Systems (THERMINIC). IEEE, 2022. p. 1-5.

Thank you for your attention!

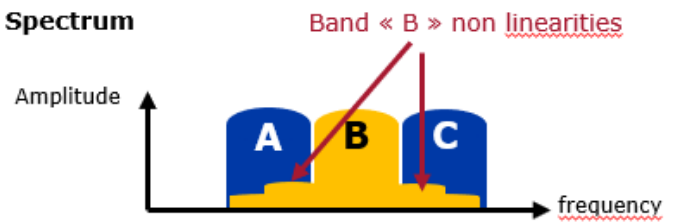
Any question



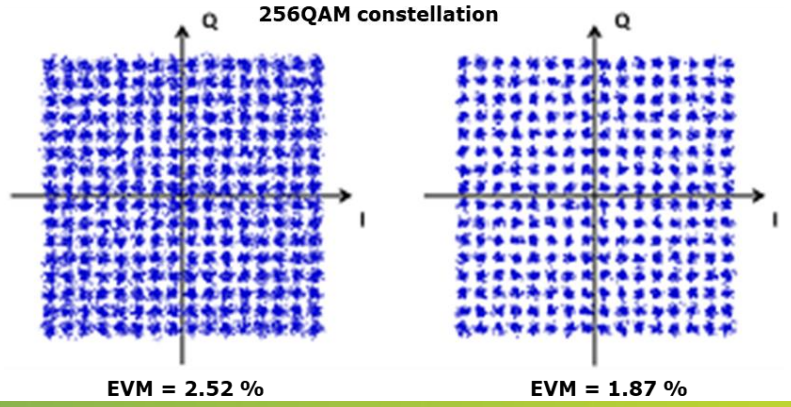
To achieve these performances (3GPP, release 15):

- Use of millimetre wave (mmWave) frequencies for larger bandwidth (BW up to 400 MHz)
- Use of MIMO and beamforming: smaller circuit footprint → Higher power density & efficiency
- Increase number of subcarriers (up to 3276 (1201 max in 4G) with a spacing of 60kHz, 120 kHz, 240 kHz for mmWave & 15kHz, 30 KHz, 60kHz for sub-6GHz)
  - Better linearity is needed.
  - More selectivity and configurability for filters

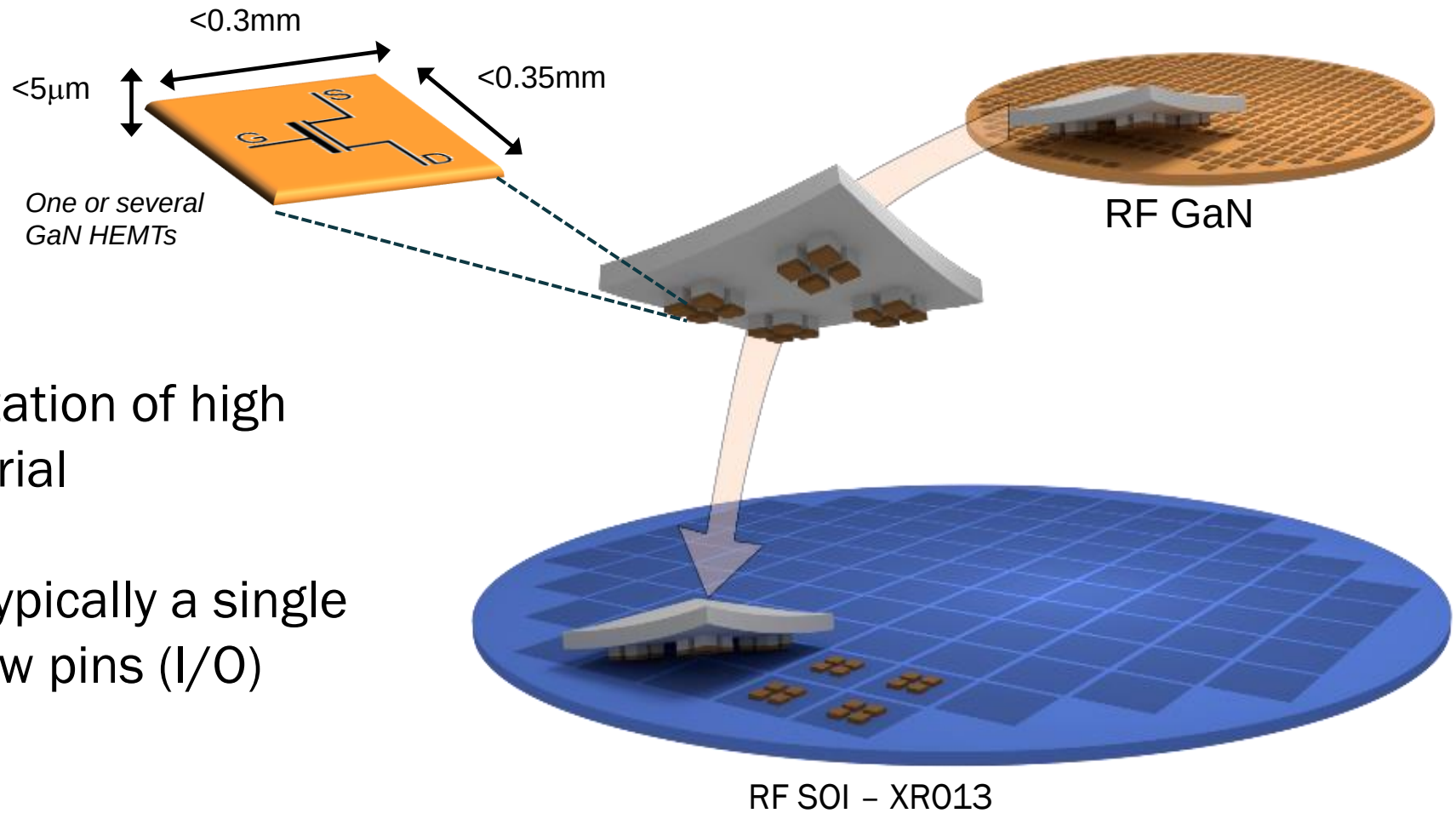
    => more losses => Higher power for Power Amplifiers & Switches.



- Use 256 QAM modulation
  - EVM required 256QAM for 5G < 3%
  - Better S/N is needed
    - Lower noise & Higher linearity



RF GaN micro-transfer printing on RF-SOI



- Efficient area utilization of high value source material
- Coupon contains typically a single component with few pins (I/O)

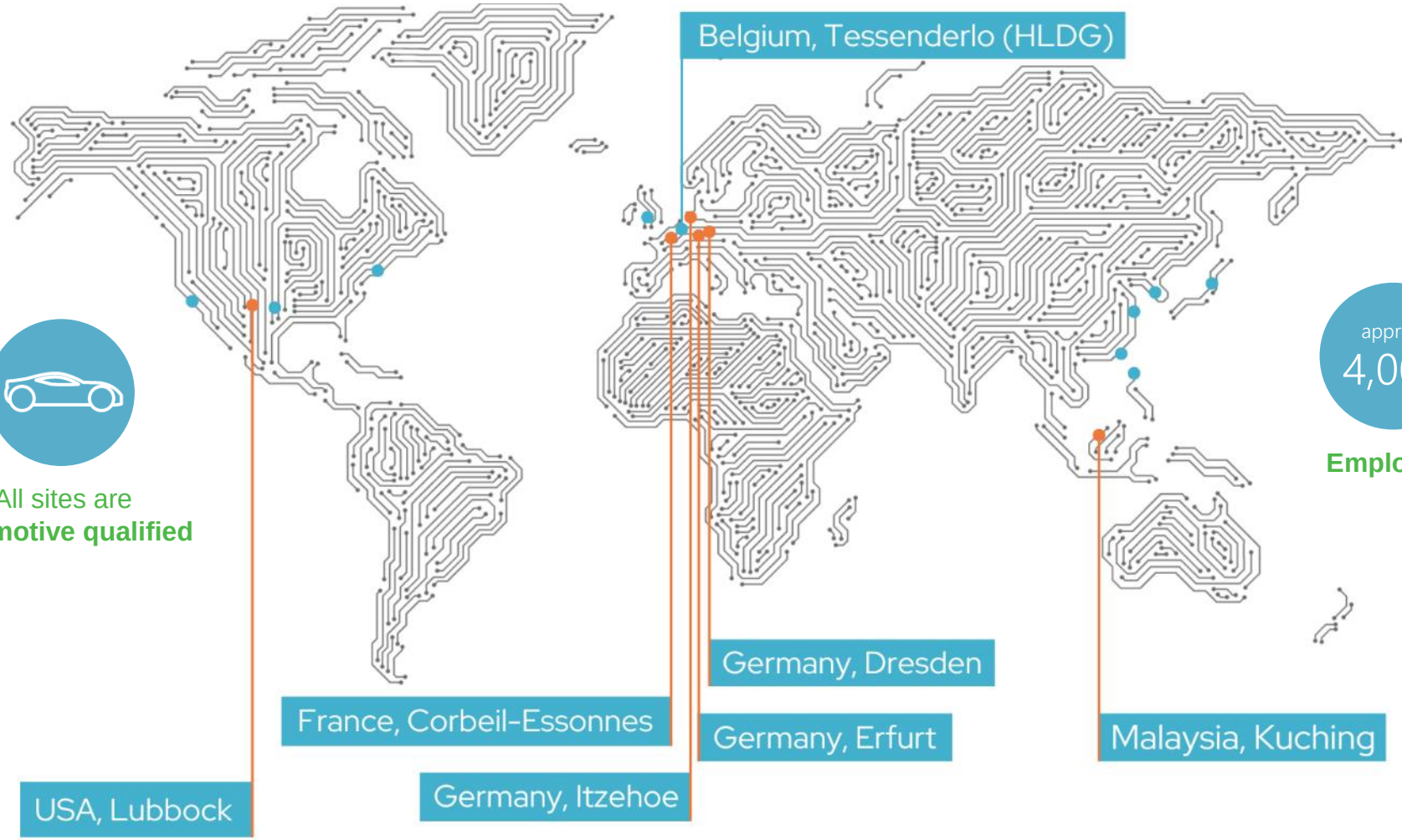
C. A. Bower, M. Meitl and D. Kneeburg, "Micro-Transfer-Printing: Heterogeneous integration of microscale semiconductor devices using elastomer stamps," *SENSORS, 2014 IEEE*, 2014, pp. 2111-2113, doi: 10.1109/ICSENS.2014.6985454.

Transfer-Printing at X-FAB: A novel approach for wafer-level integration, Sebastian Witch, X-FAB technology conference 2022

X-FAB at a glance

6
Manufacturing facilities

100,000
Wafer starts per month*



All sites are **automotive qualified**

approx. **4,000**
Employees

420
Customers in 4 key markets

735 million $
Revenue 2022

Fabs/subsidiaries Sales offices

* 200mm equivalent