WE2D-3

A Novel Ultra-Broadband Low-Loss Bond-Wire Interconnect Design Concept Applied to a 2 GHz to 135 GHz Substrate-to-Substrate Interface

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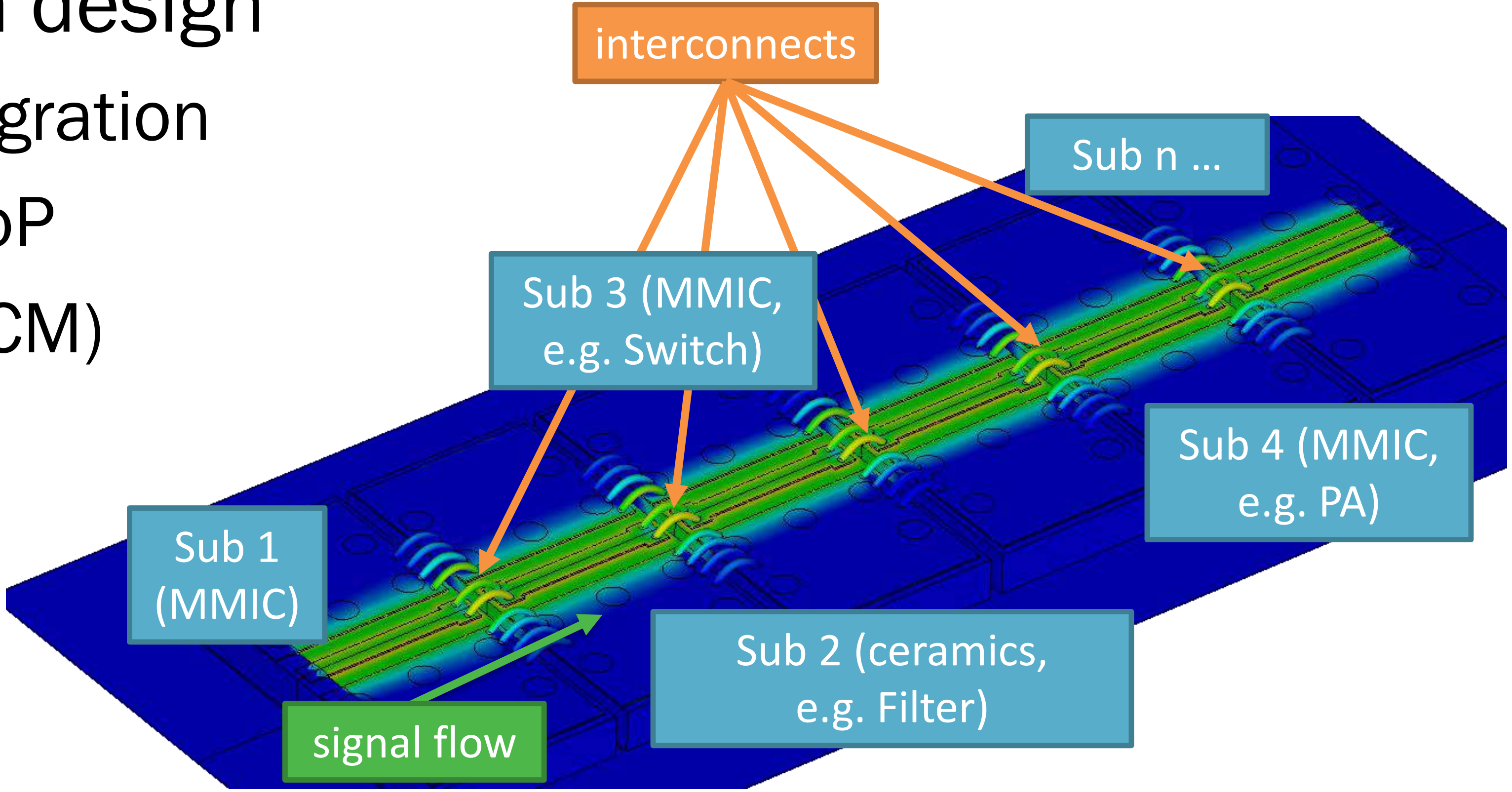
Motivation

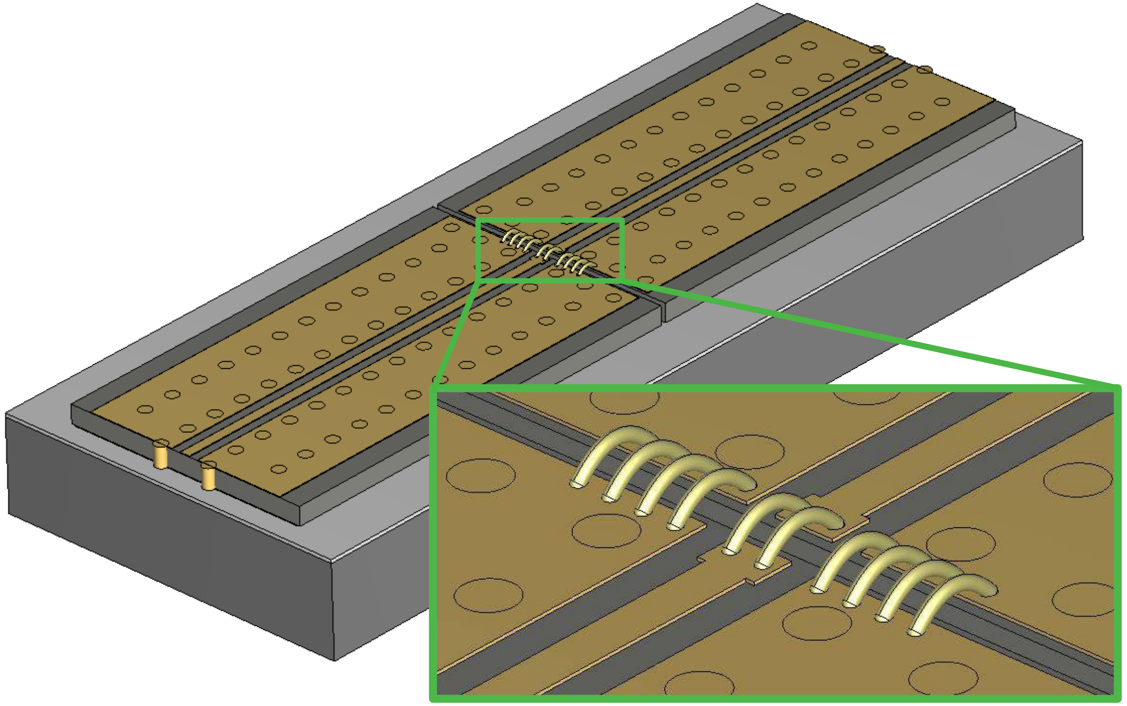
- Combination of different semiconductor processes
  → Increase system performance
- Heterogeneous system design
  – Wafer level system integration
  – Chiplet-approaches/ SoP
  – Multi-Chip-Modules (MCM)
  – ...

→ mmW-interconnects enable heterogeneous system **design**

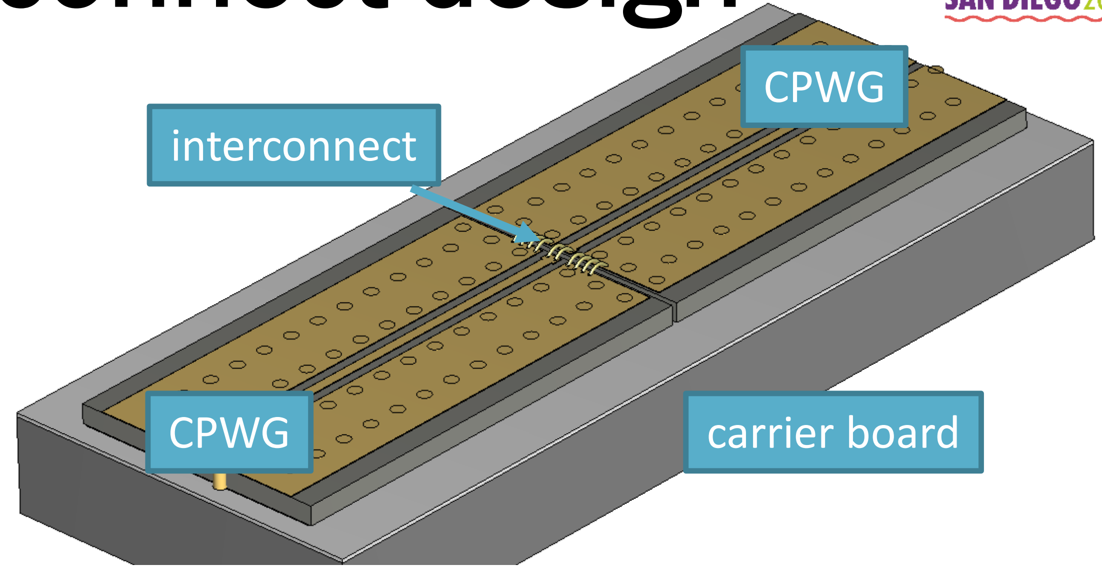


Outline

- Motivation
- Assembly & interconnect design
- Measurement characterization
- Comparison with literature
- Conclusion

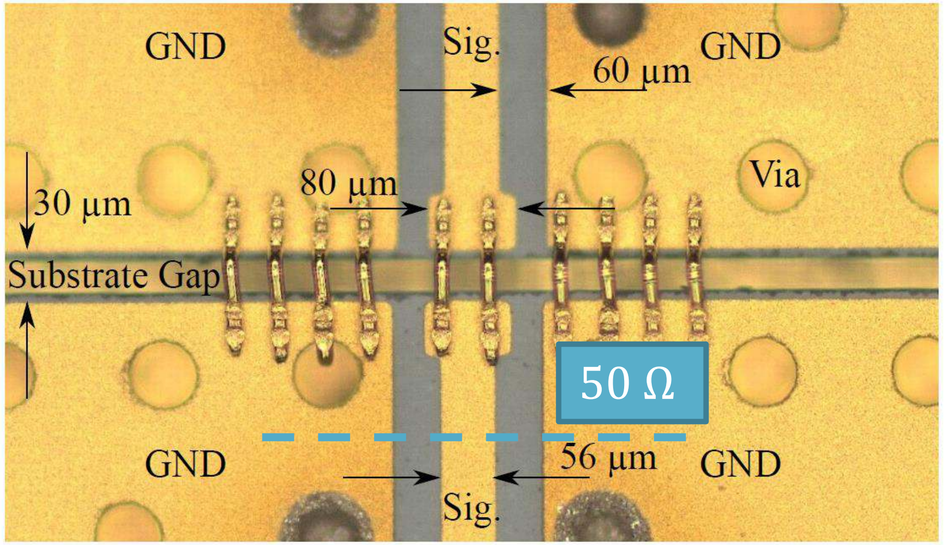


Assembly & interconnect design



Substrate selection:

- Ceramics
  - 4 mil ≈ 100 μm
  - ε_r = 9.7, tan(δ) = 10^{-4}
- Conductor material: Au ($4\mu m$)
- 50 Ω Grounded Coplanar Waveguide



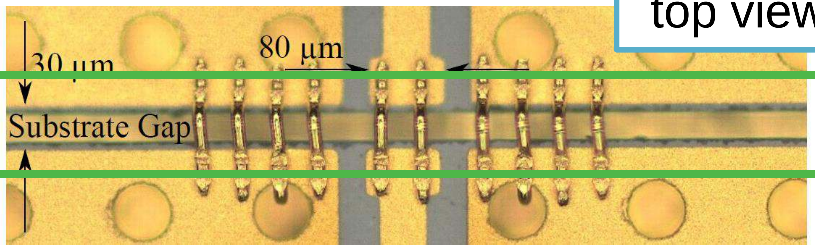
Footprint of ceramics = footprint of MMIC
→ Easy transfer to MMIC

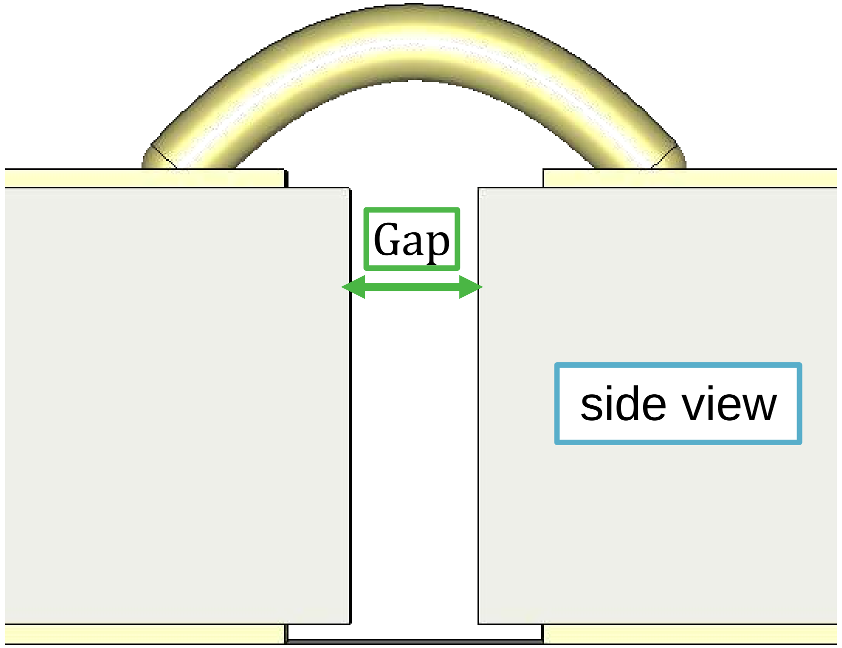
Connecting Minds. Exchanging Ideas.

Assembly & interconnect design

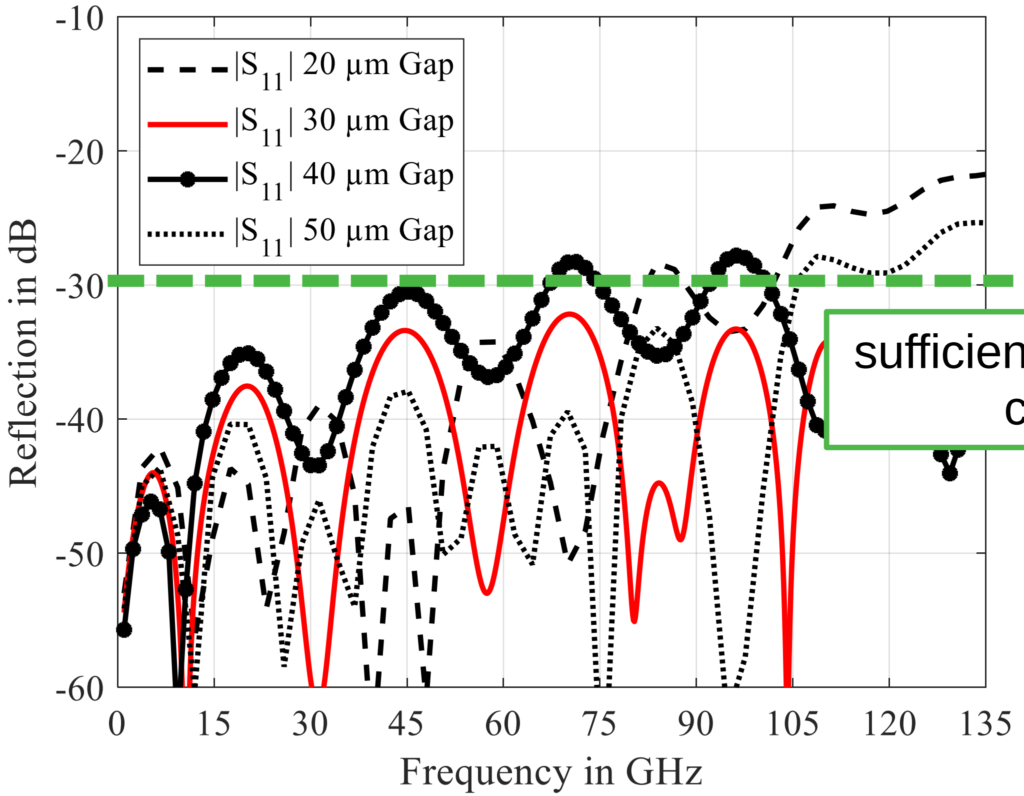
Gap selection:

top view





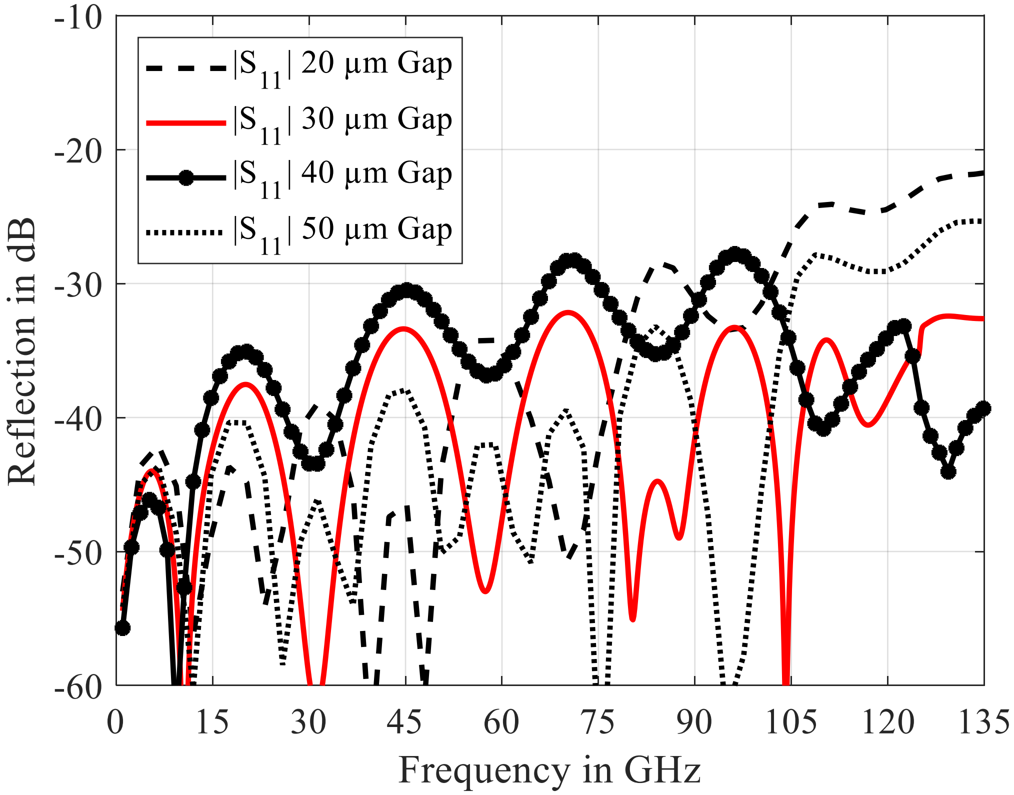
side view



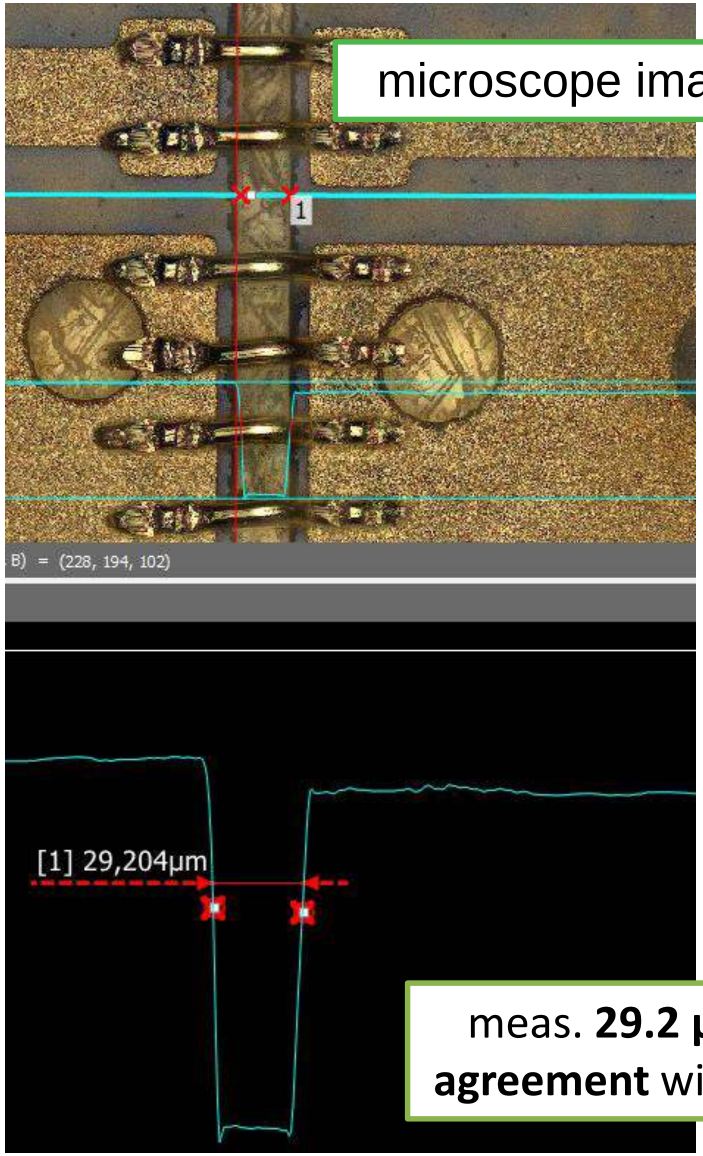
sufficient performance criterion

Assembly & interconnect design

Gap selection:



→ 30 µm **sweet-spot** mechanical **margin** ⇔ **EM-performance**

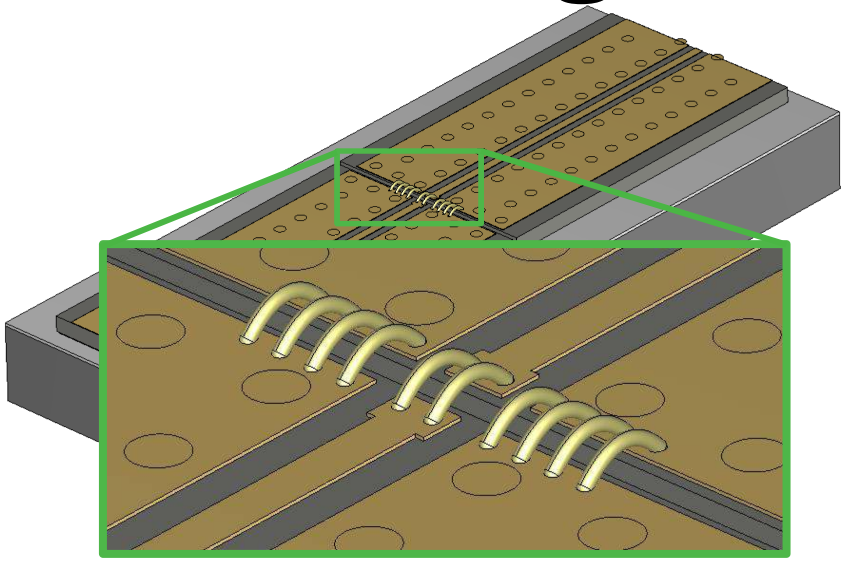


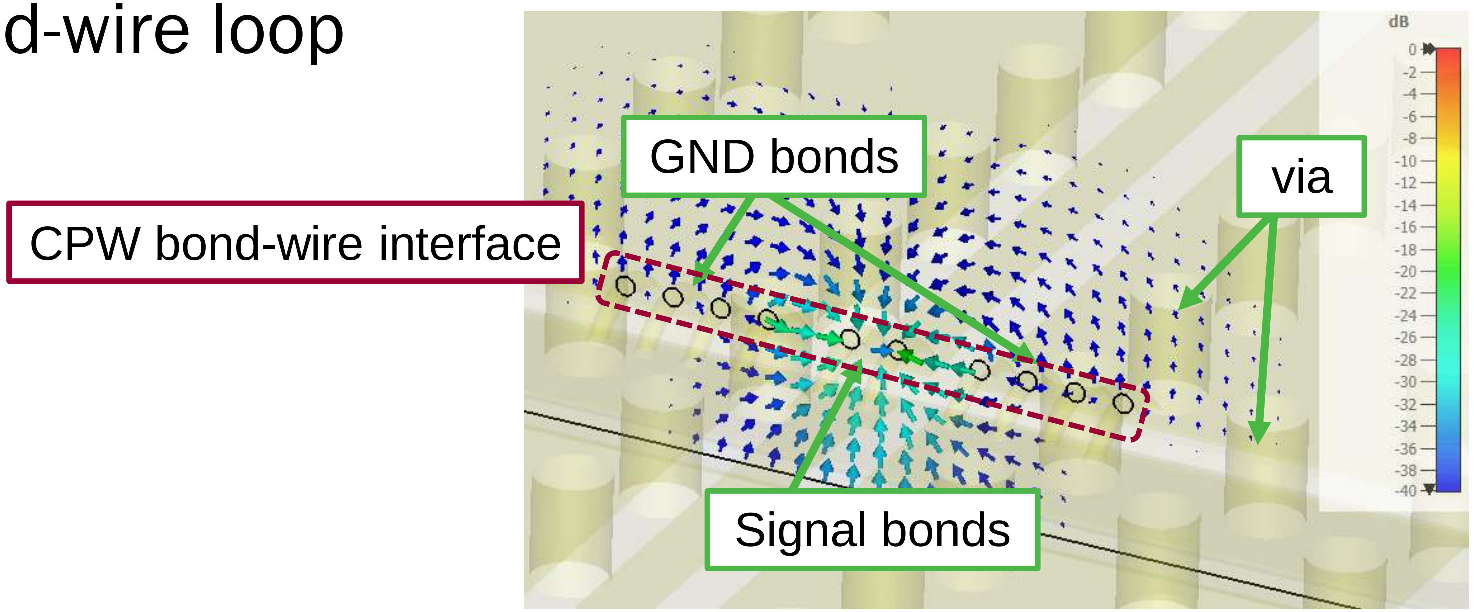
meas. **29.2 µm** in **perfect agreement** with **target** value

Assembly & interconnect design

Design of bond-wire interface:

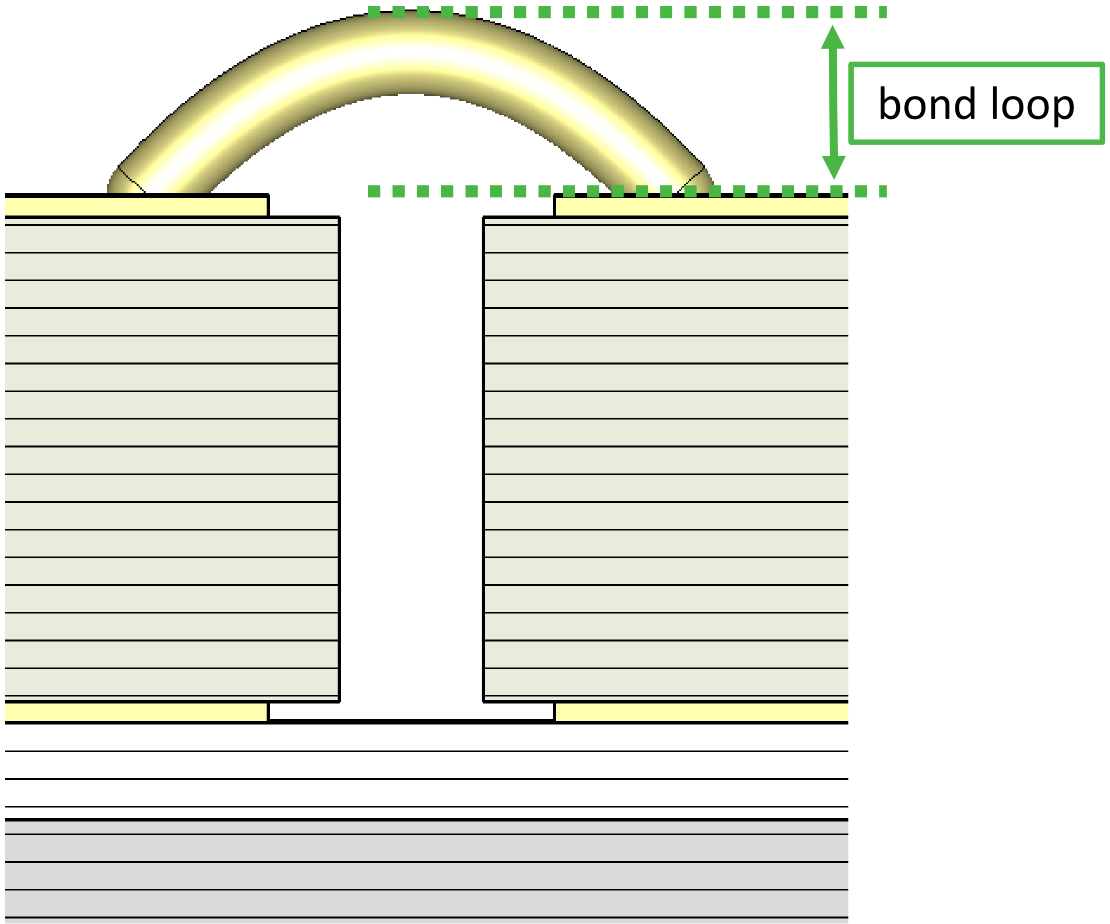
- Two parallel signal bonds
- Four GND-bonds (each side)
- Landing pads (80 x 60 µm^2)
- Critical parameter: bond-wire loop

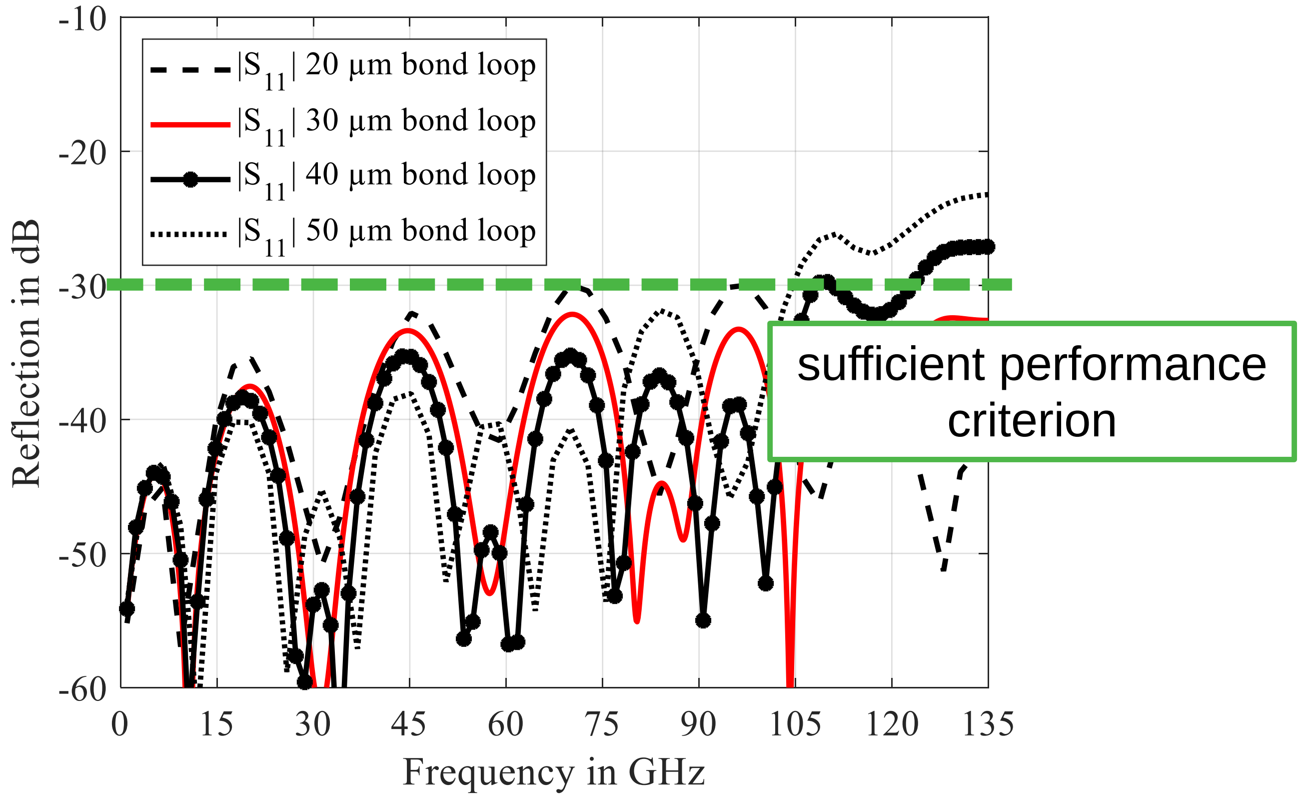




Assembly & interconnect design

Design of bond-wire loop:





Assembly & interconnect design

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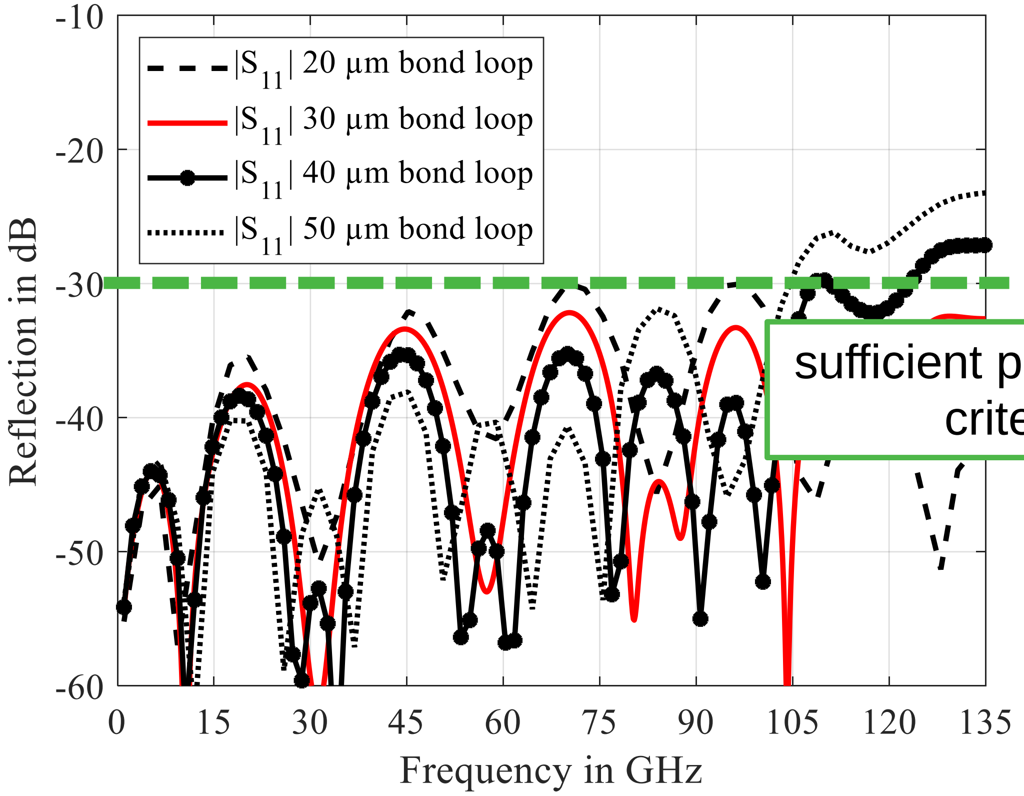
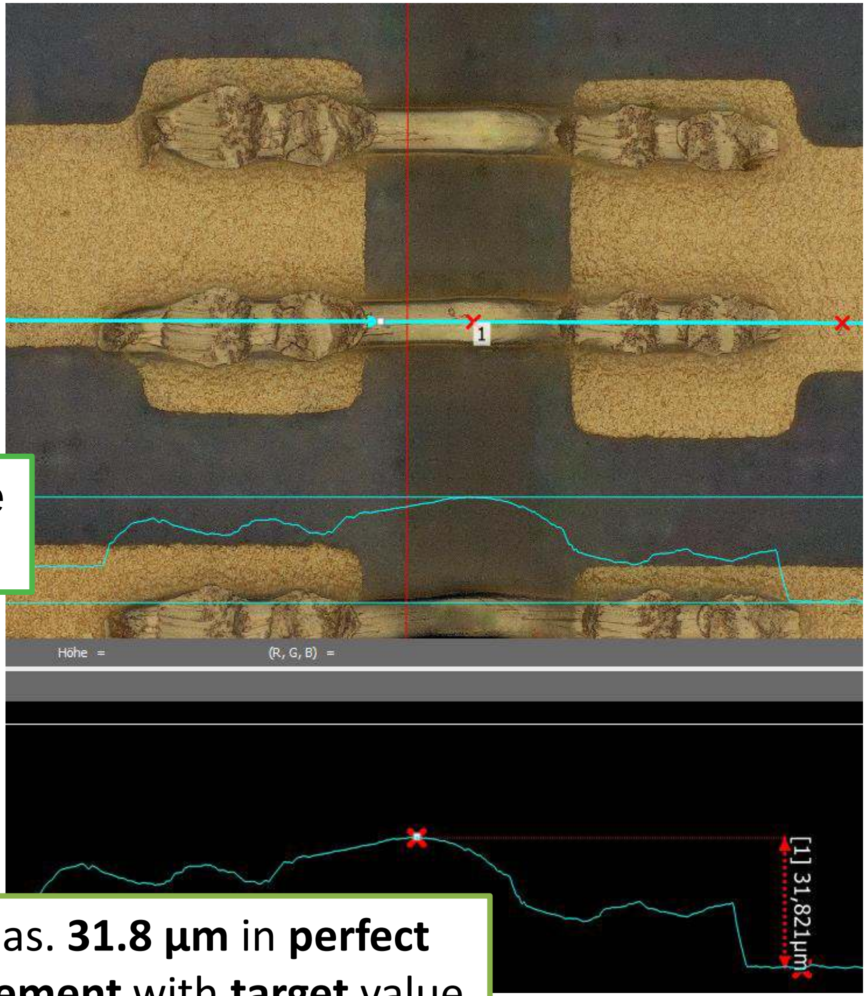


sufficient performance criterion



meas. **31.8 µm** in **perfect agreement** with **target** value

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- Comparison with literature
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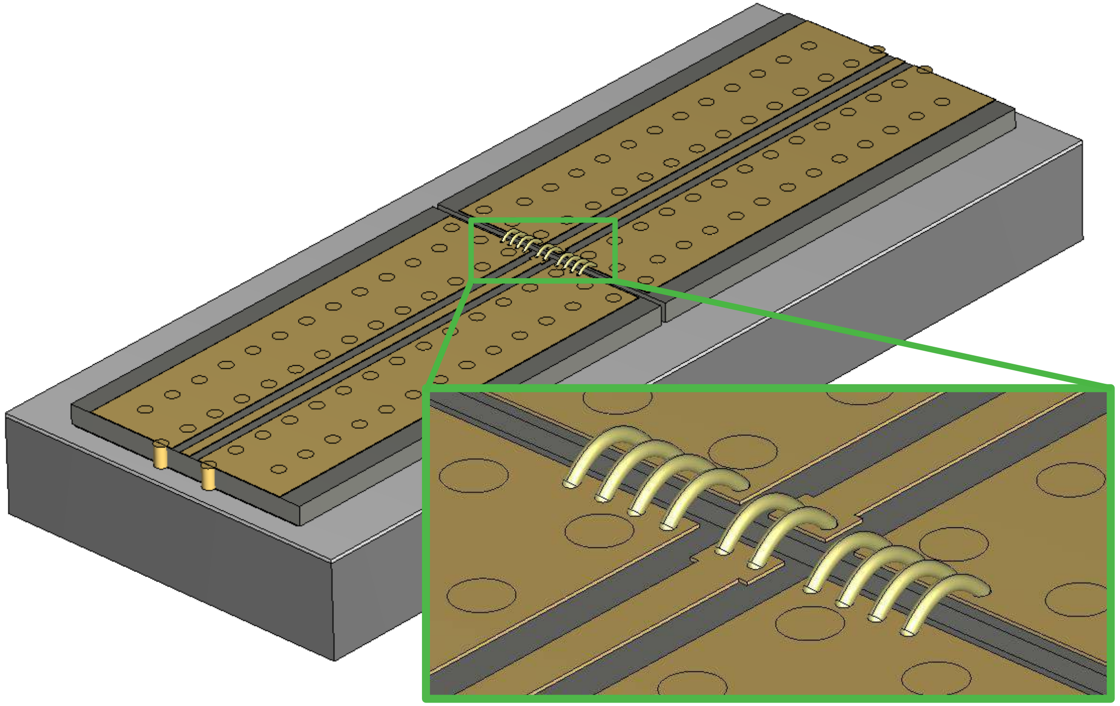
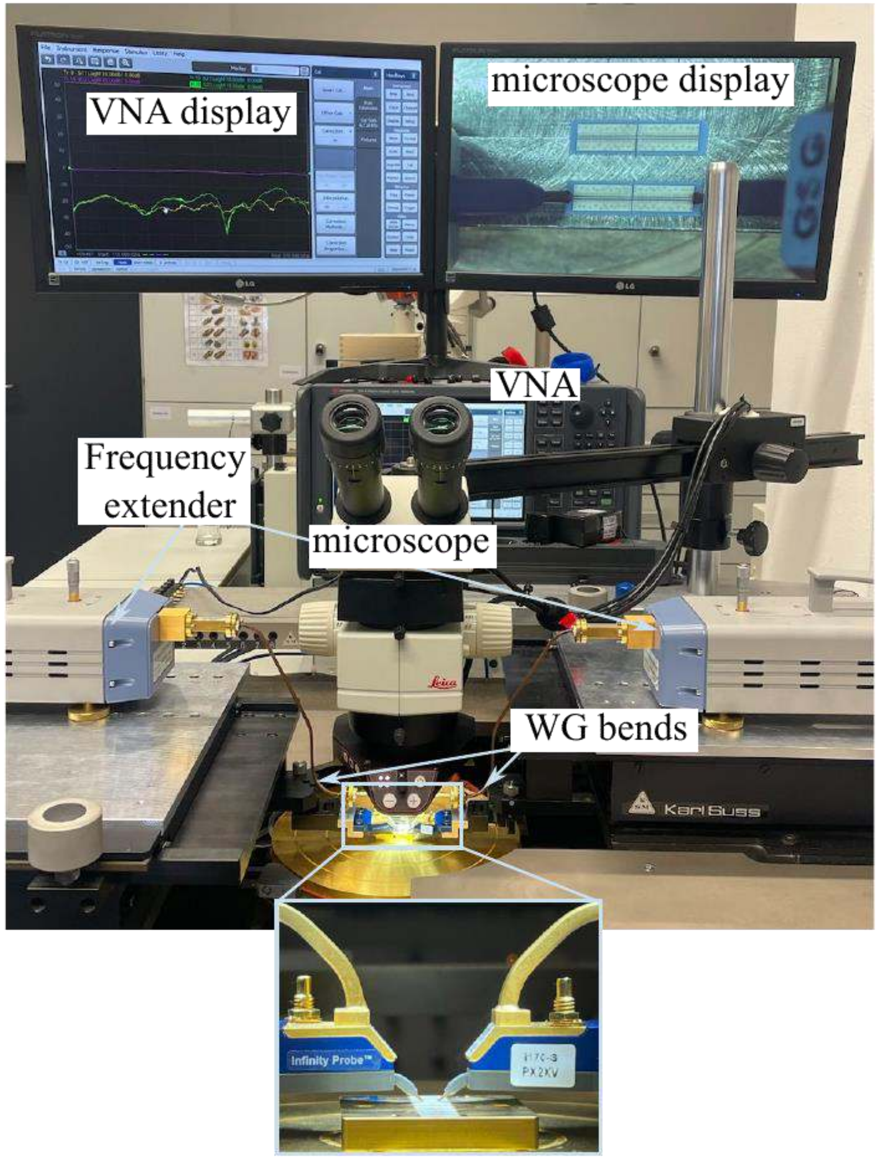


Measurement characterization

- PNA-X VNA
- **Ultra-broadband** meas. setup:
  - 2-110 GHz: 1 mm – Coaxial setup
  - 110-140 GHz: frequency extender

  ➔ Frequency band: **2-140 GHz**
- Infinity GSG probes
- Custom-made TRL calibration kit

  ➔ Reference plane on ceramics



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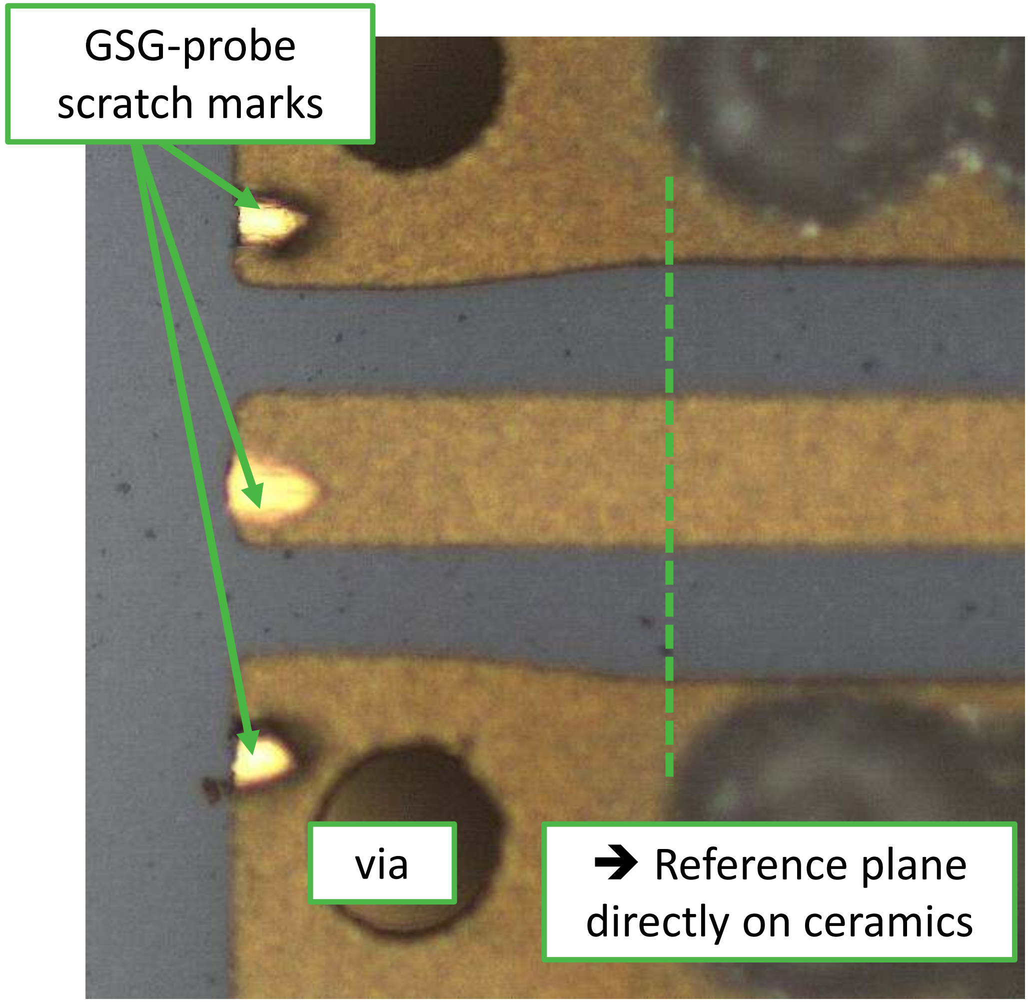
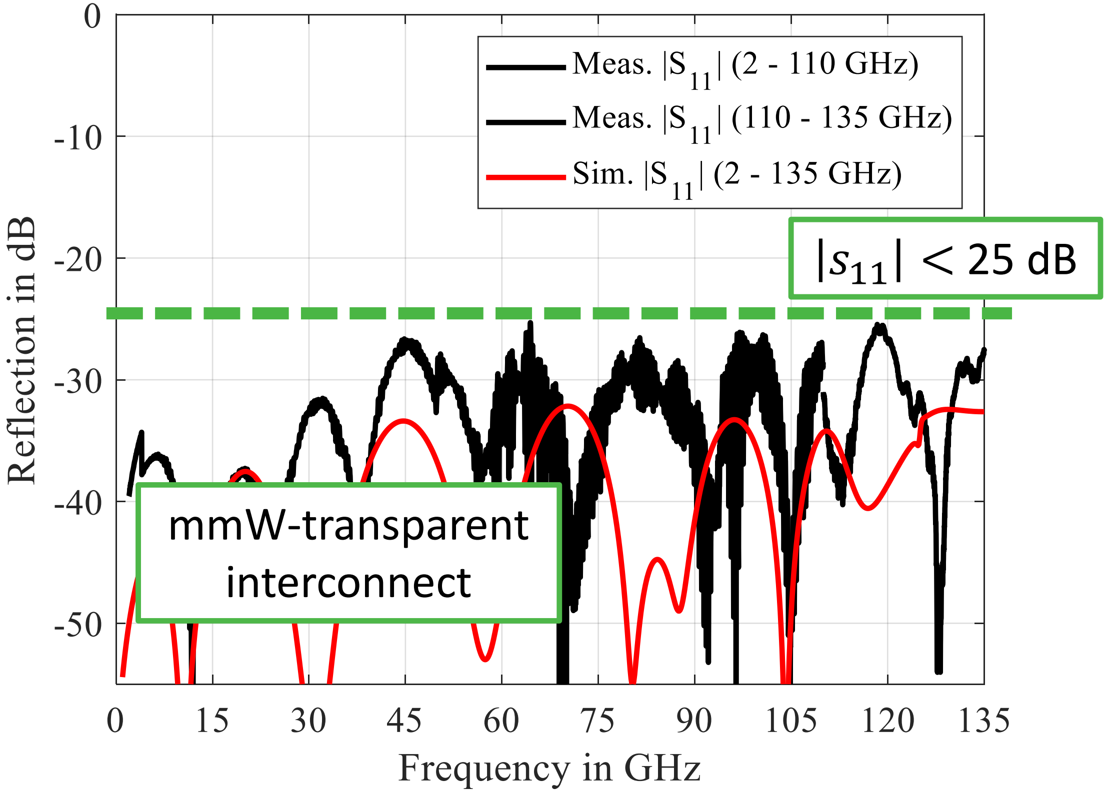
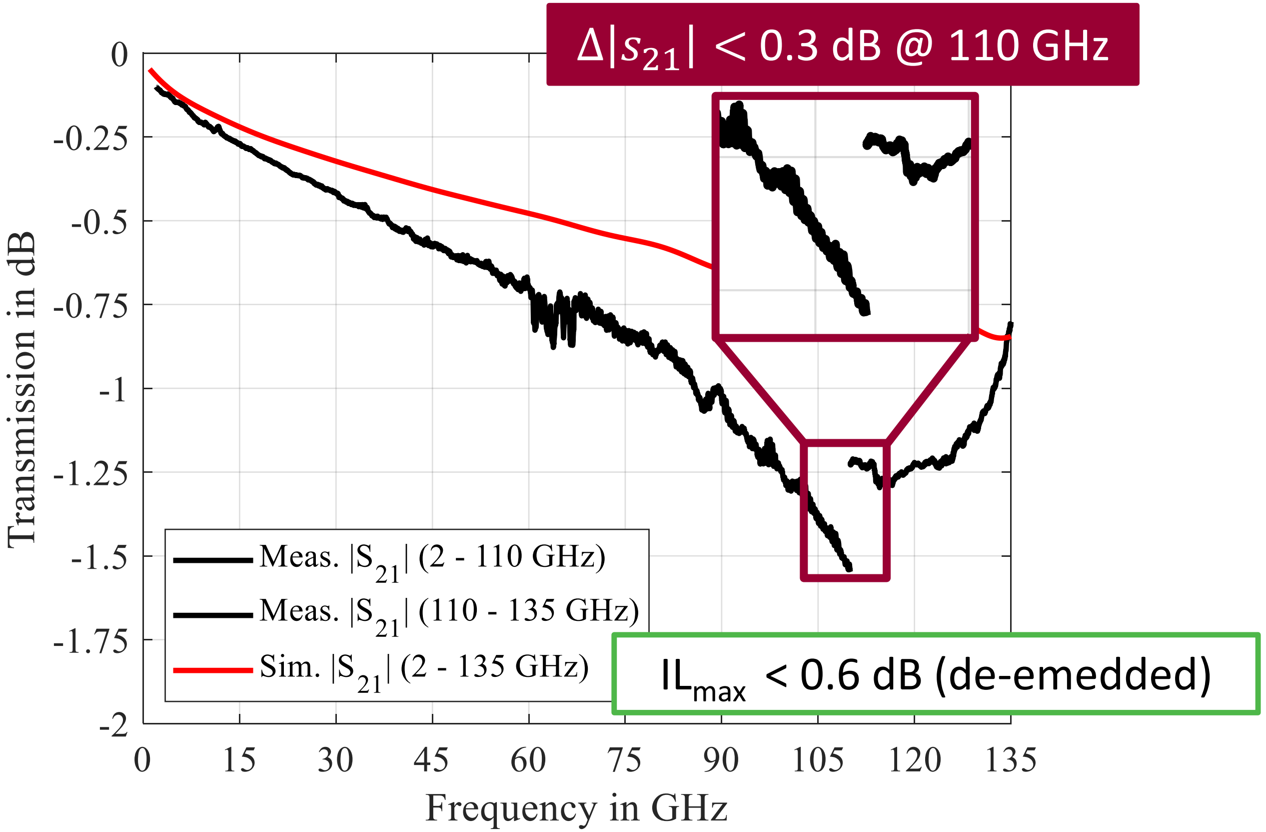
  - ➔ **Reference plane** on **ceramics**



Measurement characterization

Measurement results:





→ **Perfect match** of **simulation** and **measurement proves** working **interconnect design**

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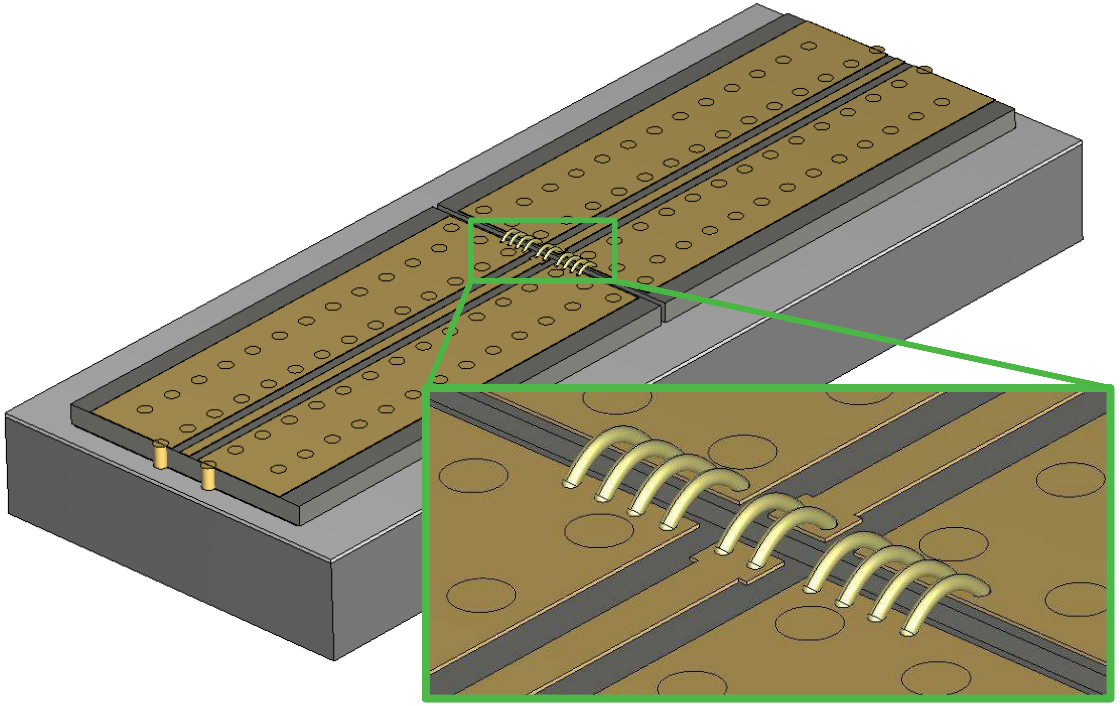

Comparison with literature

Reference	meas. match. bandwidth	meas. match. level	max. meas. insertion loss	interconnect technology
[1]	84 GHz	RL > 13 dB	IL < 3 dB	bond-wire
[3]	500 GHz	RL > 15 dB	IL < 1.8 dB (b-t-b)	flip-chip
[4]	100 GHz	RL > 12 dB	not known	flip-chip
[5]	10 GHz	RL > 10 dB	IL < 3 dB	bond-wire
[6]	100 GHz	RL > 7.5 dB	IL < 2.5 dB	bond-wire
[7]	220 GHz	RL > 8 dB	IL < 2.5 dB	quilt-package
This work	**> 130 GHz**	**RL > 25 dB**	**IL < 1.6 dB IL < 0.6 dB (de-embedded)**	**bond-wire**

→ Benchmark in return loss, comparable to flip-chip approaches
→ **Enable bond-wire interconnect above 110 GHz with excellent EM-performance**

Conclusion

- **Ultra-broadband** bond-wire **interconnect**
- **Rethinking** of **interconnect interface**
  → **Elimination** of **current limitations** (BW and IL)
- **“Auto. assembly technology"-ready**