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SAN DIEGO 2023

We3A-1

A 10-Gb/s 275-fsec Jitter Charge-Sampling CDR for Quantum Computing Applications

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QuTech

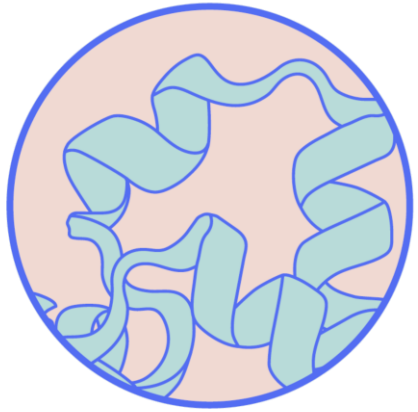
Presentation Overview

- **Introduction**
  - Motivation & Challenges
- **Proposed Clock and Data Recovery System**
  - Charge Sampling Phase Detector
  - Impact of Data Dependency on the Performance of the Proposed Phase Detector
  - Clock Retiming Alignment
- **Measurement Results at 300K & 4.2K**
  - Power Consumption
  - Recovered Eye Diagram and Phase Noise
  - Jitter Transfer and Tolerance
  - Comparison Table
- **Conclusion**

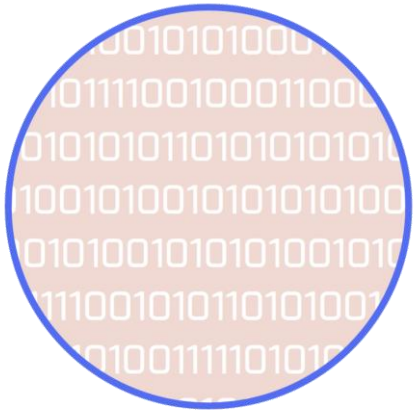
Why Quantum Computing?

Encryption/decryption

Protein folding

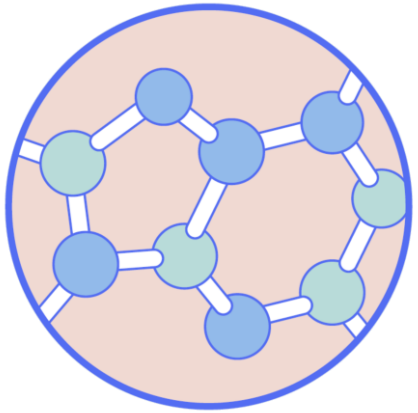


Big data

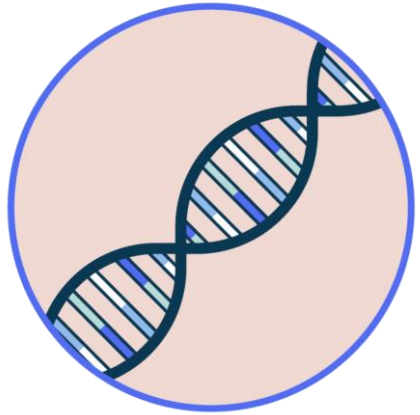


Drug synthesis

Molecule simulation

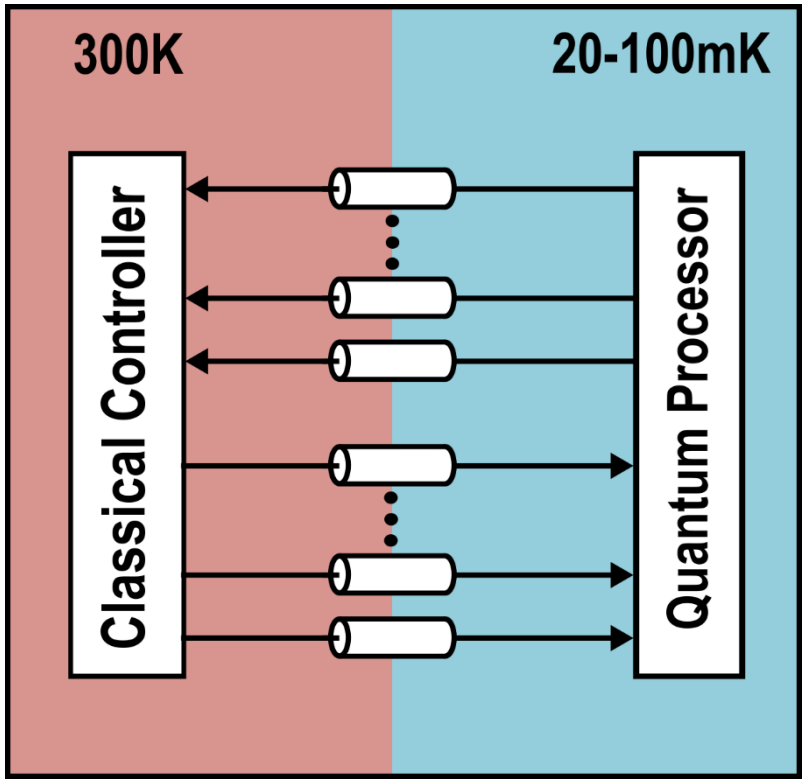


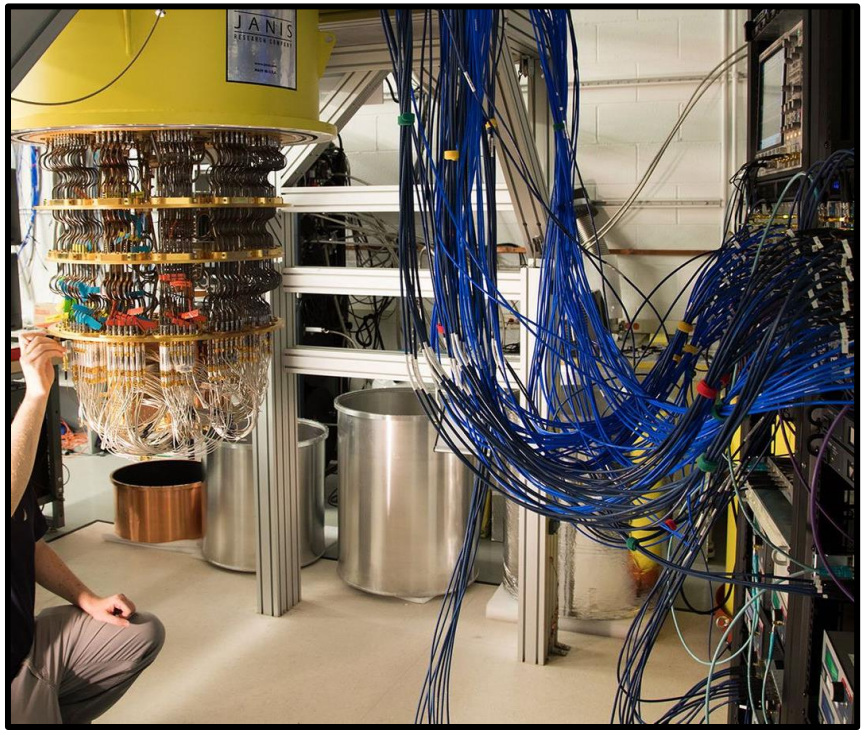
DNA analysis



Current State-of-the-Art Quantum Computer

- Direct connection between each quantum bit at milli-Kelvin stage and its control/readout electronics at room temperature
- Scalability limited by interconnect

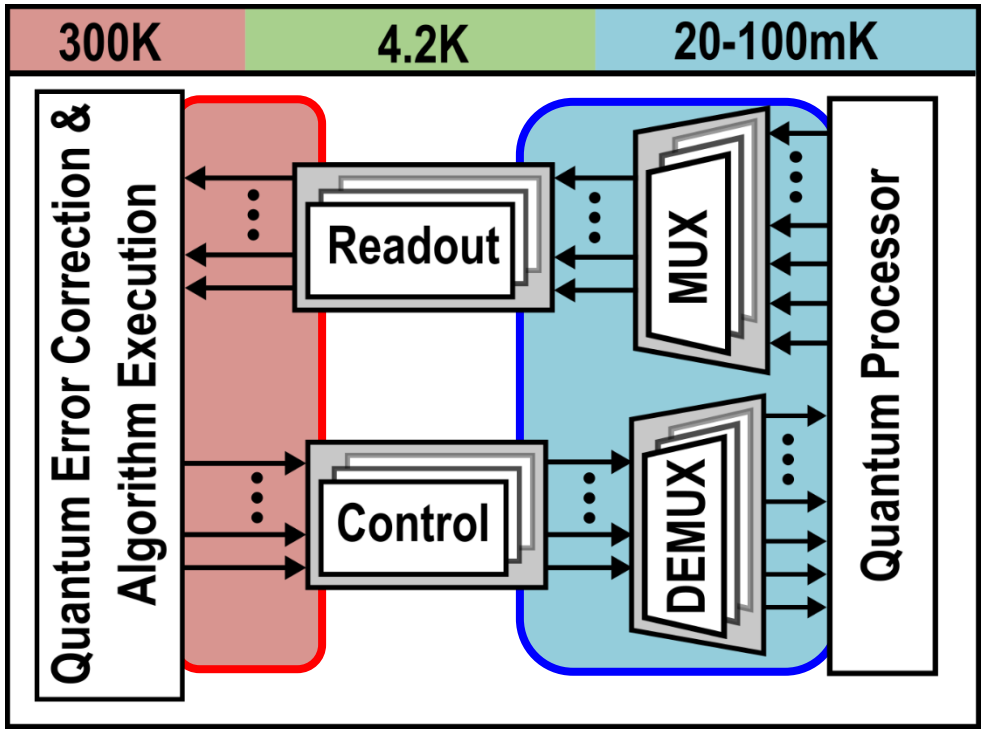


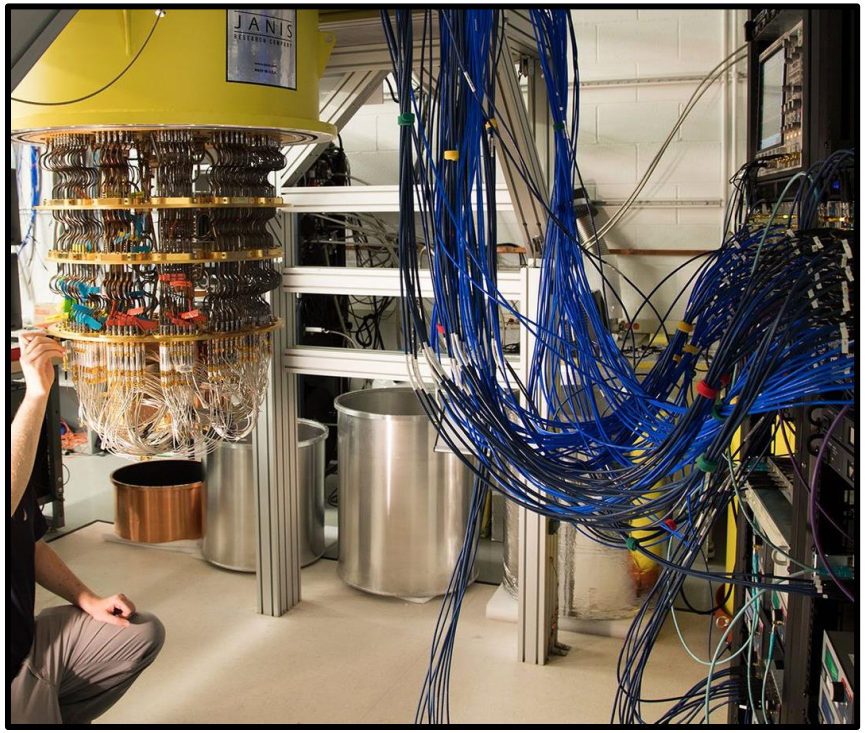


[Photo: Google's 72-bit quantum processor]

Need for Cryogenic Electronics

- Current proposals for scalable quantum computers
  - MUX and DEMUX at milli-Kelvin to perform time multiplexing of qubit control/readout lines
  - Cryogenic control and readout circuits at 4.2K to communicate outside the fridge with digital signals rather than sensitive analog signals

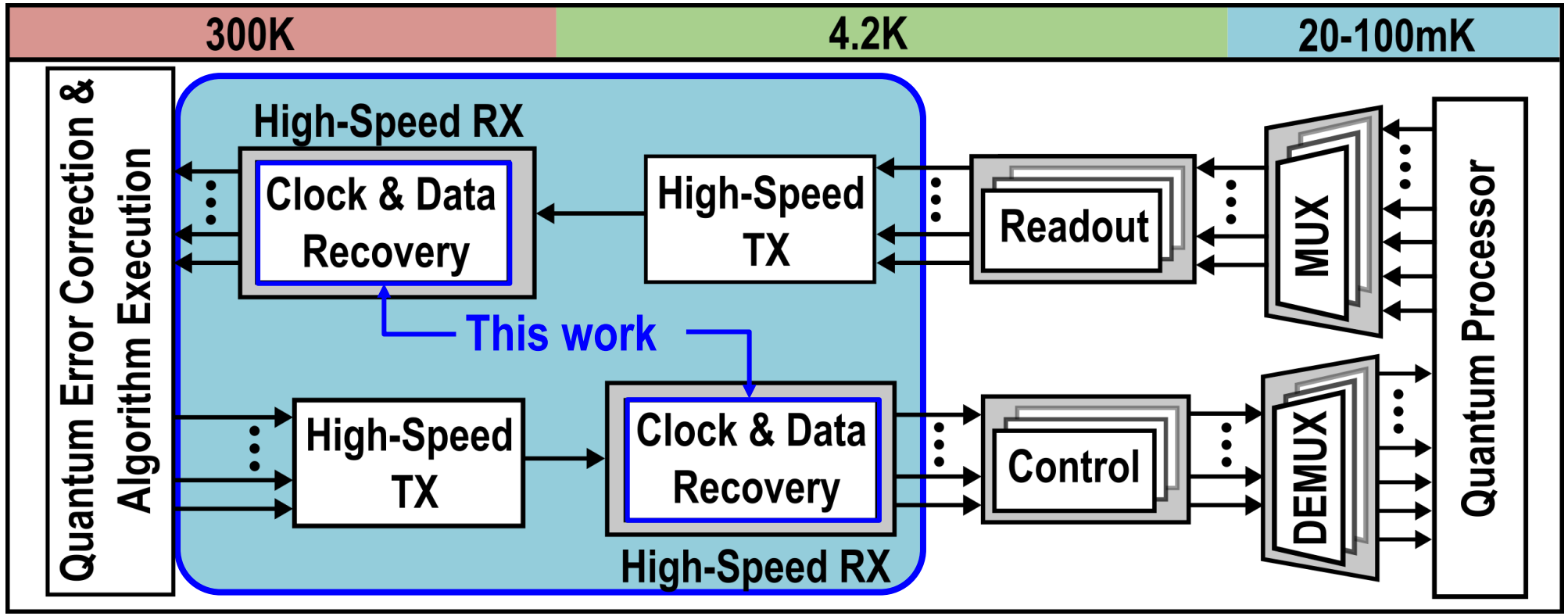




[Photo: Google's 72-bit quantum processor]

Need for Cryogenic High-Speed Link

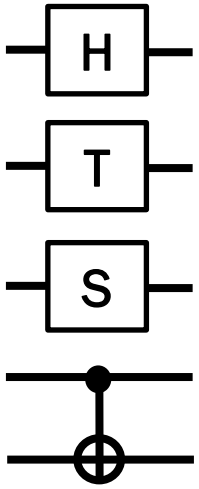
- A high-speed wireline link is required to communicate real-time data between control/readout blocks at 4.2K and classical digital processor at 300K

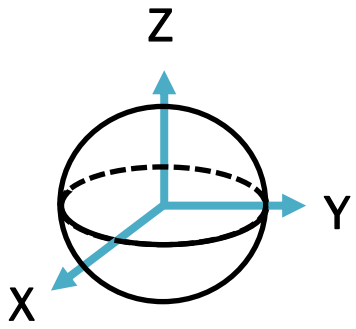


Data Rate Requirement

8 instructions/qubit

- Gates & auxiliary rotations



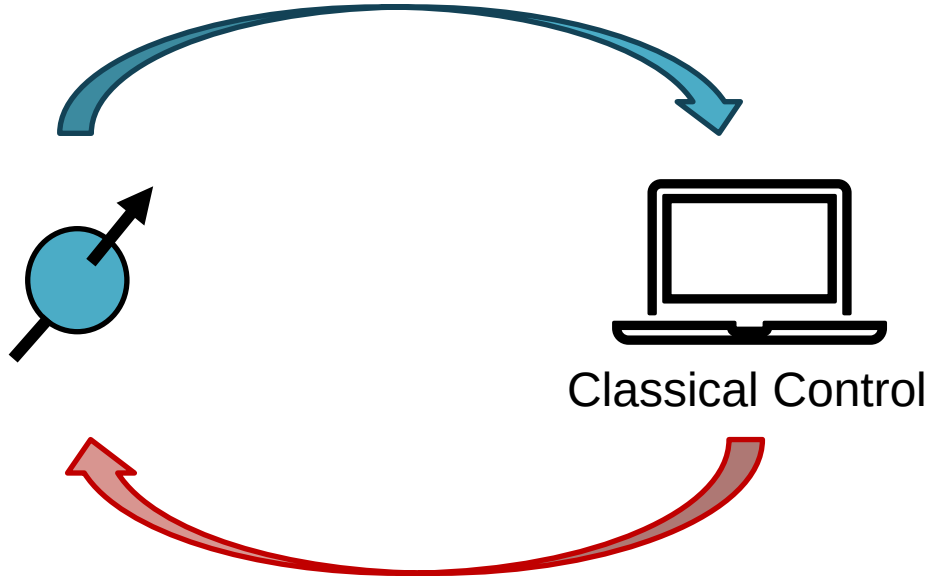


Gates	H, T, S, CNOT
Rotations	2*X, 2*Y

✖

1µs/qubit

- Envisioned surface code cycle time of spin qubit



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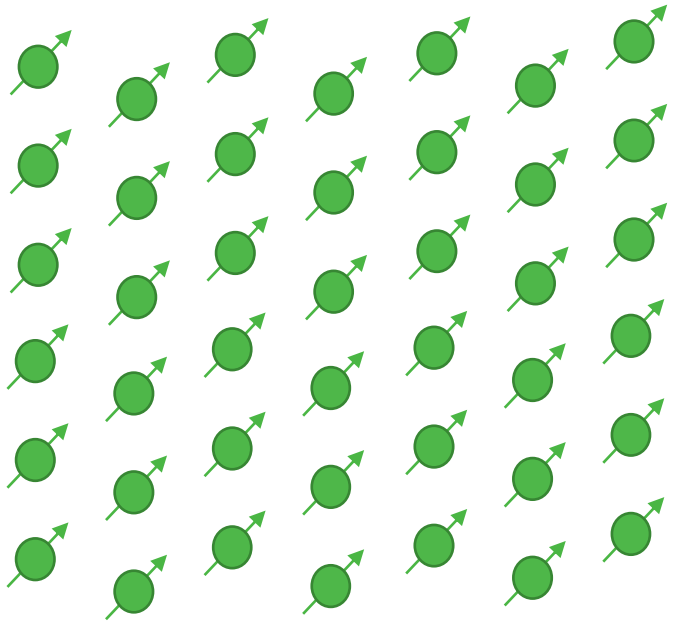
1000 qubits

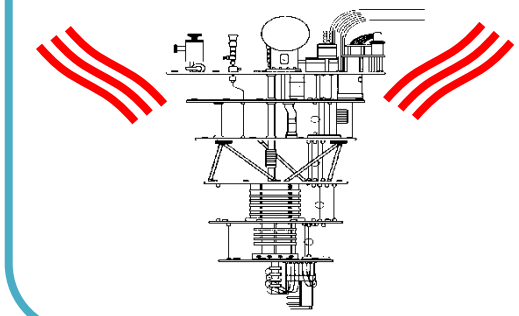
- Near-future quantum roadmap target



>3Gb/s wireline link required for real-time error correction of 1000 qubits

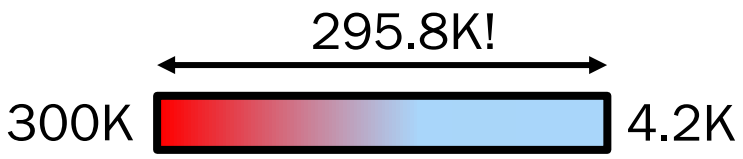
Challenges for Cryogenic CDR

Heat dissipation



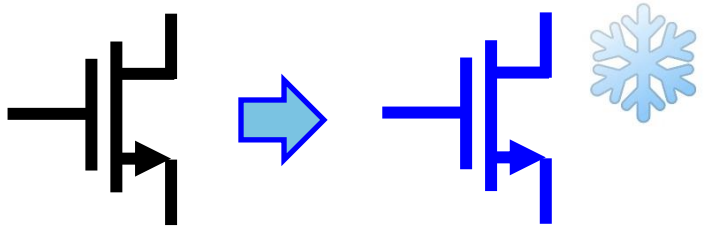
Power efficient structure

Extreme temperature range



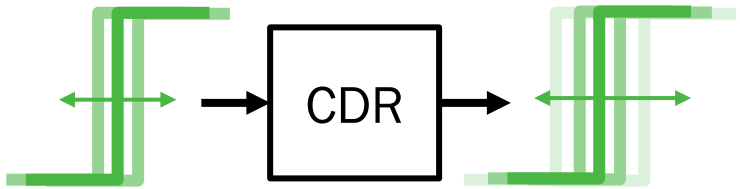
Reconfigurability & robustness

Device behavior at 4.2K



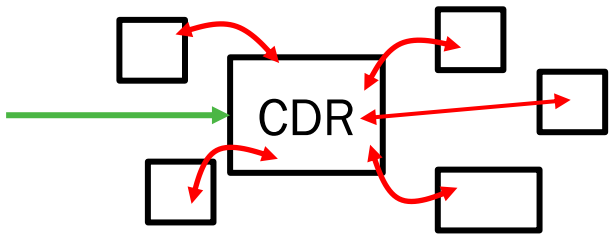
Cryogenic aware design

Jitter transfer



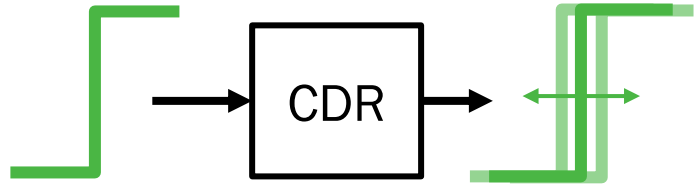
Minimize transferred jitter

SoC integration



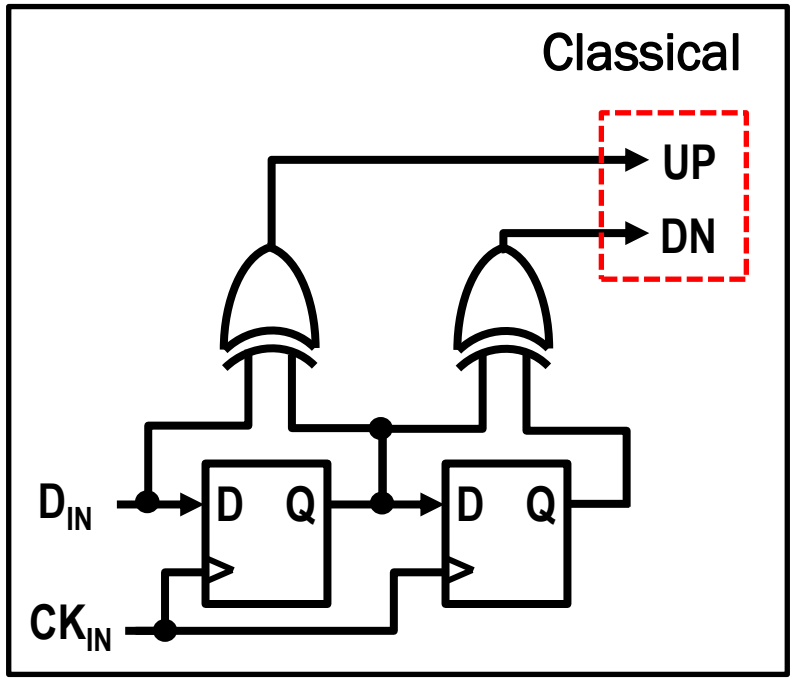
High jitter tolerance

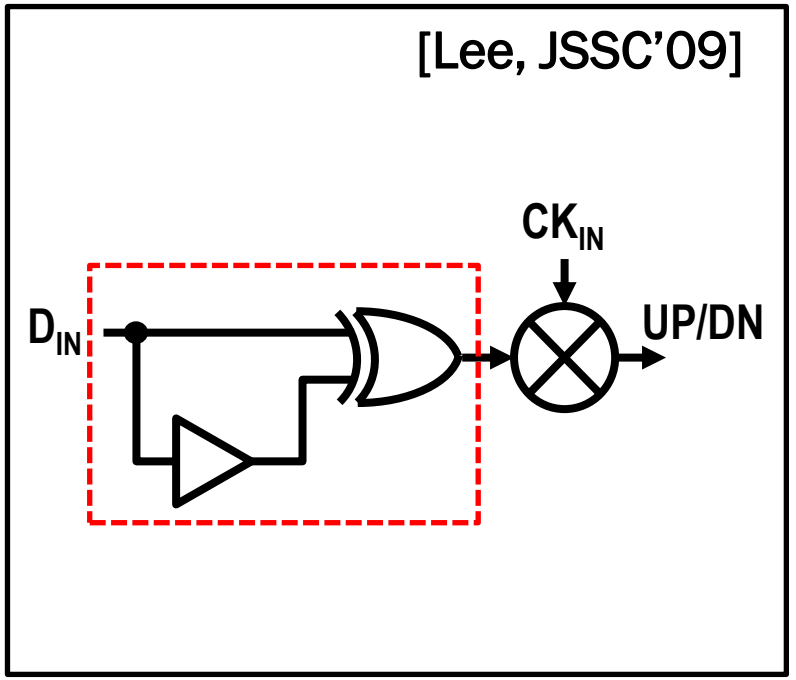
Intrinsic jitter generation

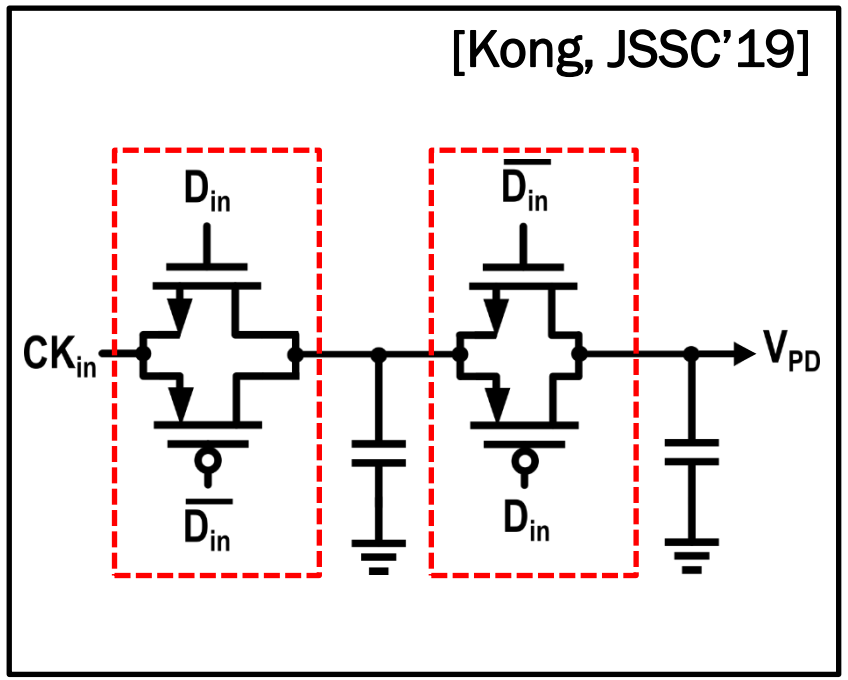


Low data dependency

Prior Art Limitations







Hogge PD

- Output pulses at the data rate
- High power consumption
- Complexity

Mixer-Based PD

- Data rate pulse generation
- High power consumption

Master-Slave Sampler

- Large locking point variation
- Degraded performance at 4.2K due to high on-resistance of transmission gates at mid-rail

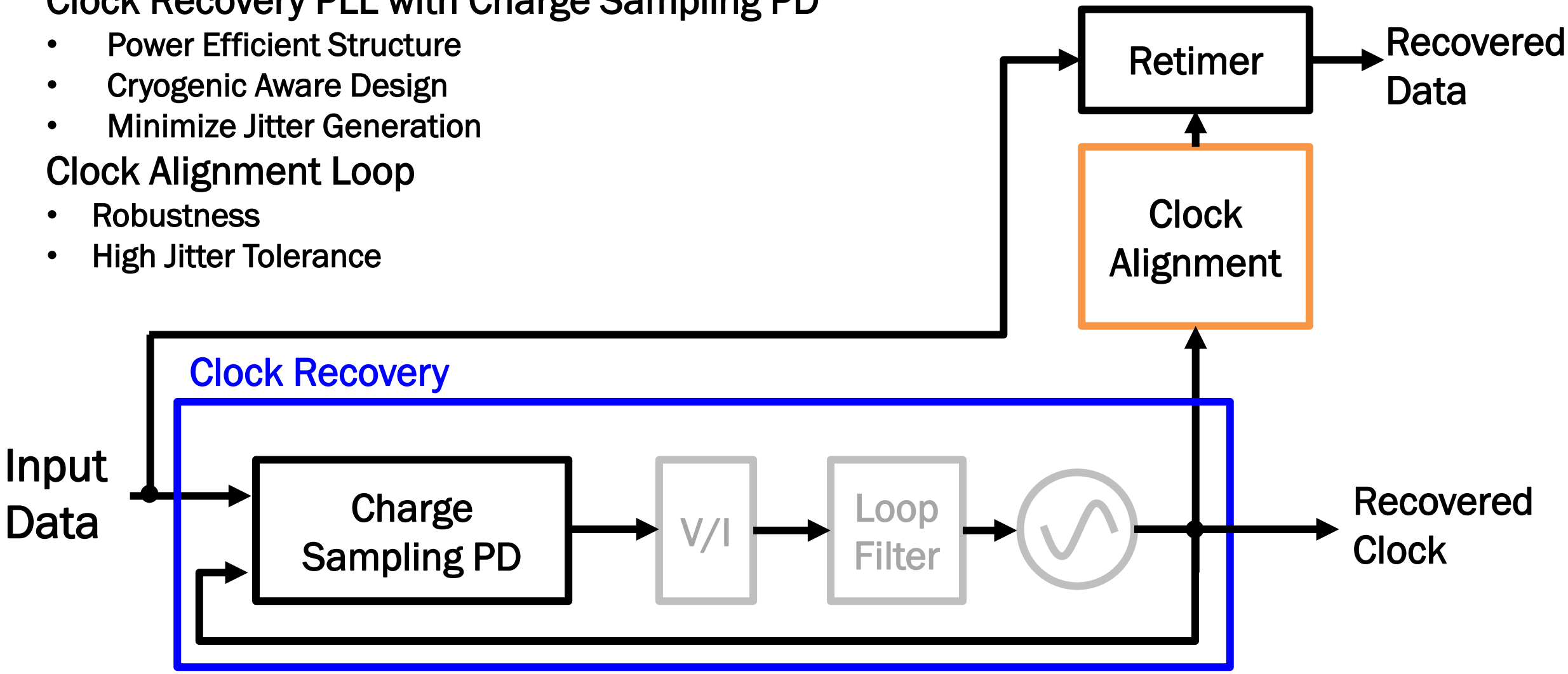
High-Level Overview of Proposed CDR

Clock Recovery PLL with Charge Sampling PD

- Power Efficient Structure
- Cryogenic Aware Design
- Minimize Jitter Generation

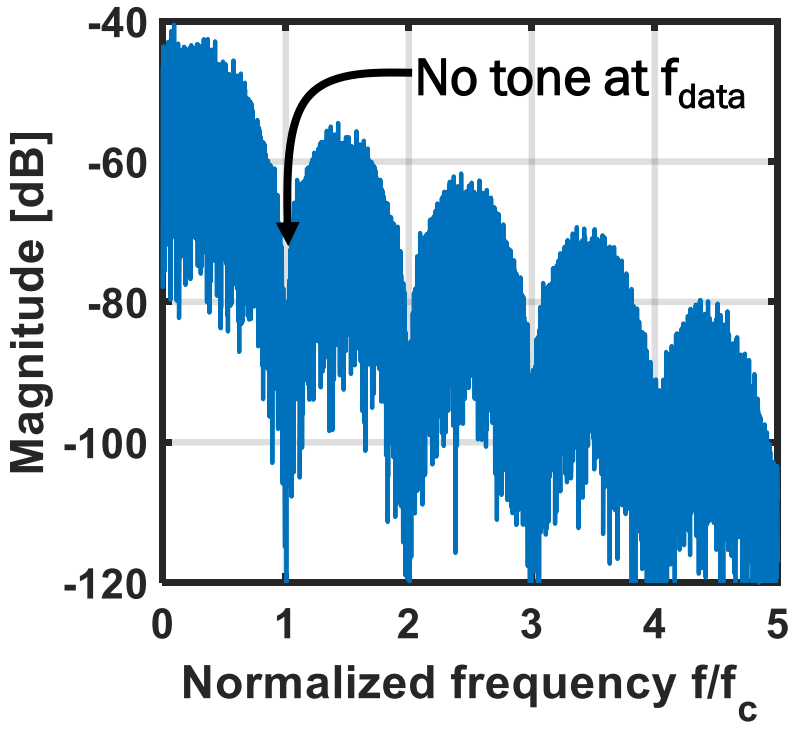
Clock Alignment Loop

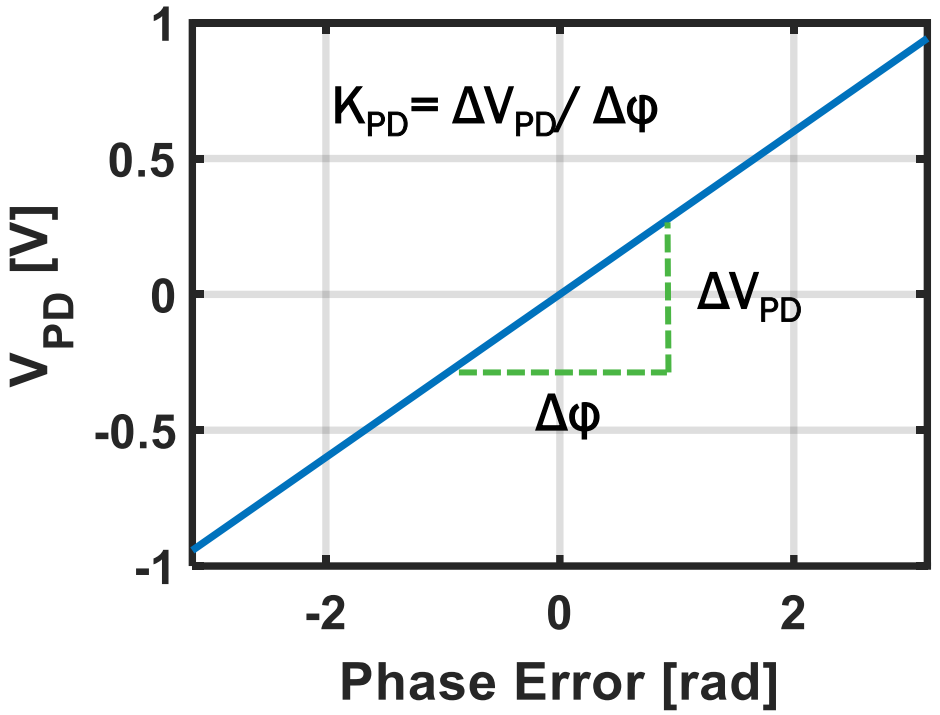
- Robustness
- High Jitter Tolerance



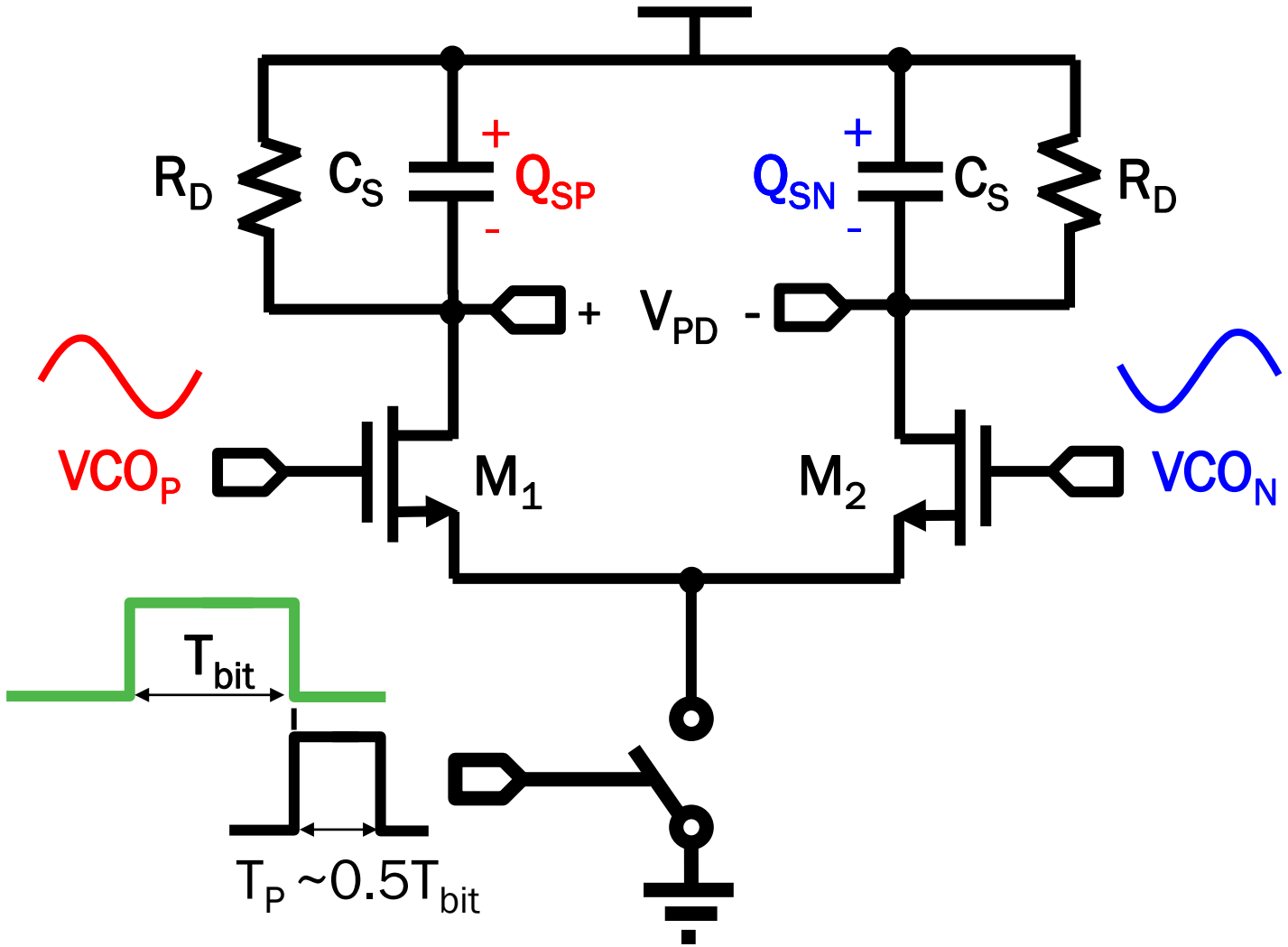
Phase Detection in CDR

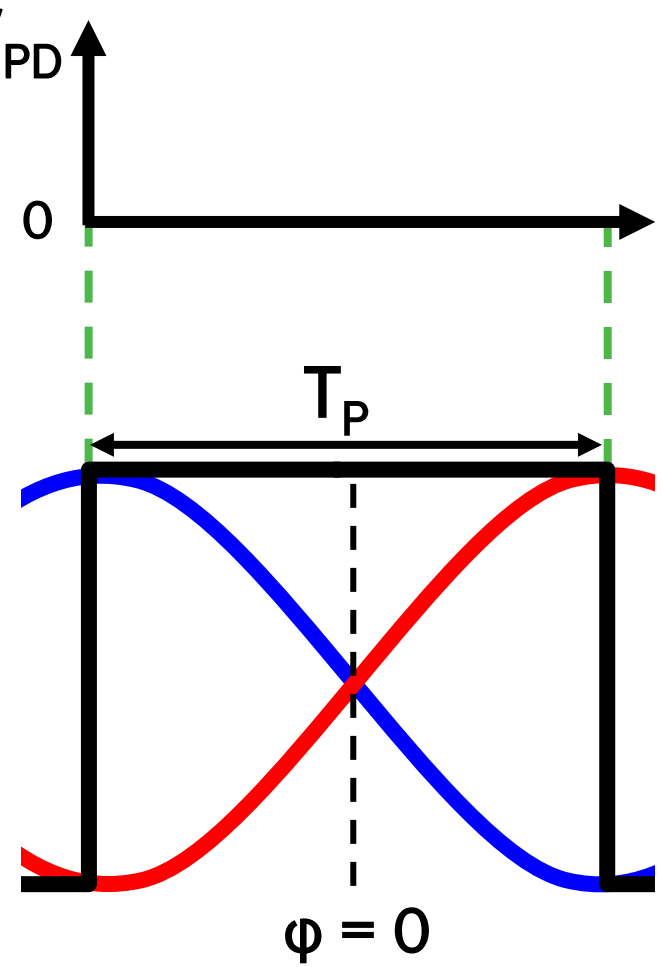
- CDR Phase Detector has two critical tasks
  1. Extract clock spectral component from data
  2. Generating error through phase comparison between data transition and VCO





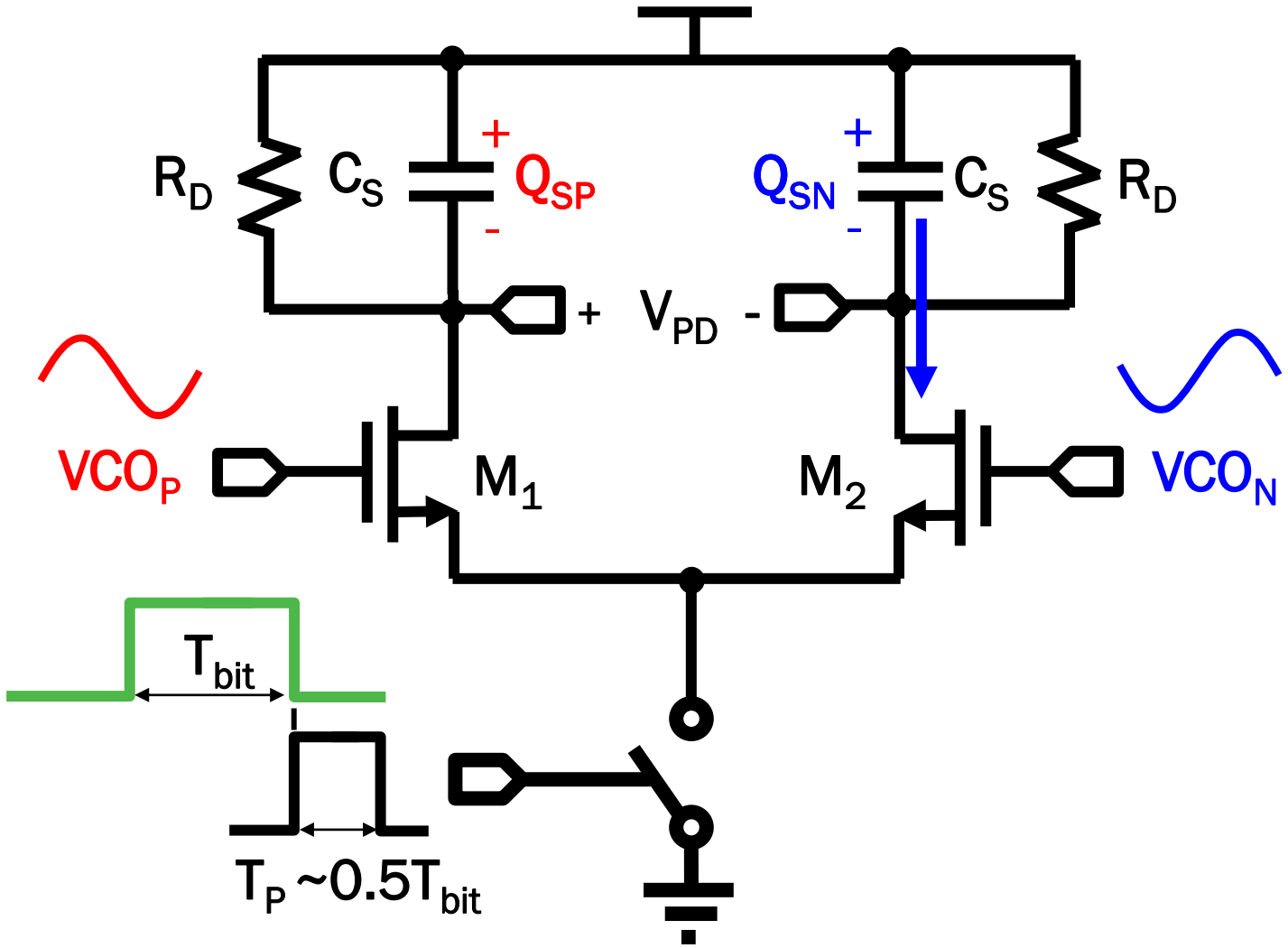
Charge Sampling Phase Detection Concept

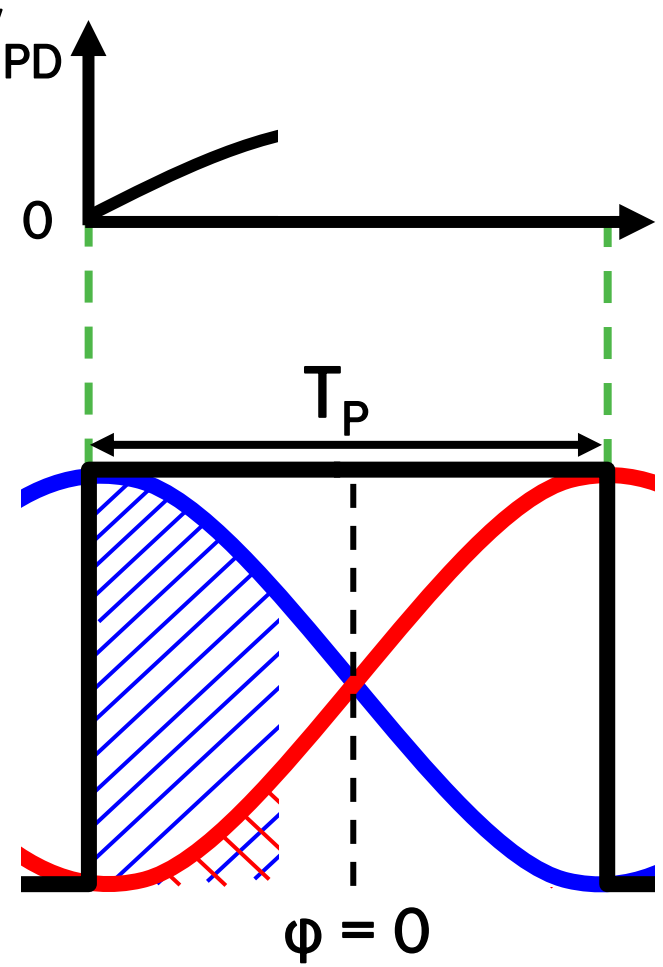




[Gong, JSSC'22]

Charge Sampling Phase Detection Concept





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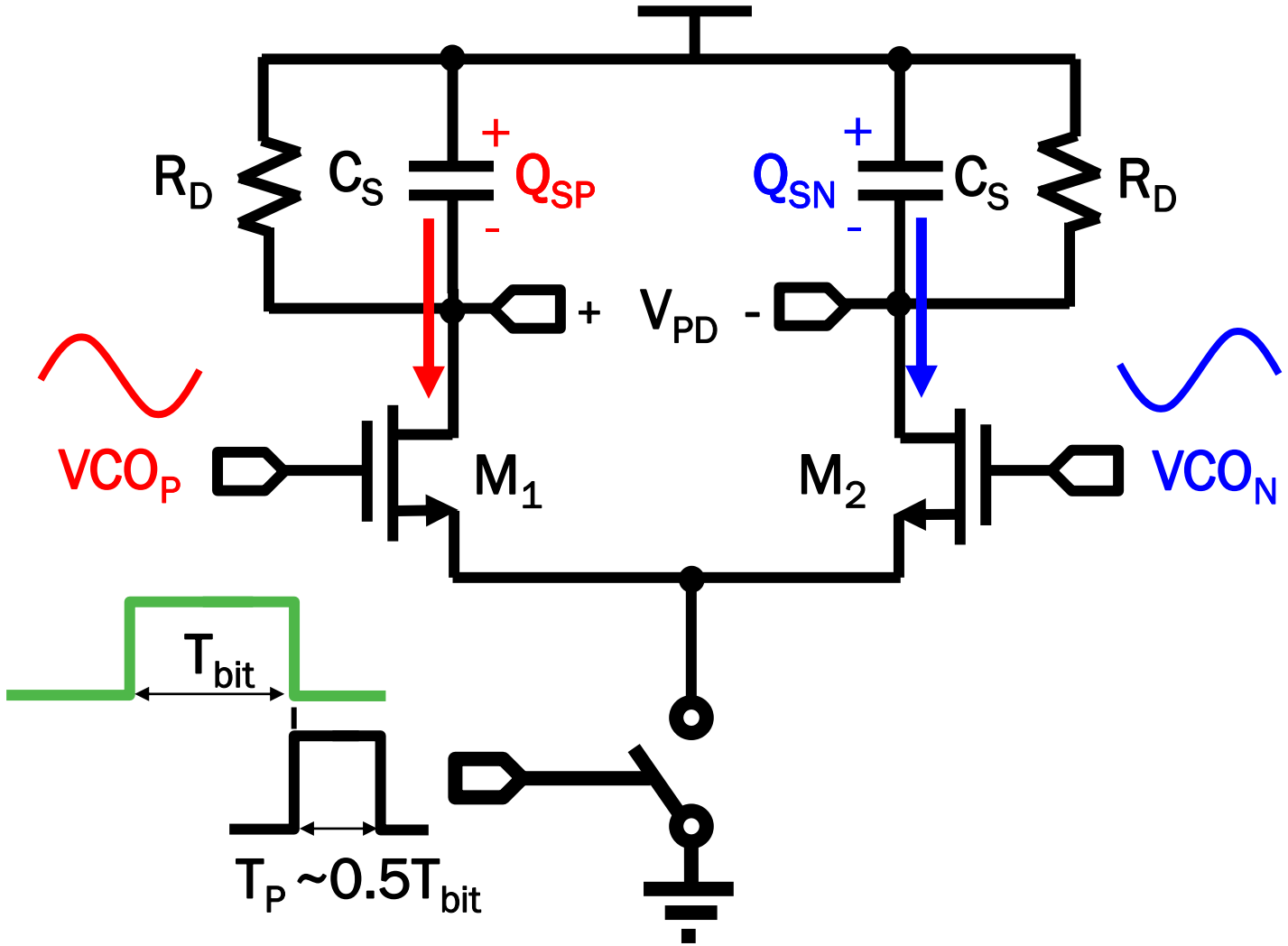

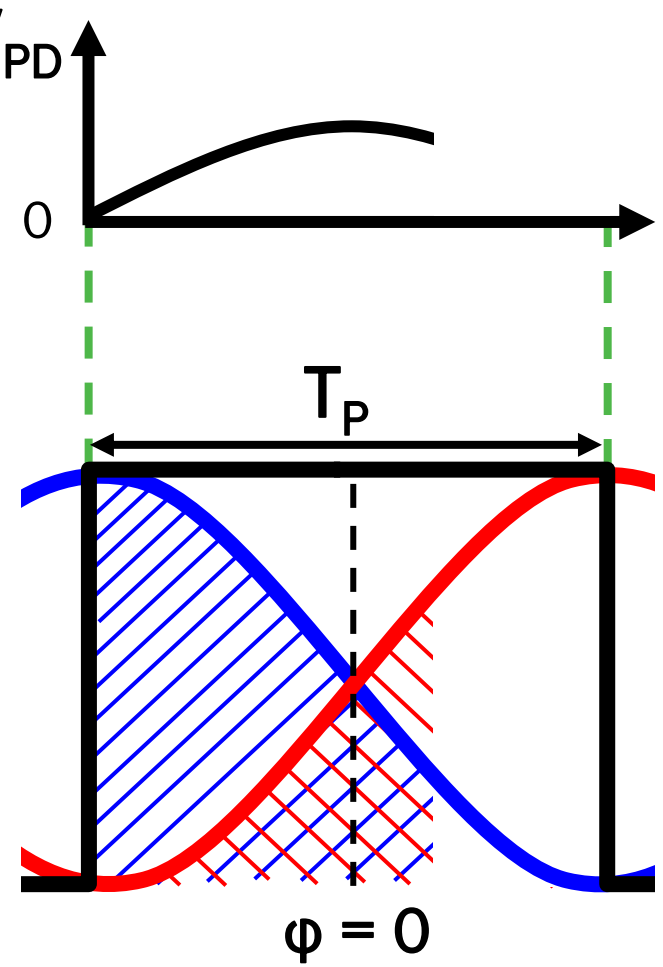

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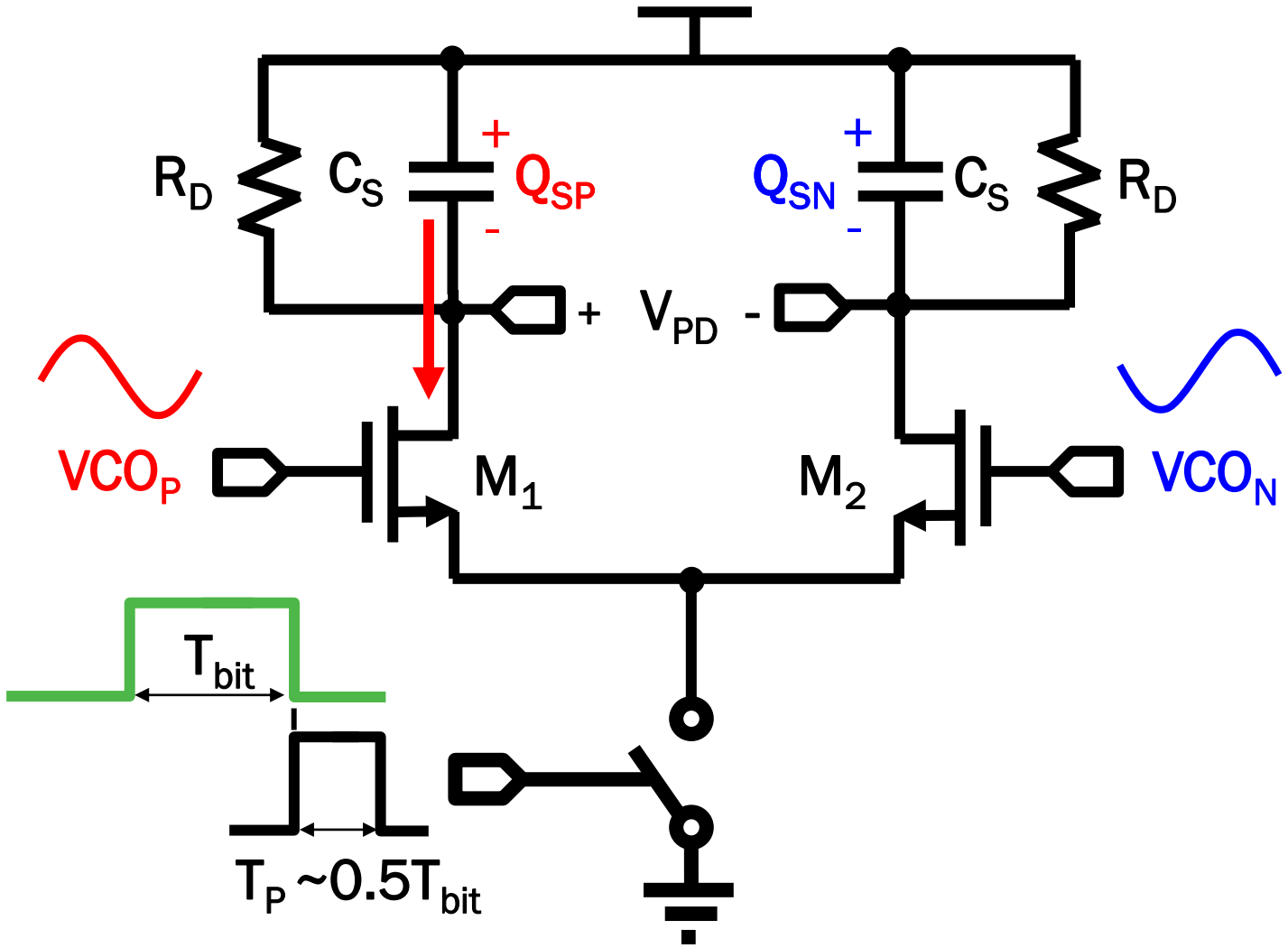

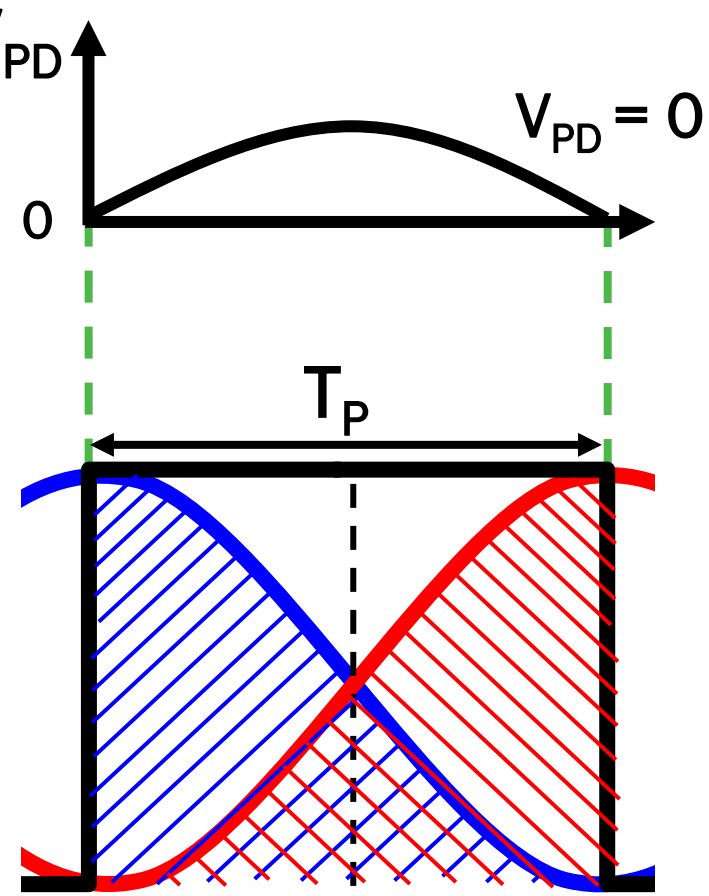

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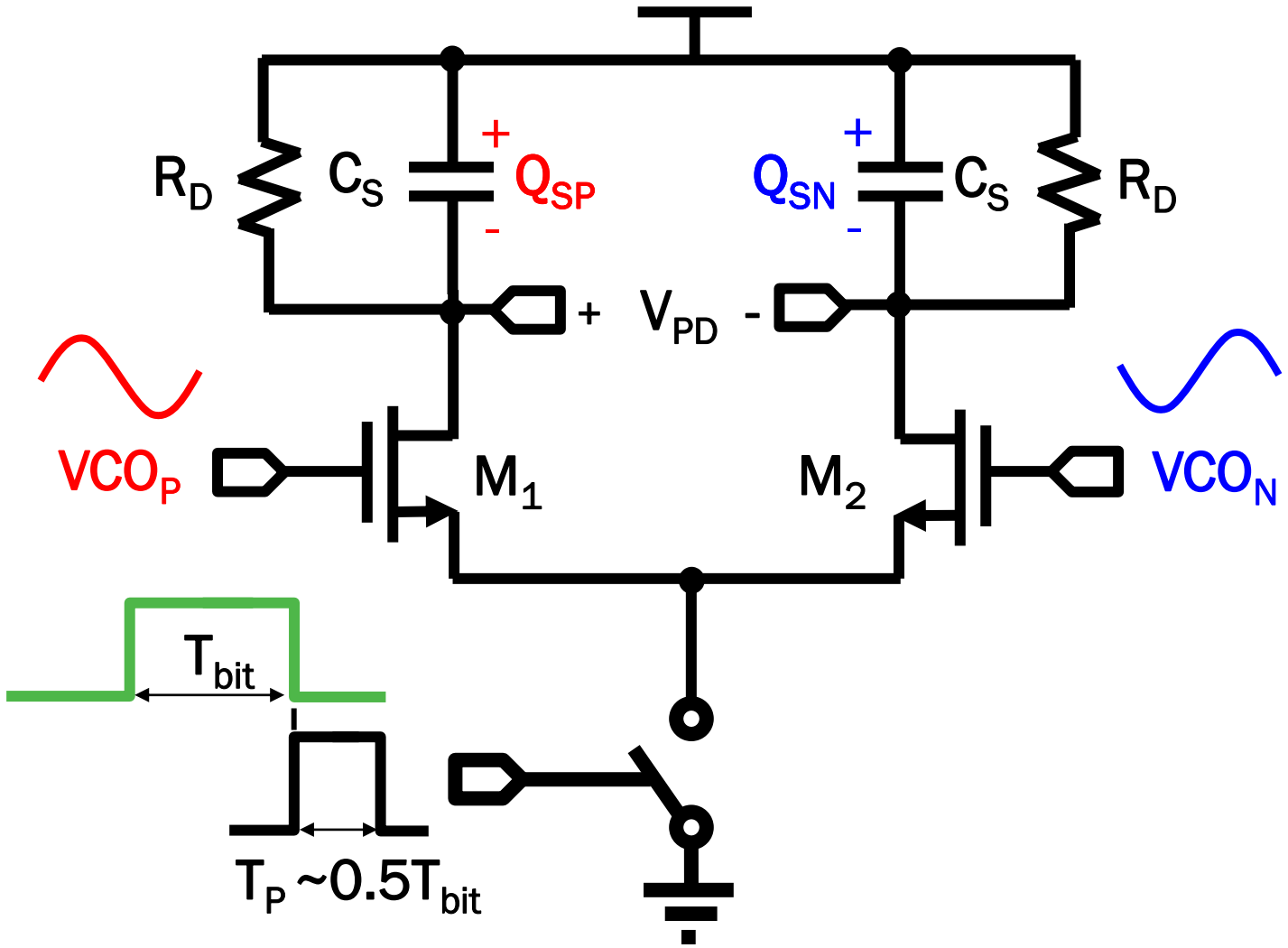
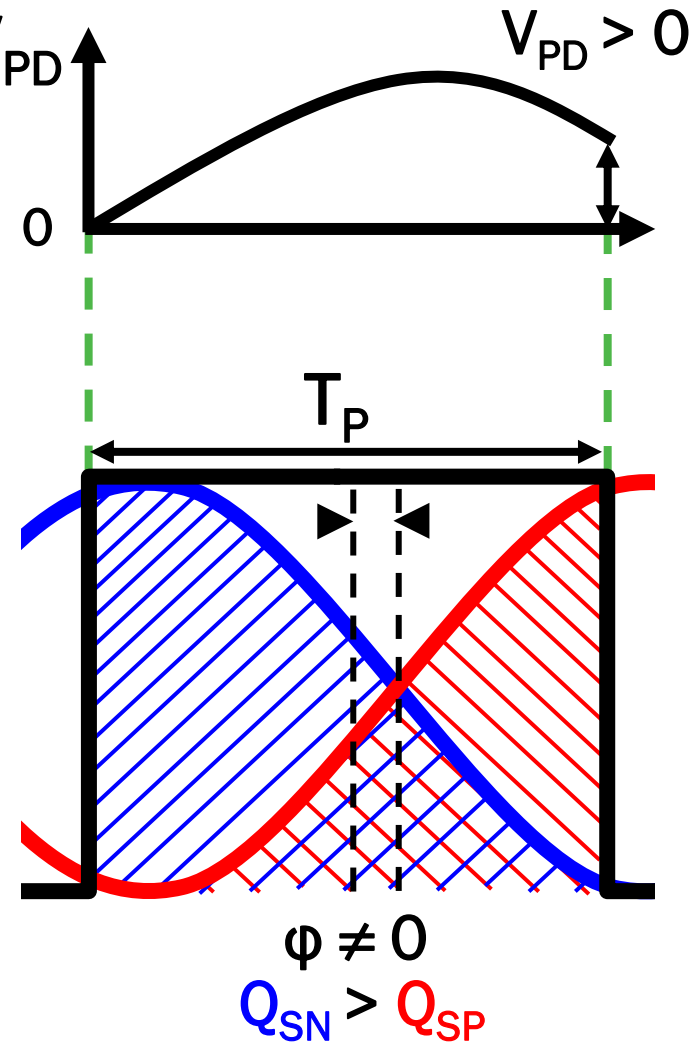
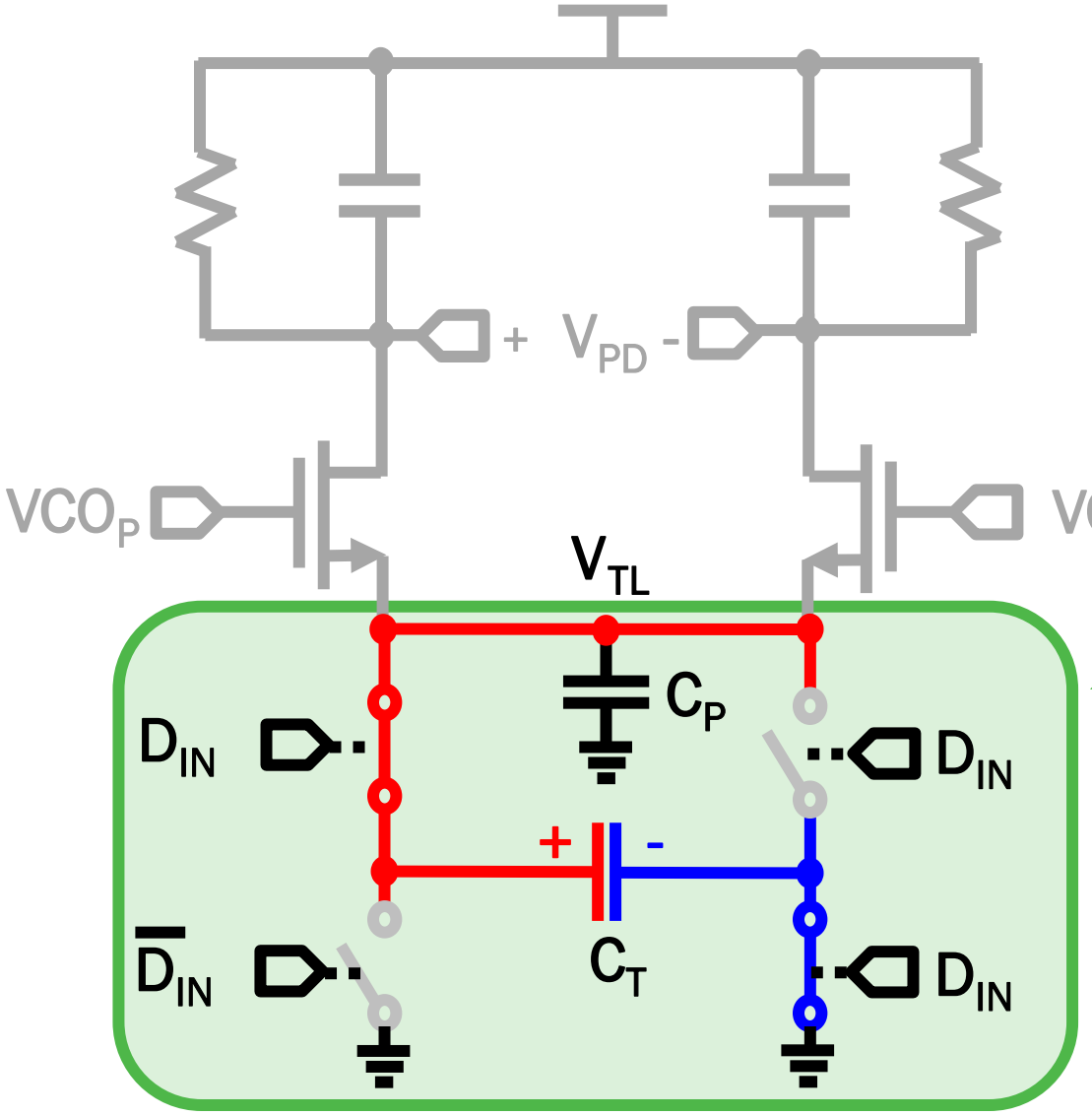
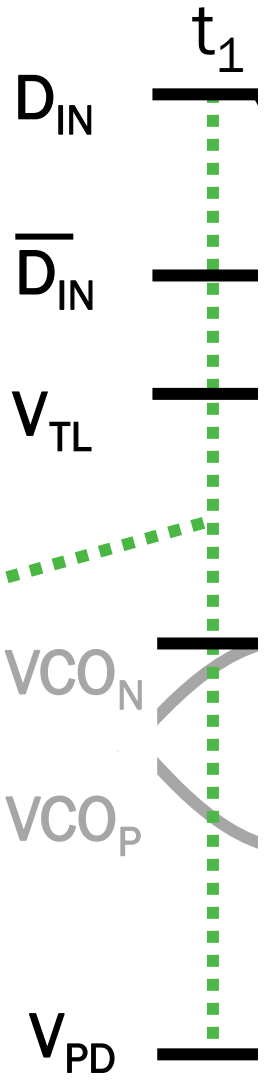




Pulse Generation in the Proposed PD





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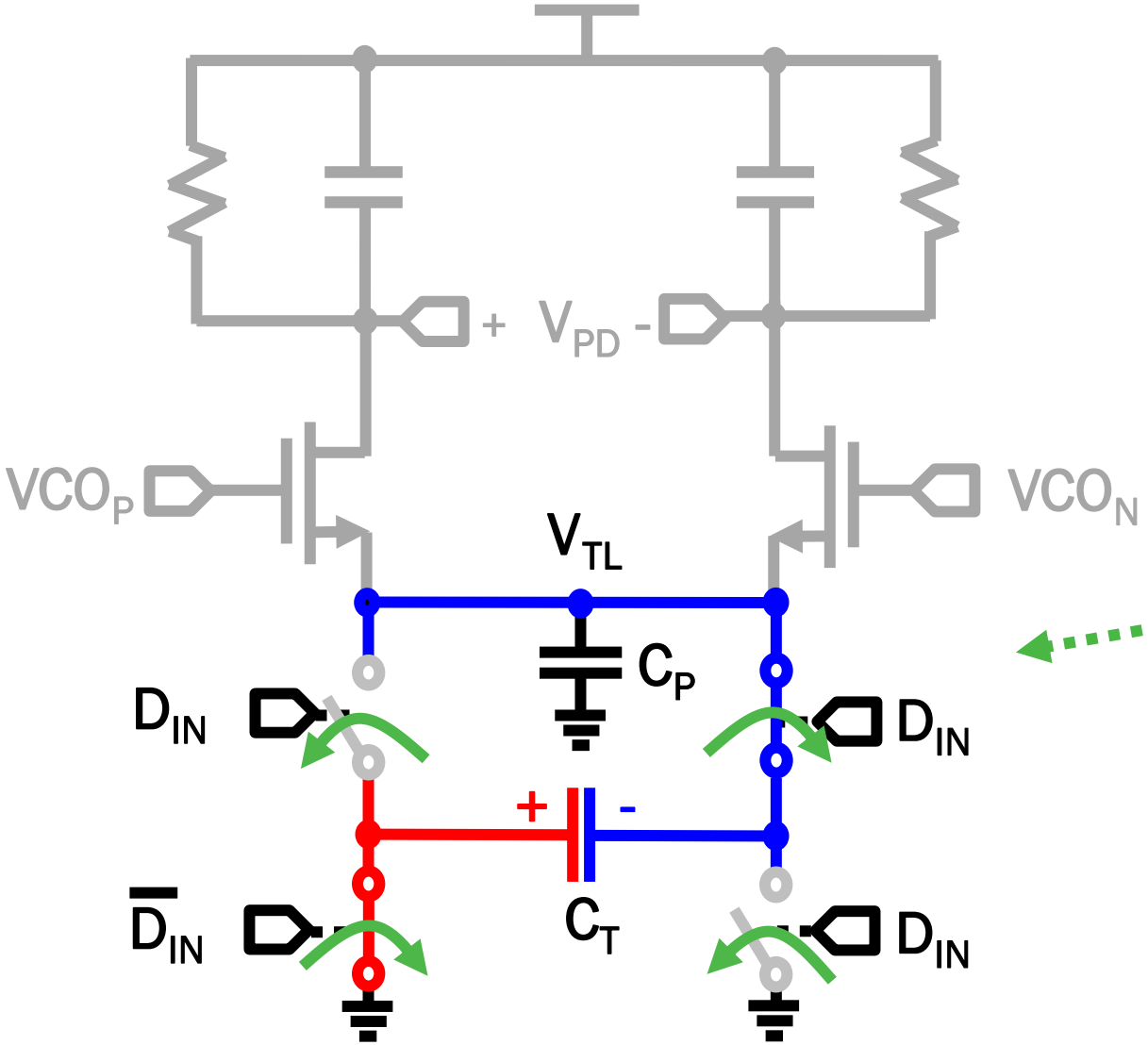
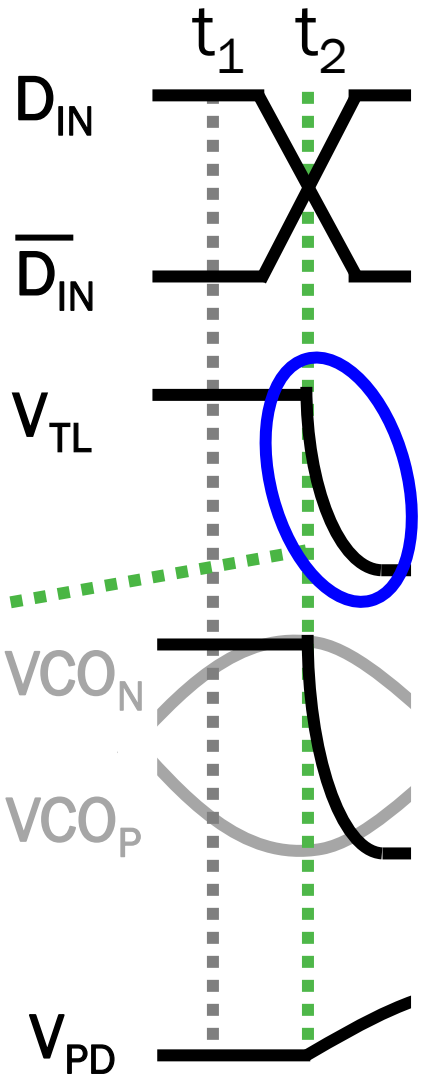
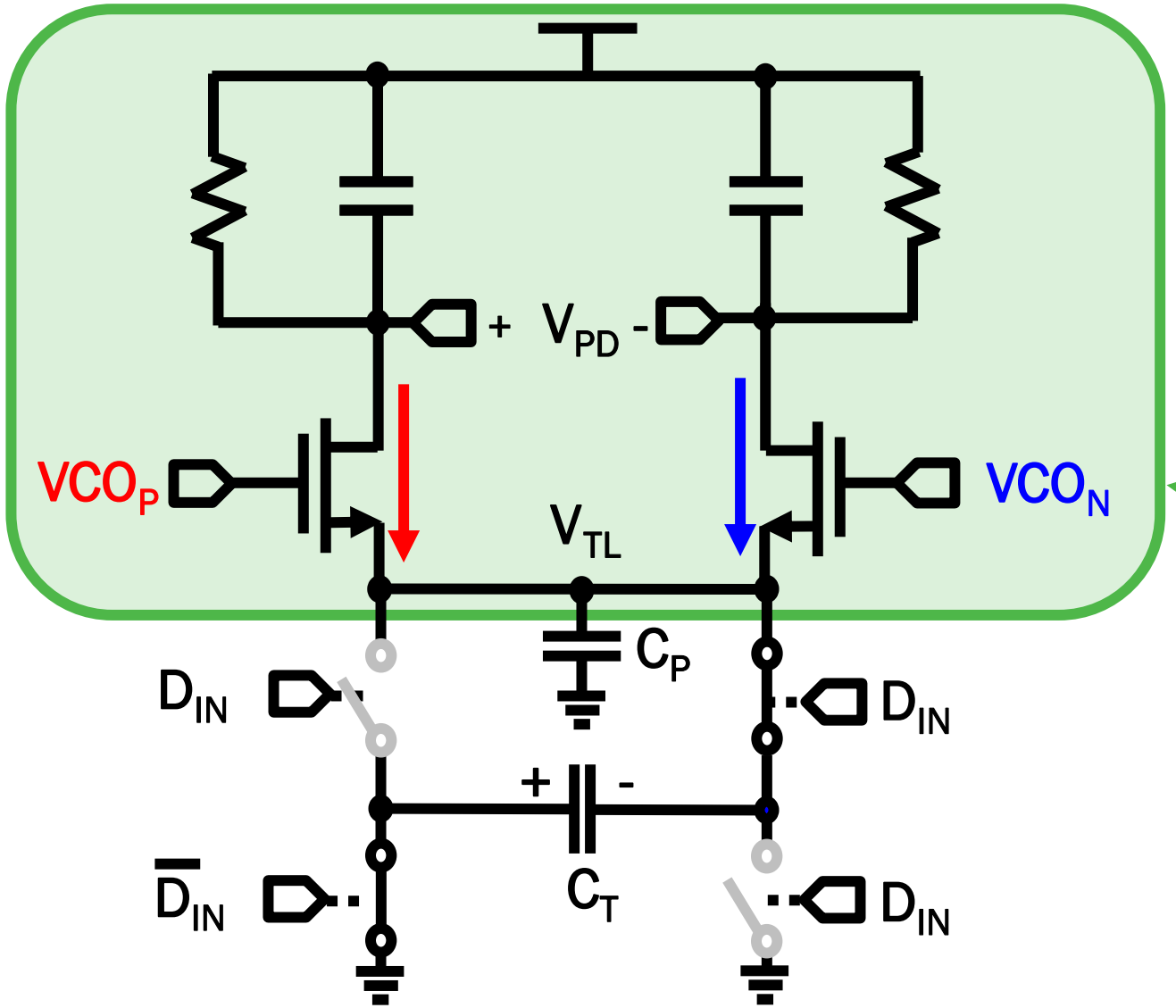
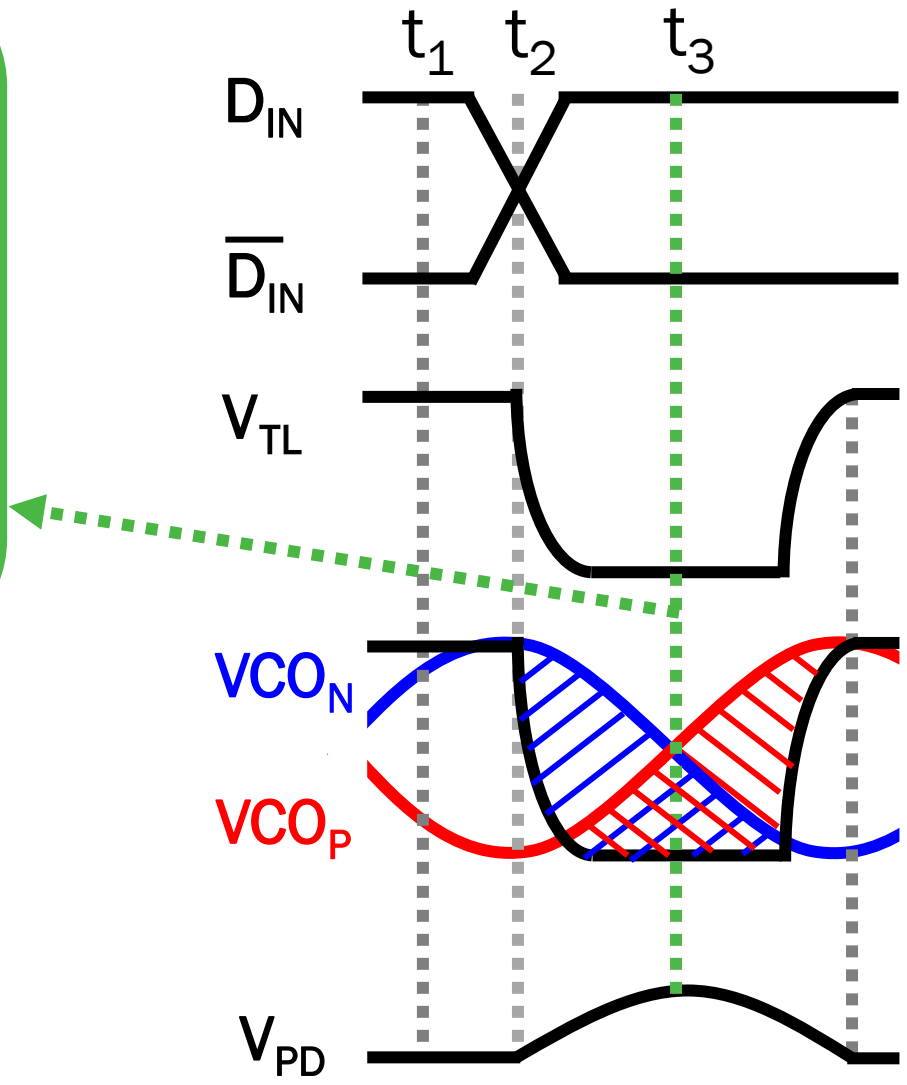


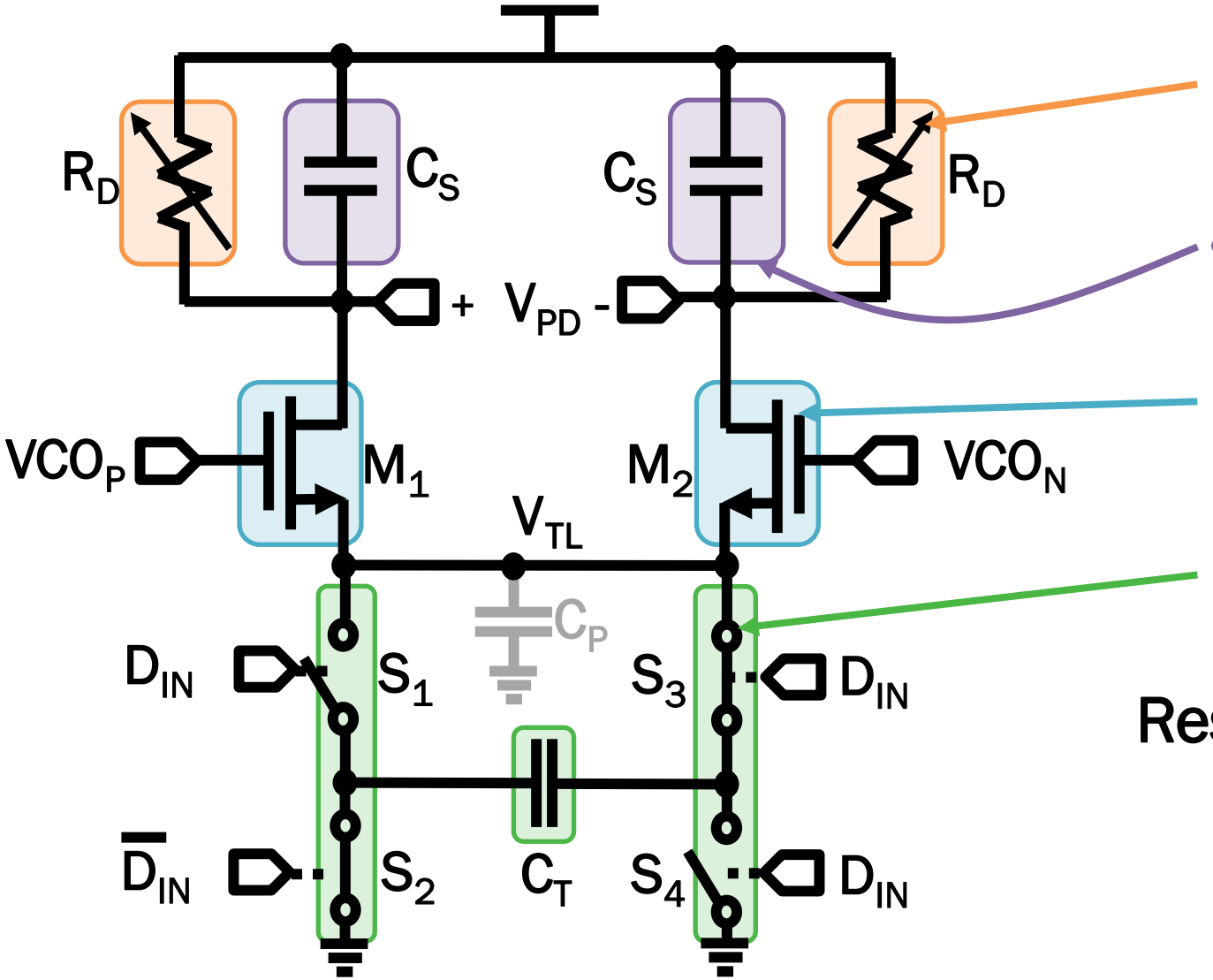


Pulse Generation in the Proposed PD





Design Considerations



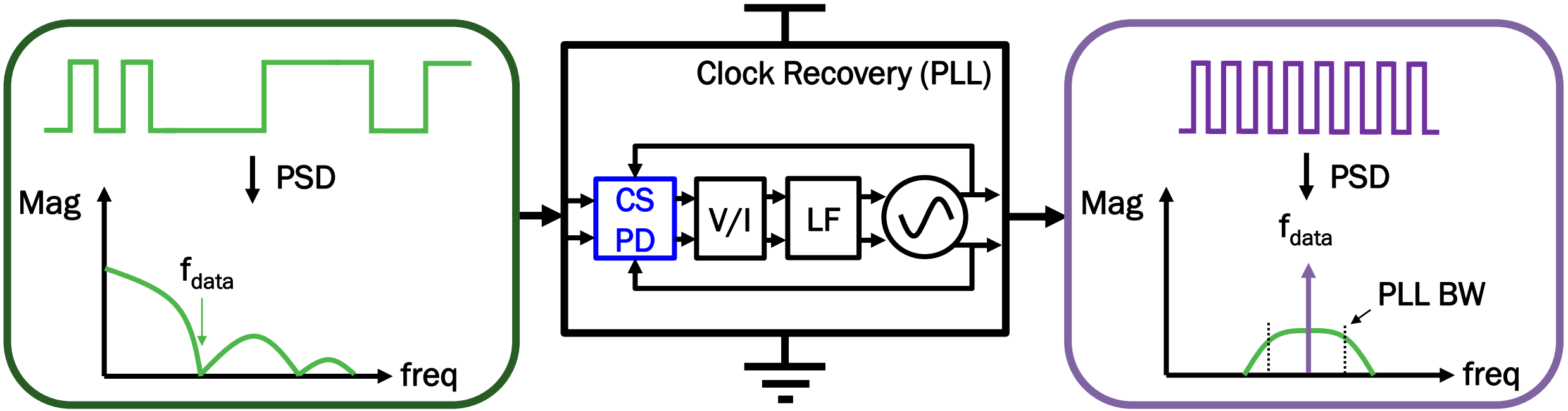
- Trimmable R_D tackles K_{PD} variation at 4.2K
- C_S trades off stability and output ripple
- Larger size reduces locking point variation
- Sets the sampling pulse to ~$0.5T_{bit}$

Result

- High K_{pd} of 0.3V/rad
- In-band PN <-150dBc/Hz
- 100uA power consumption at 10GHz

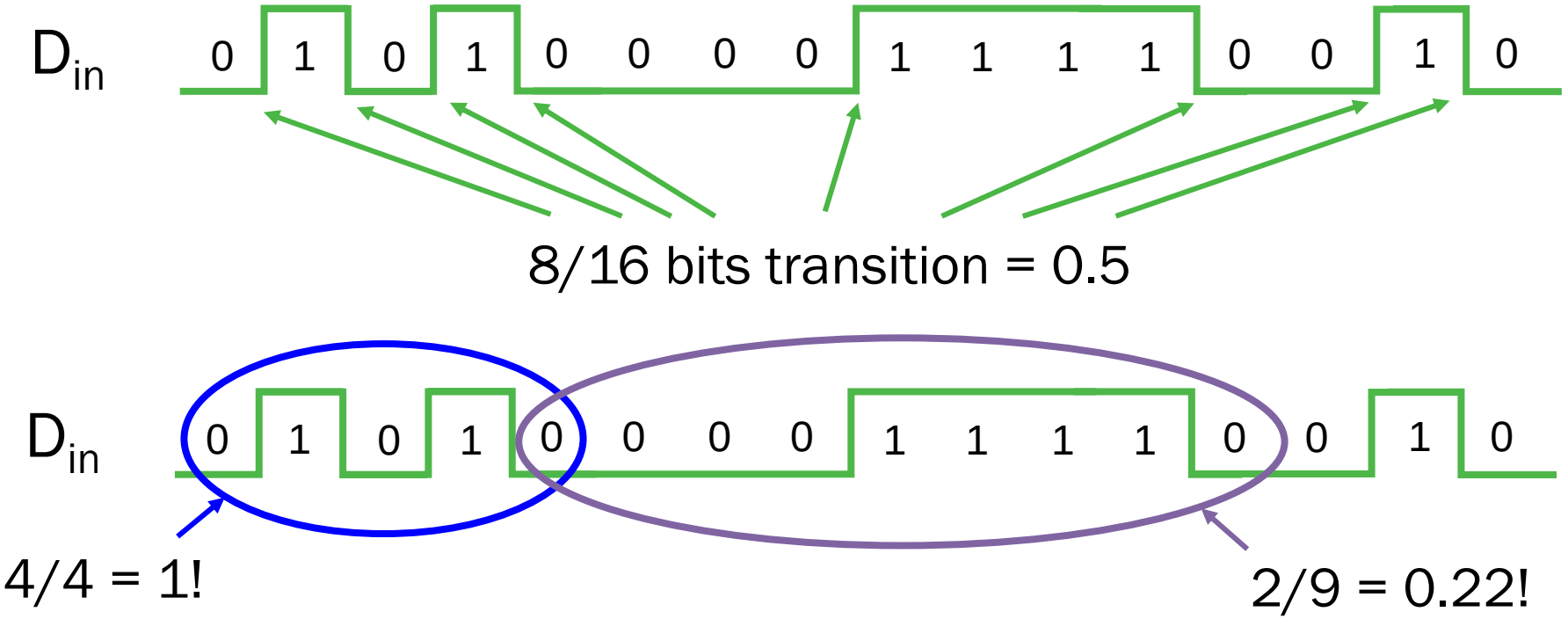
Impact of Data Transition Density on PD Operation

- Wide spectral content of random data modulates the phase of the recovered clock due to various mechanisms
  - Coupling through ground and supply
  - Data dependent memory effects

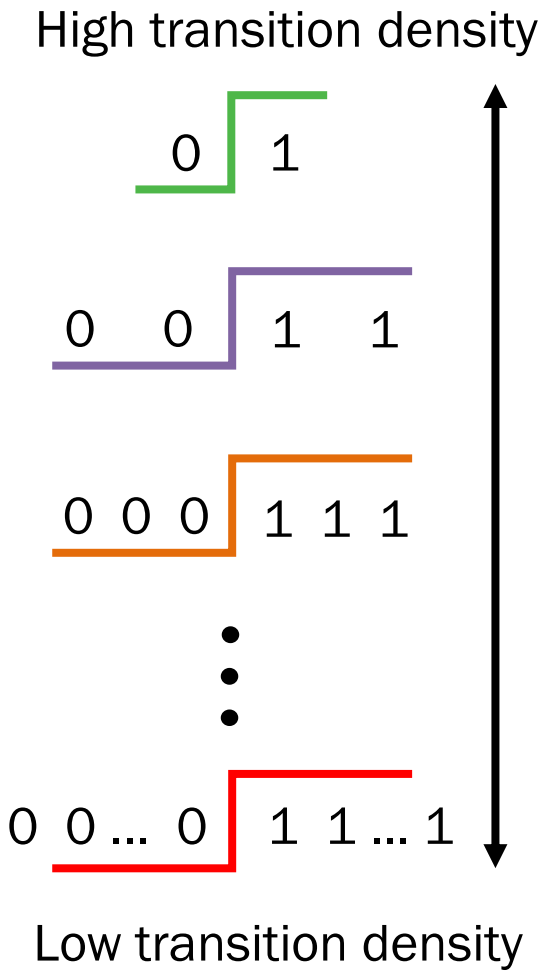


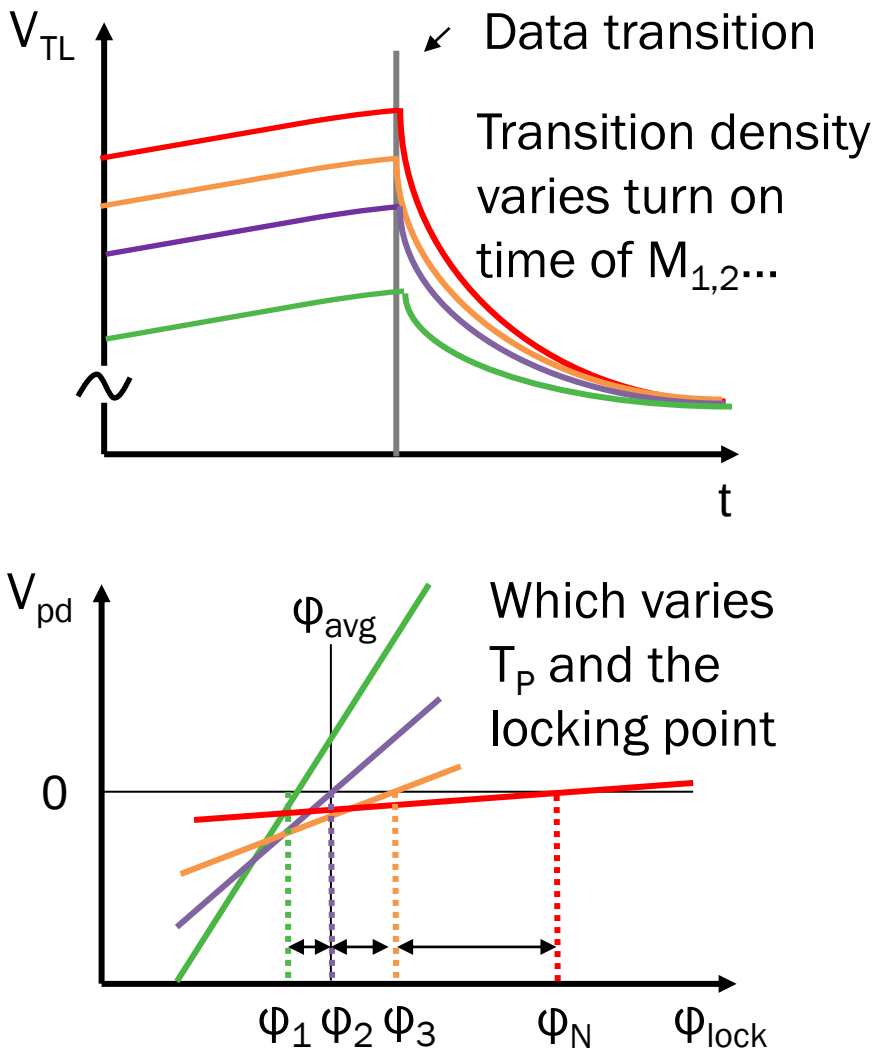
Variation of Transition Density

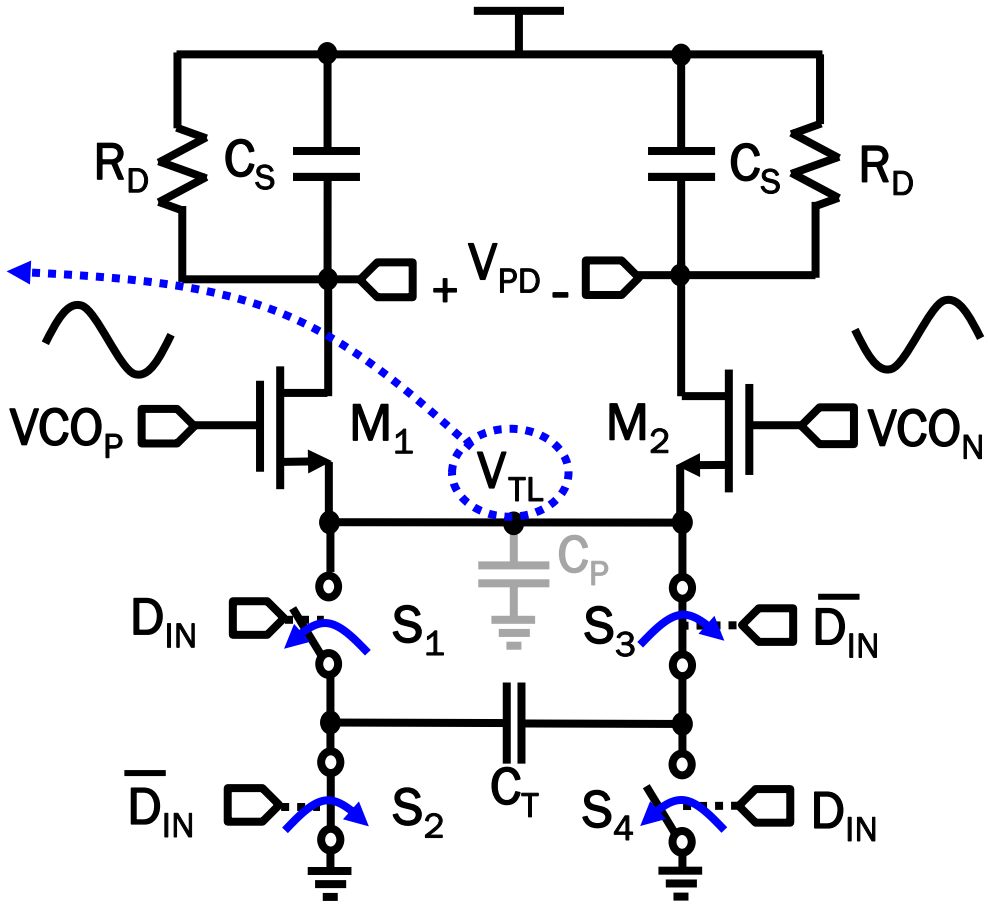
- Overall transition density of random data is ~0.5
- Locally the transition density varies over the bitstream



Data Dependent Sampling Pulse

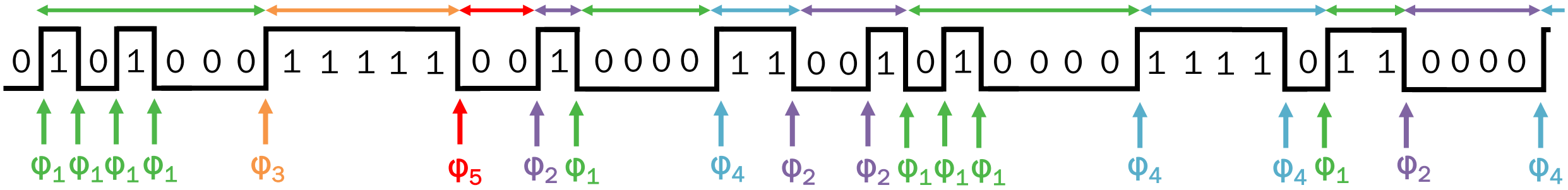






Analyzing the Data Dependent Sampling Pulse

- PLL locks to the weighted average of the entire sequence
- Variation of locking point over different transition densities increases in-band phase noise

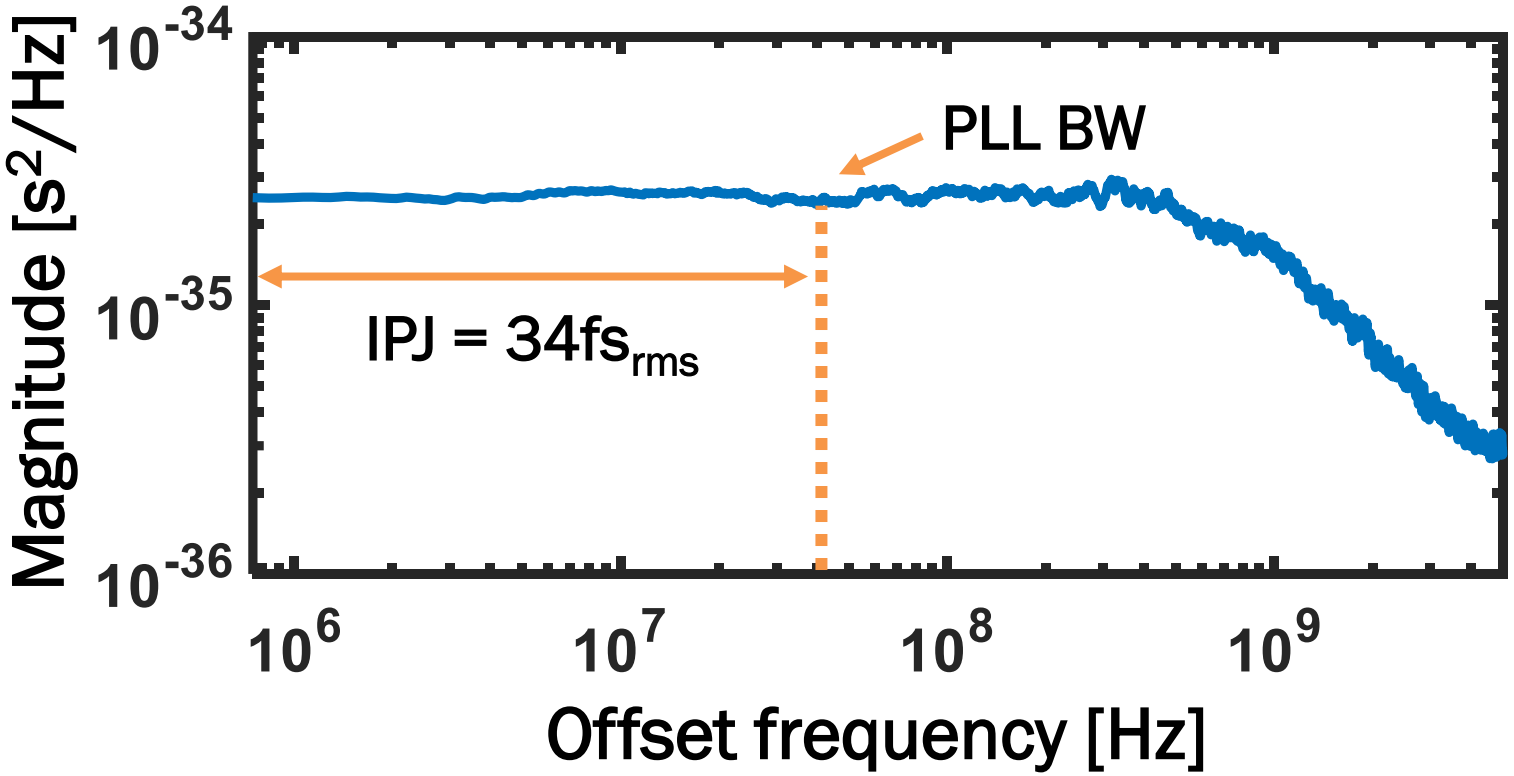


$$\Phi_{lock,avg} = mean([Bitstream] * [\Phi_{lock\_weights}])$$

$$\Phi_{lock,err} = [Bitstream] * [\Phi_{lock\_weights}] - \Phi_{lock,avg}$$

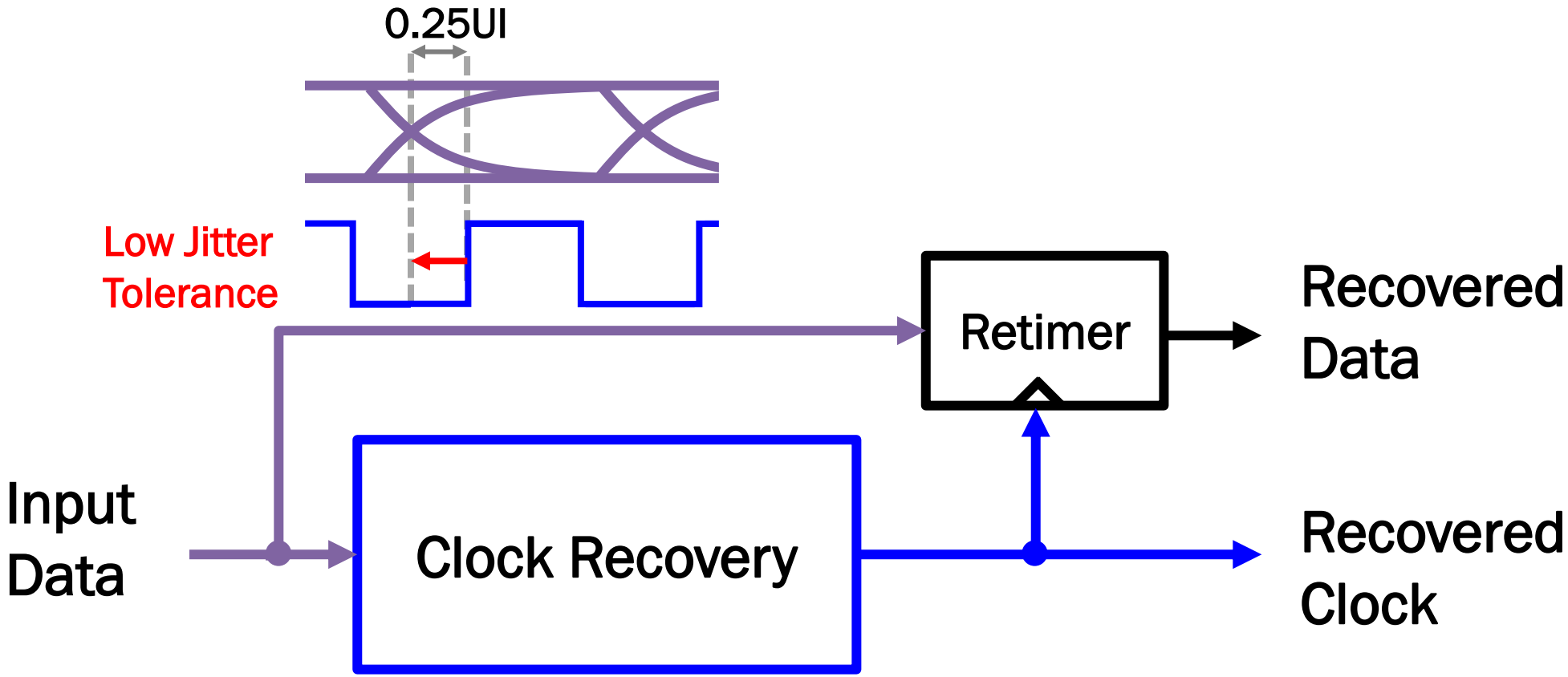
Data Dependent Sampling Pulse Spectrum

- RMS jitter due to locking point variation is only $34fs_{rms}$
- Jitter contribution is sufficiently low for required data rate



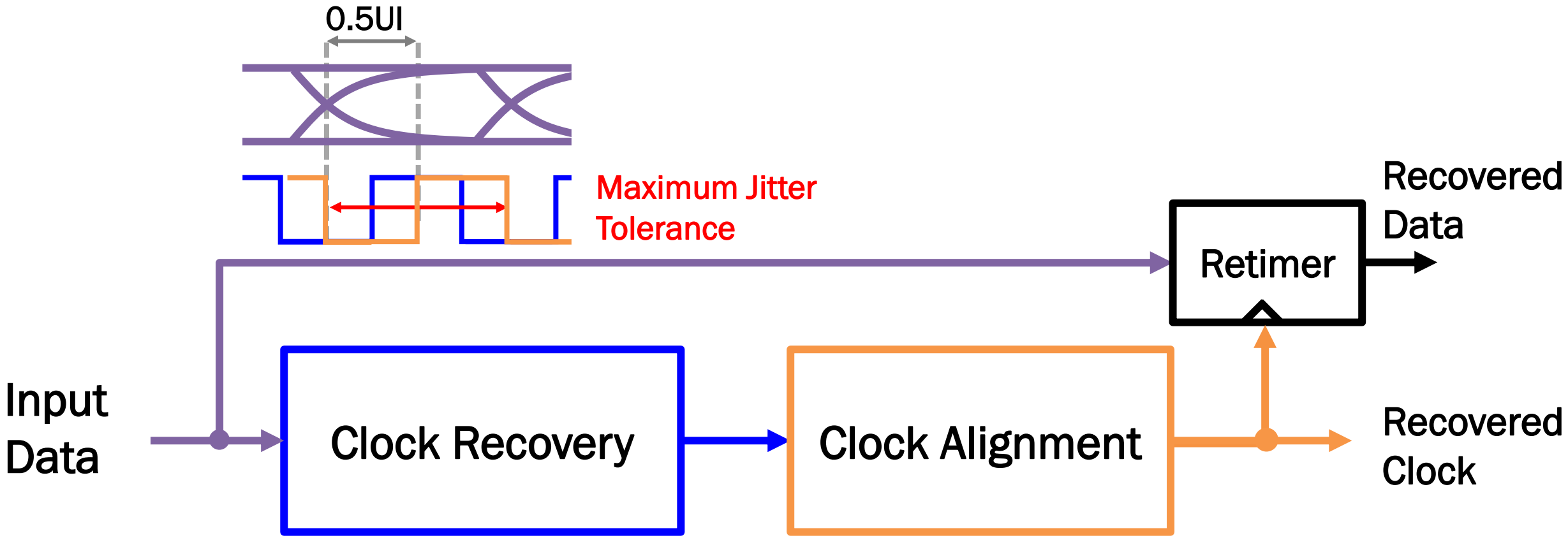
Retiming in the Proposed CDR

- Recovery loop does not lock to the center of incoming data



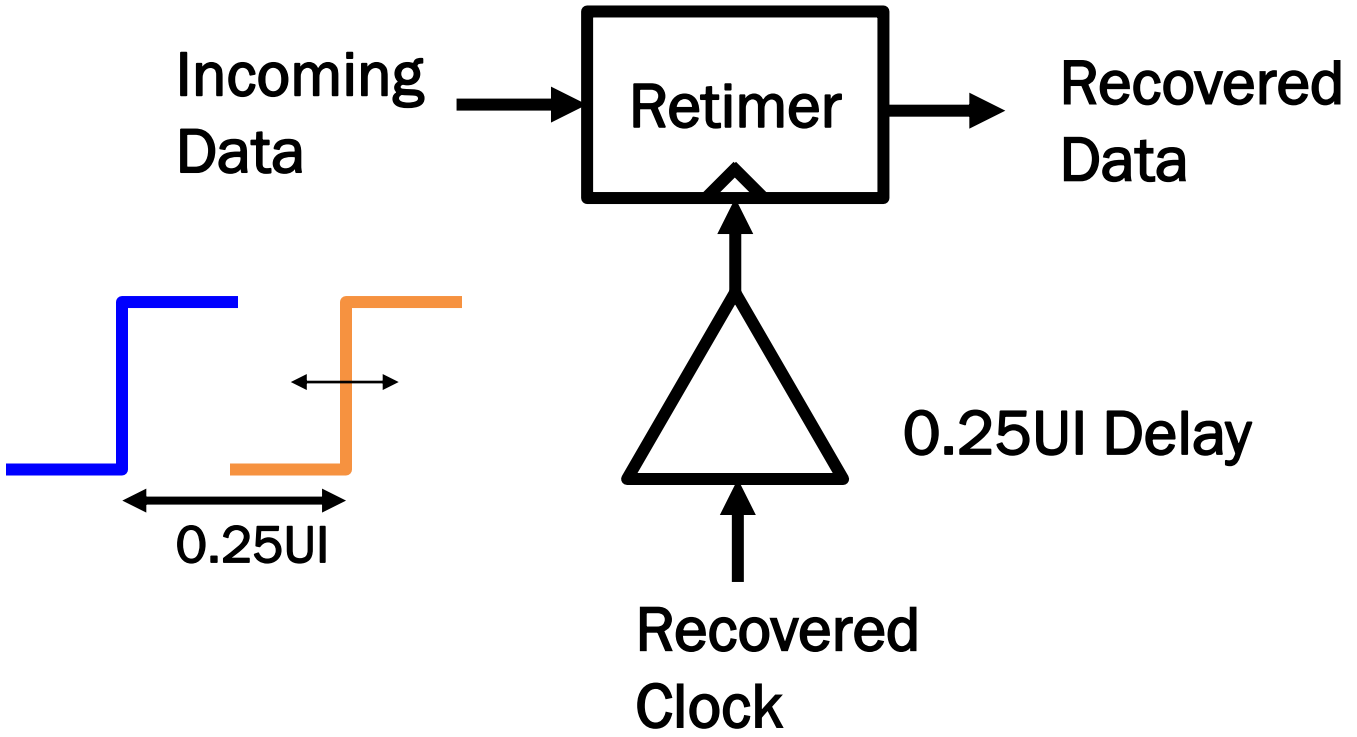
Retiming in the Proposed CDR

- Recovered clock must be centered for optimal retiming



Aligning the Recovered Clock

- Delay the recovered clock by 0.25UI using a buffer
- Large delay variation over PVT reduces Jitter Tolerance



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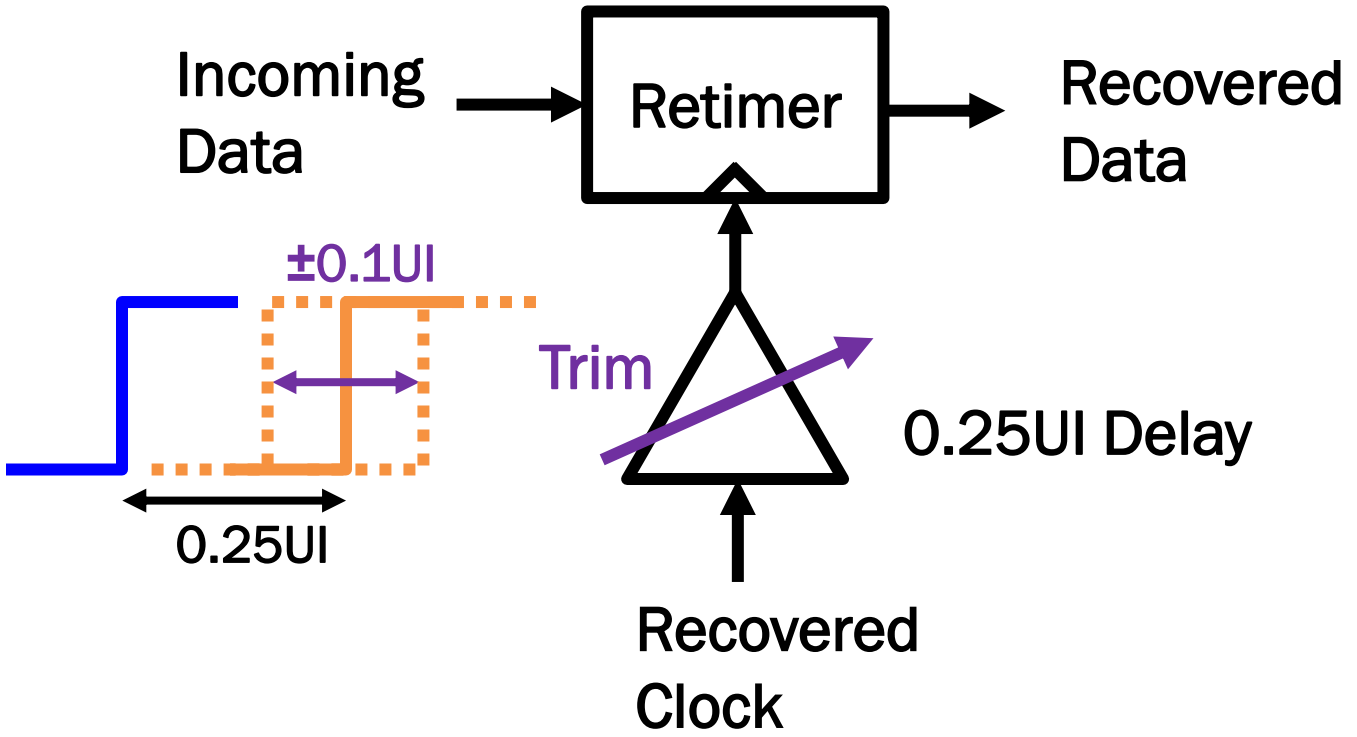

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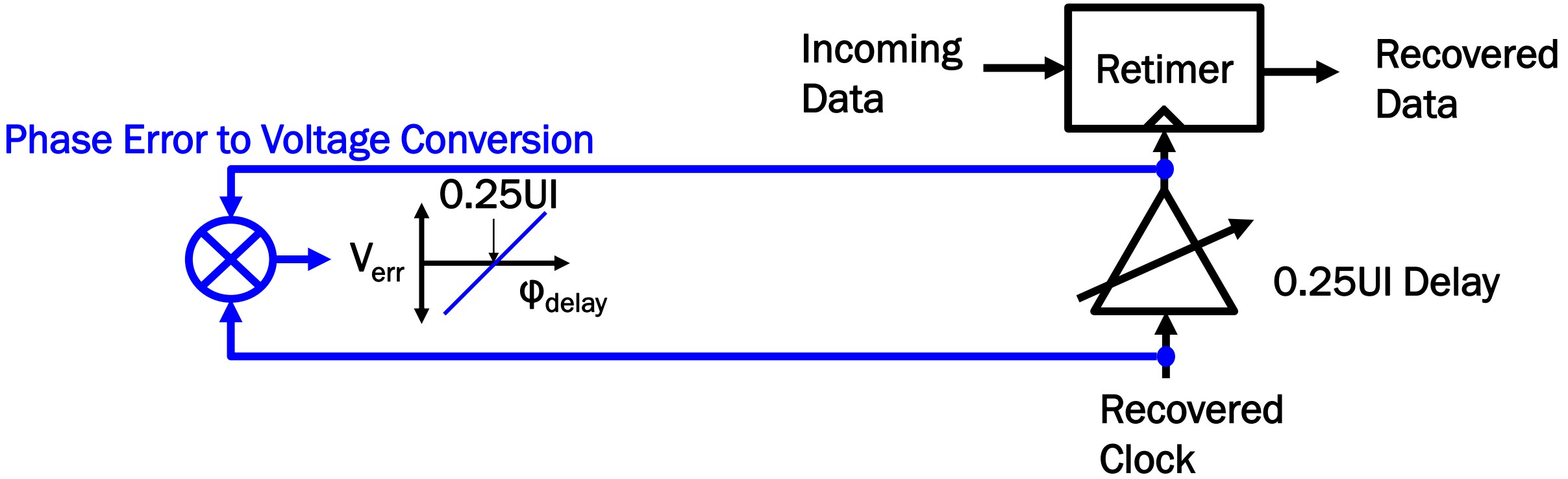

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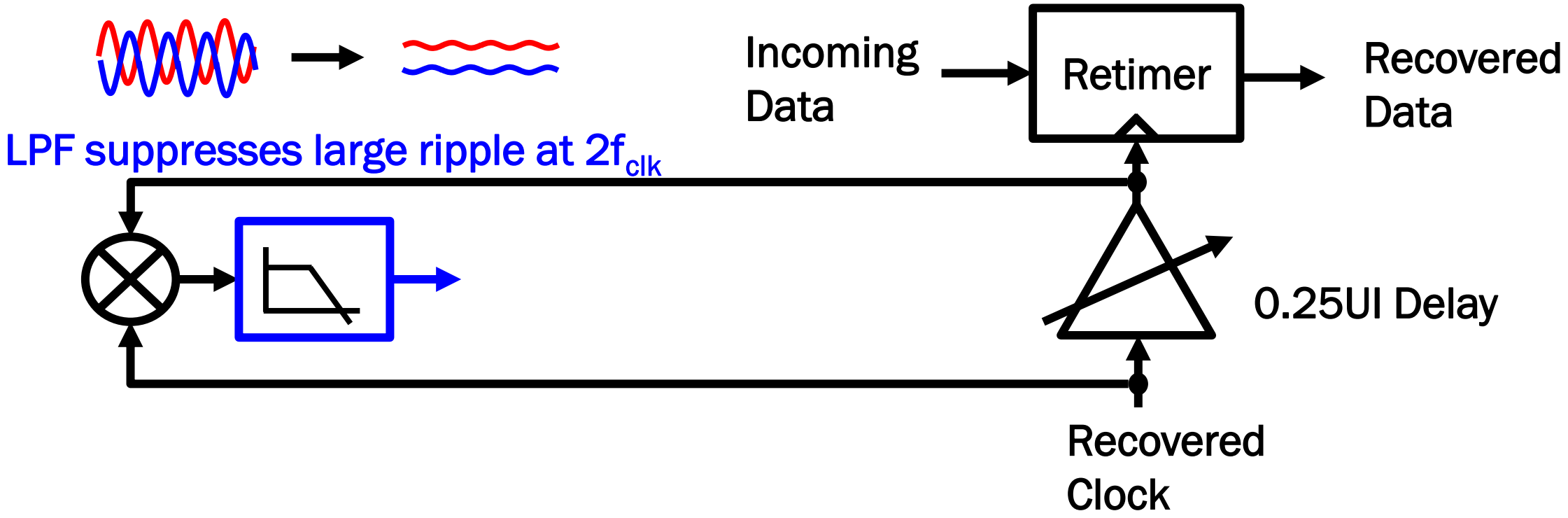

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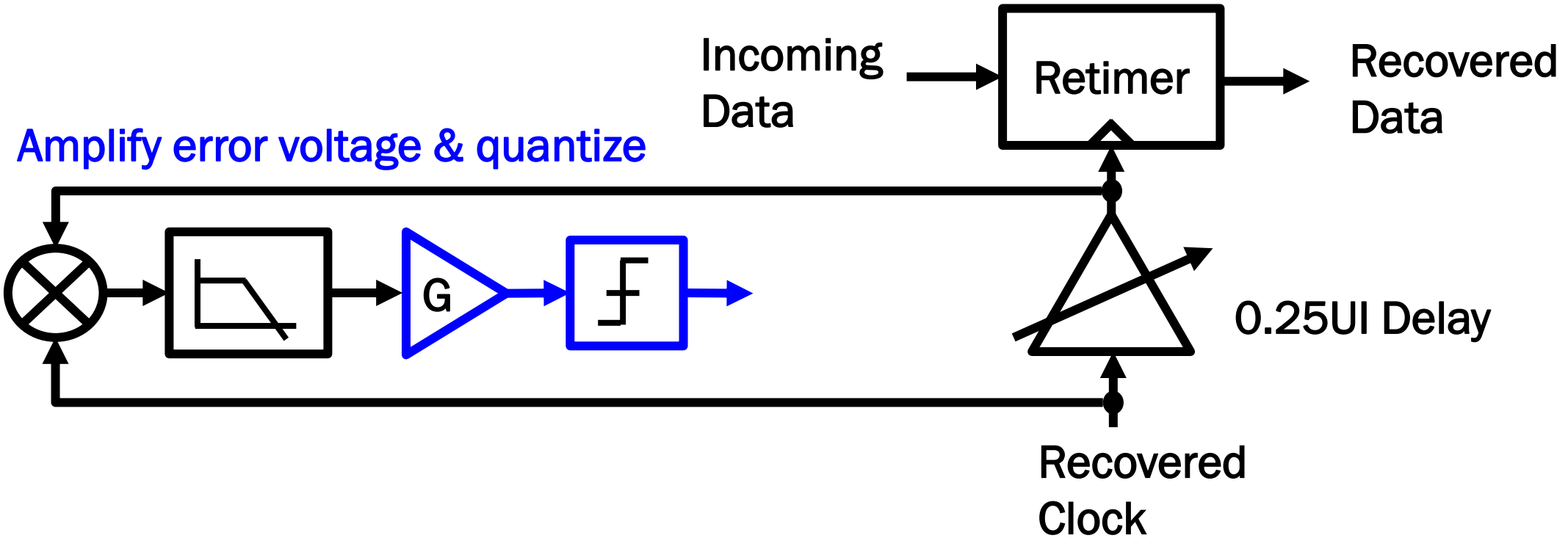

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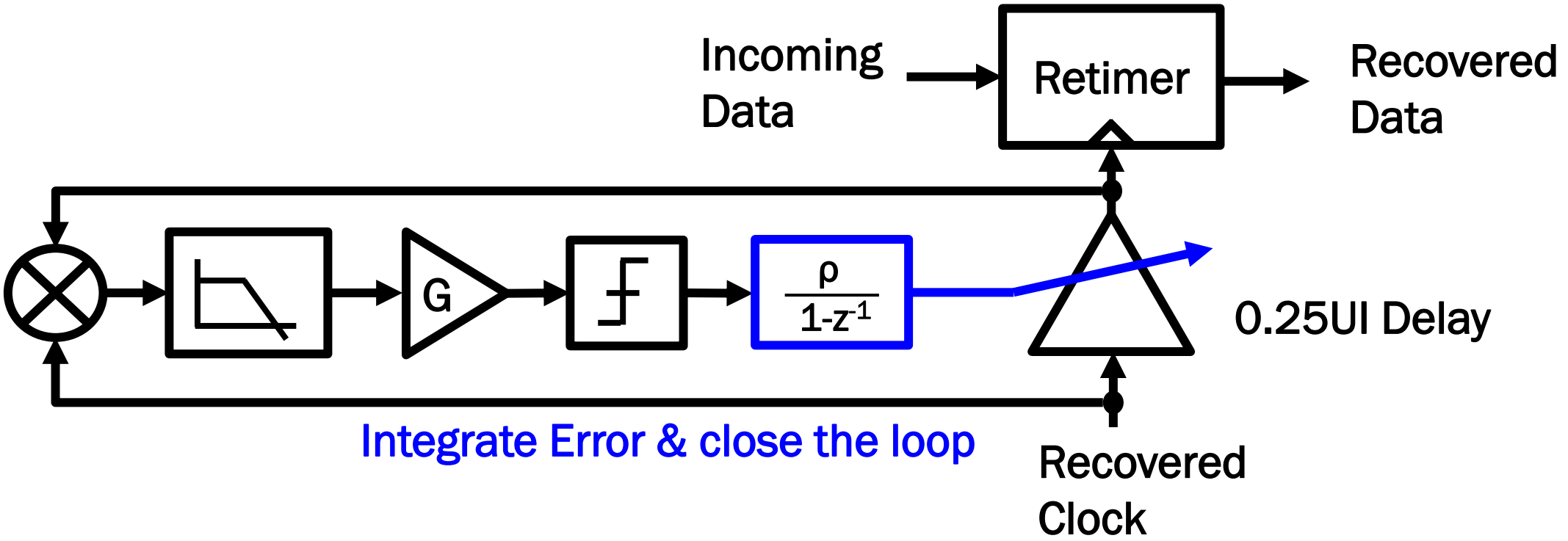
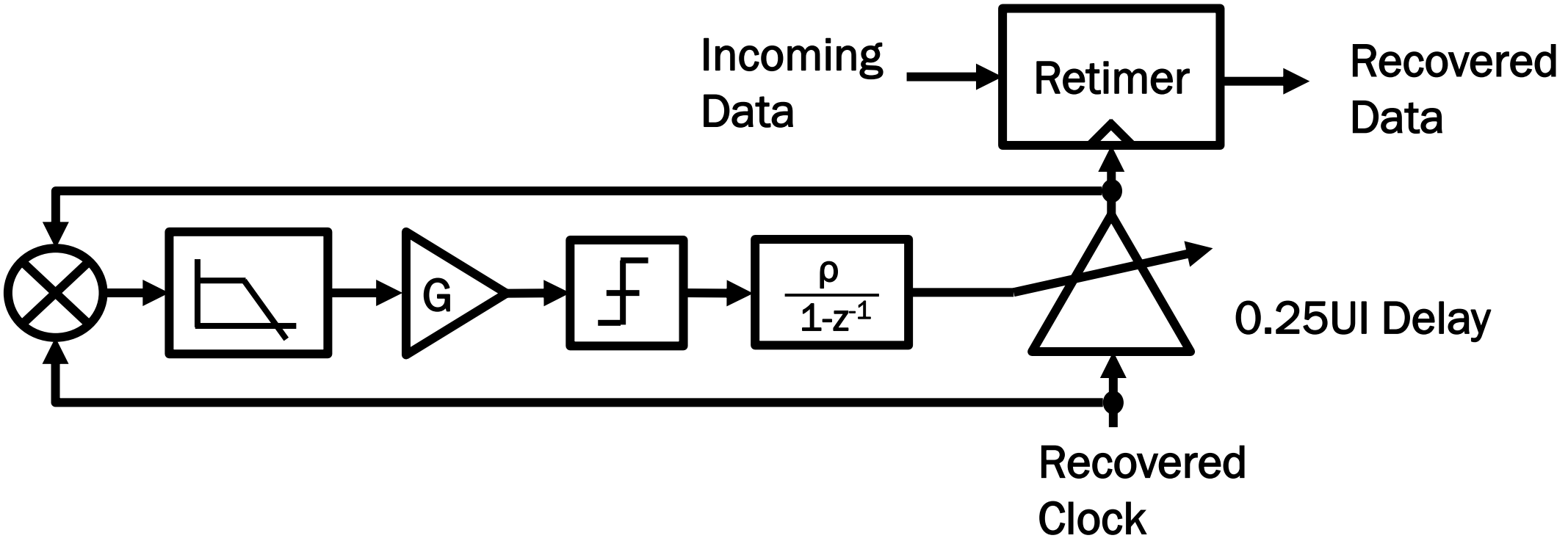


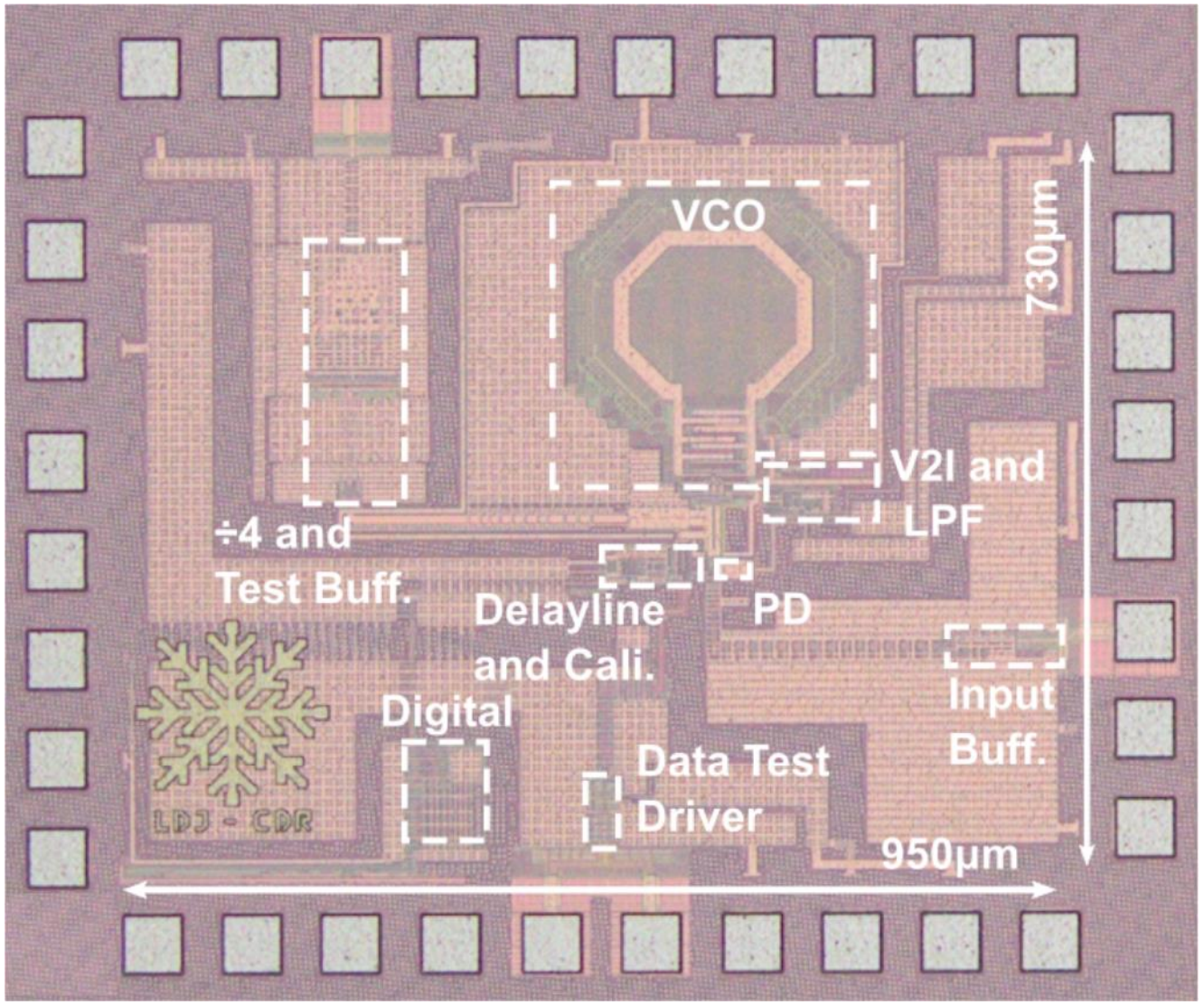
Clock Alignment Result

- 2.5x reduction: $0.1UI_{PP}$ down to $0.04UI_{PP}$
- Theoretical Jitter Tolerance increase of 10%

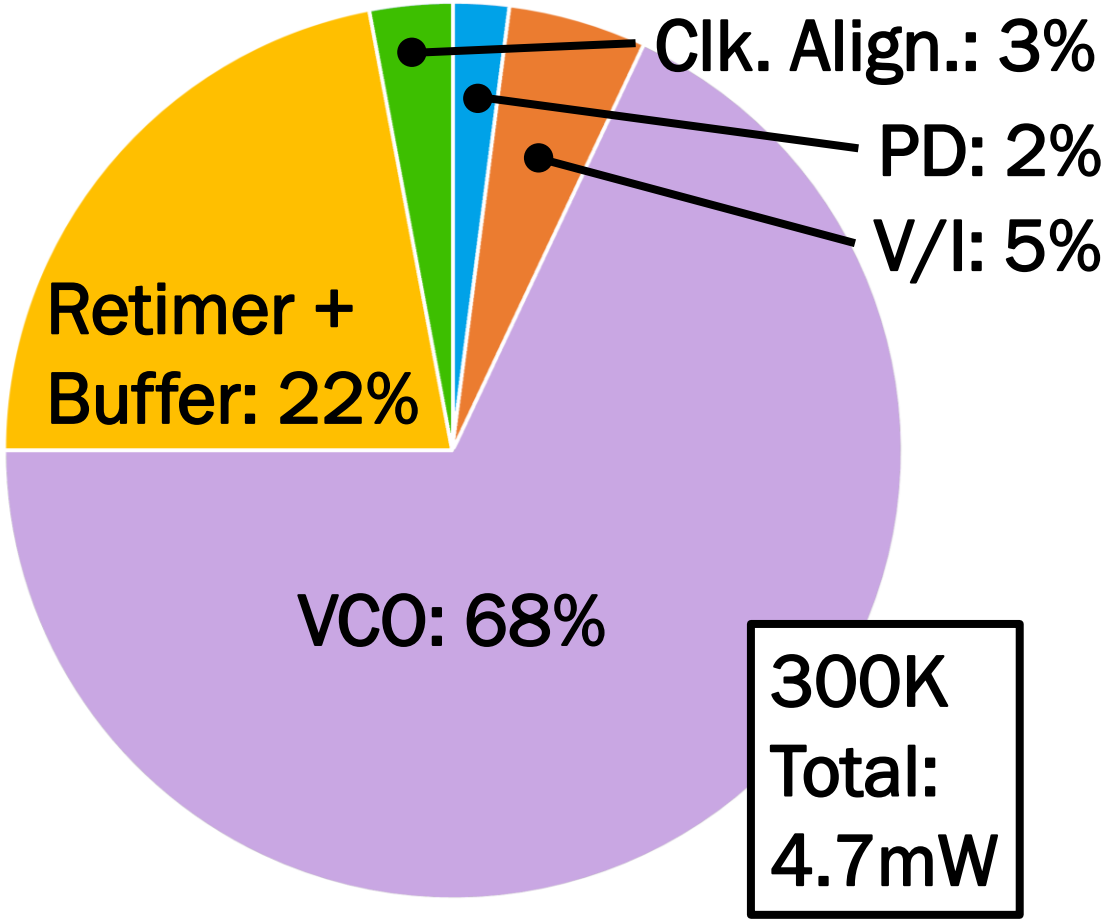


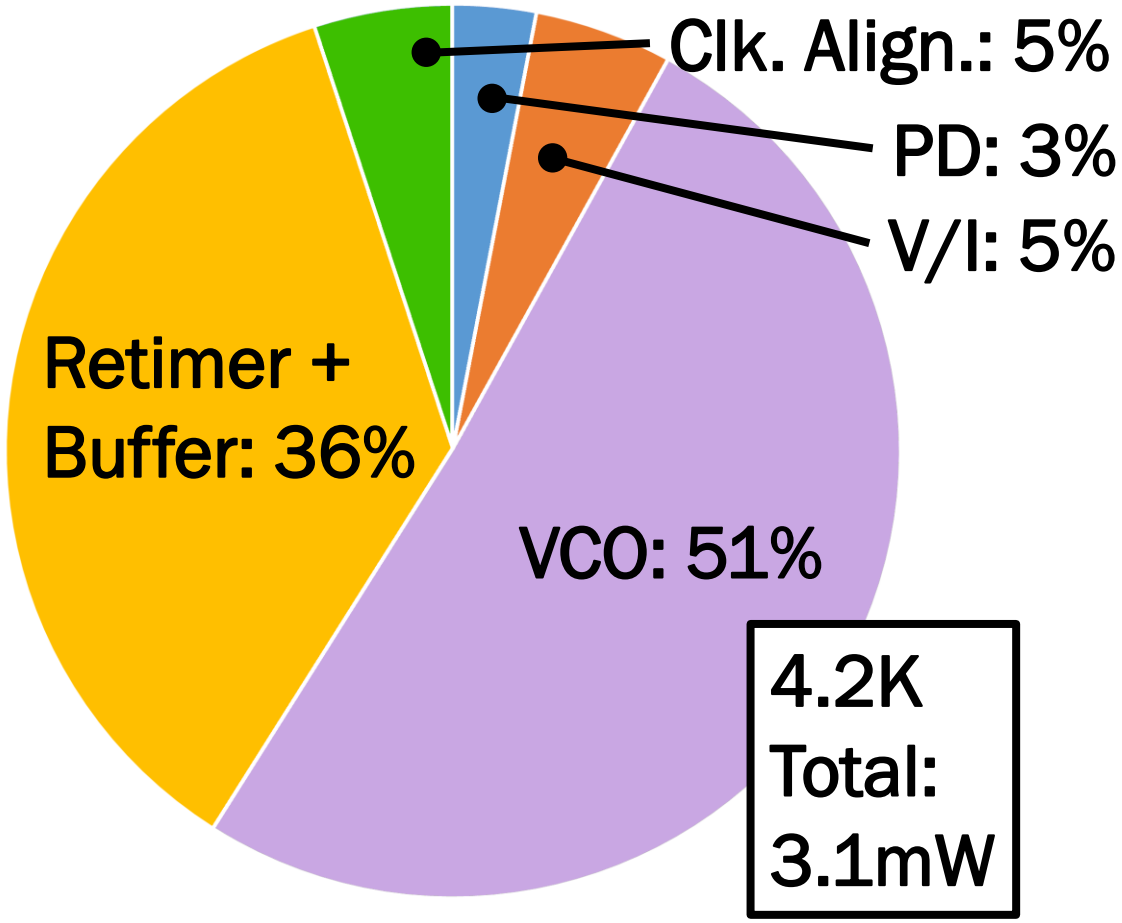
Die Micrograph

- TSMC 40nm process
- 0. 13mm^2 active die area
- Split ground domains to reduce data dependent coupling



Power Breakdown

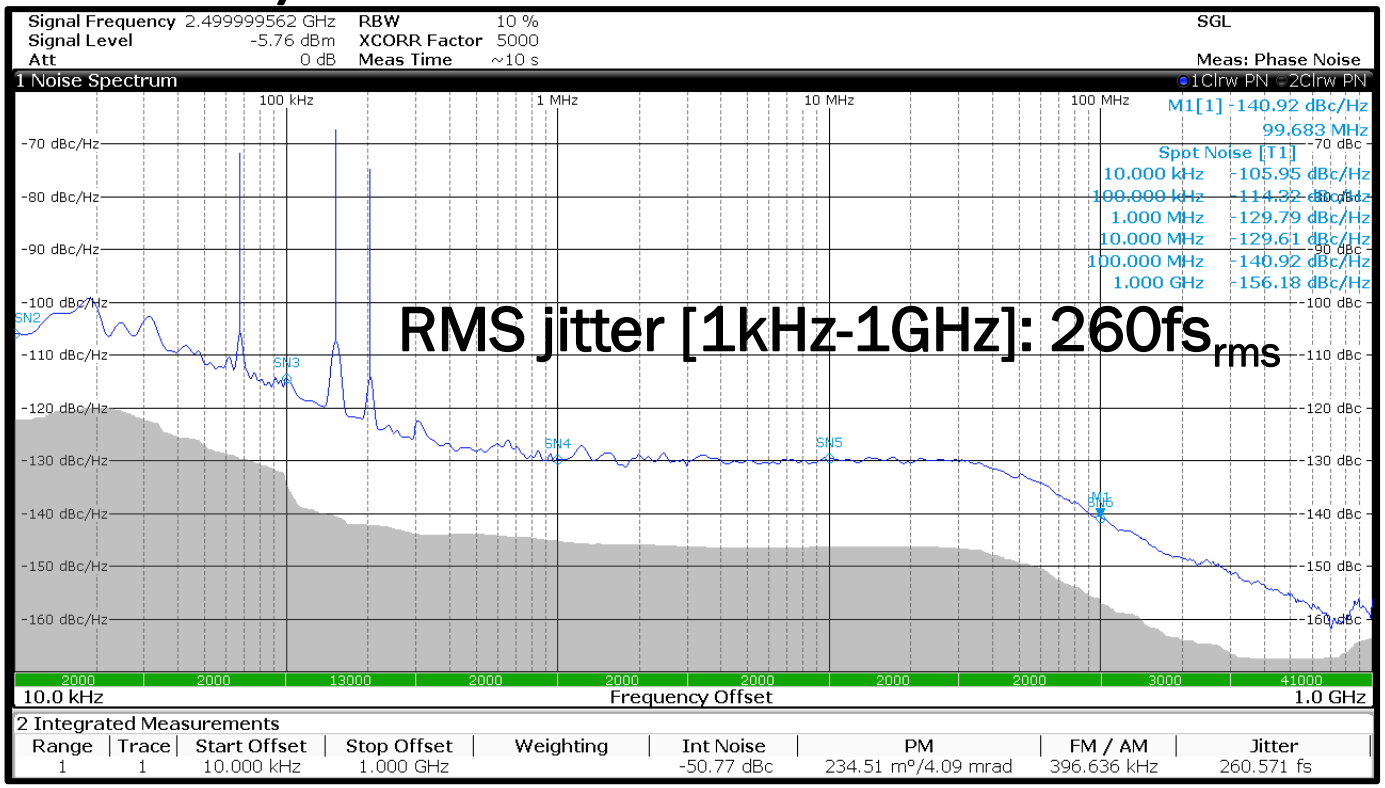




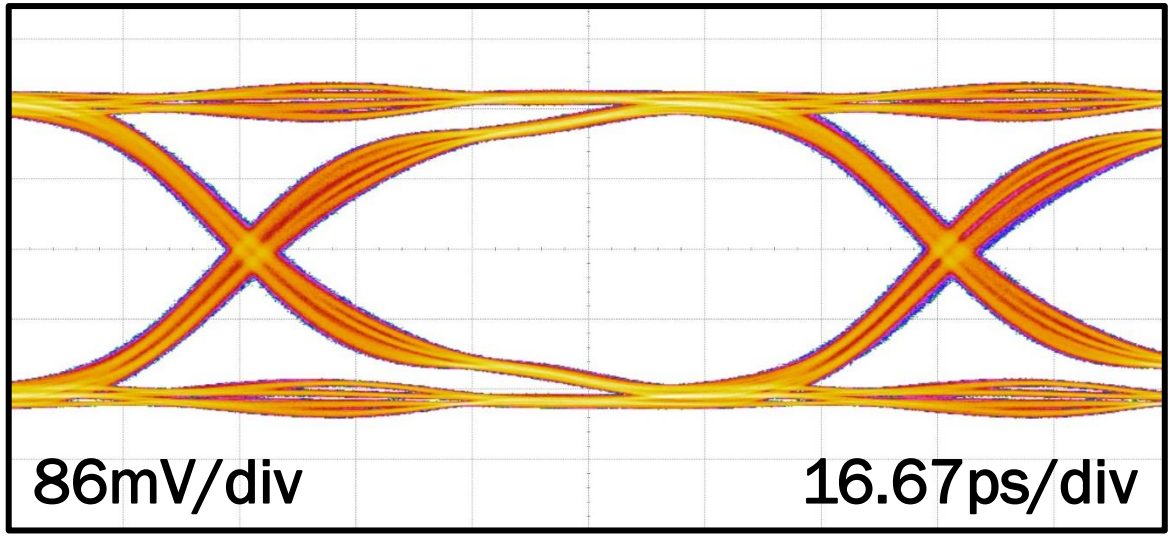
- Power consumption at 4.2K reduces due to increased LC tank Q

Recovered Clock and Data at 300K

10/4 = 2.5GHz Recovered Clock



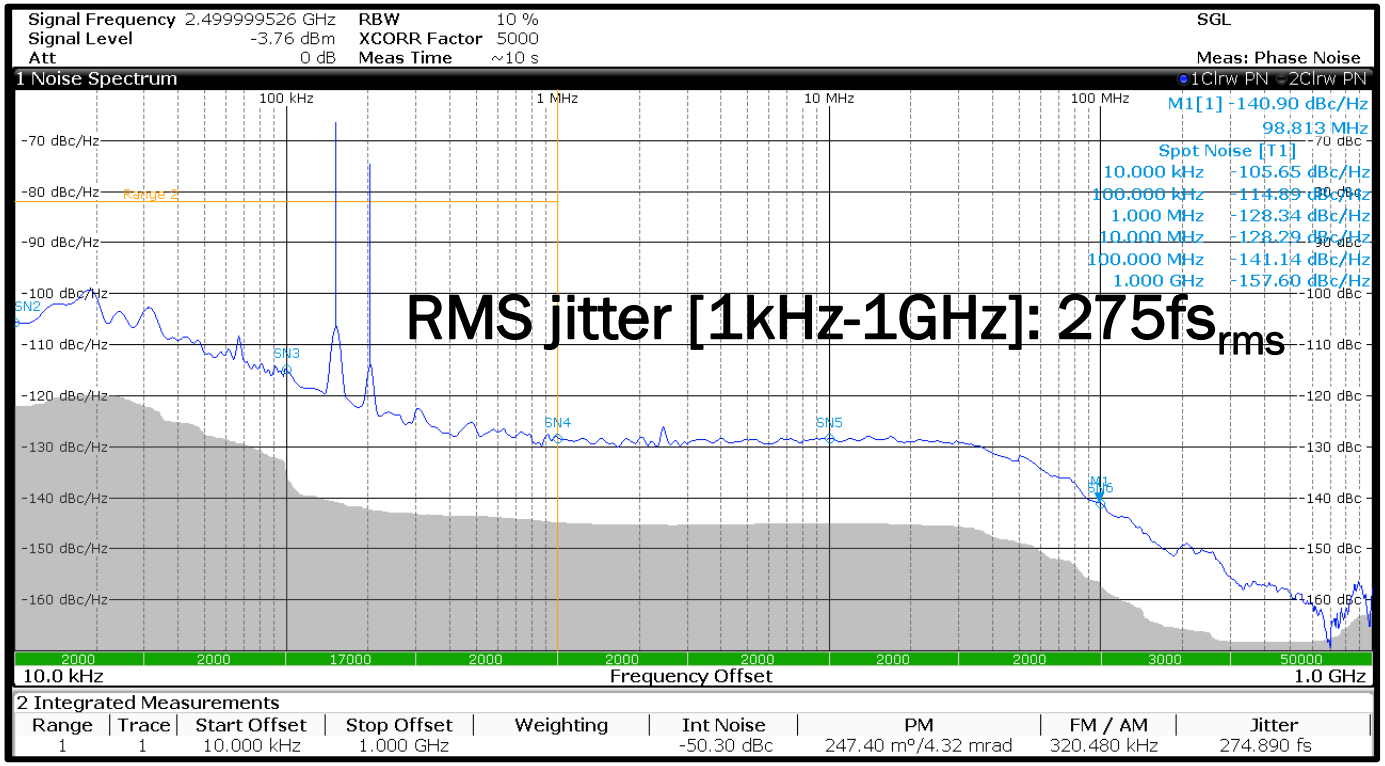
10Gb/s Recovered Data



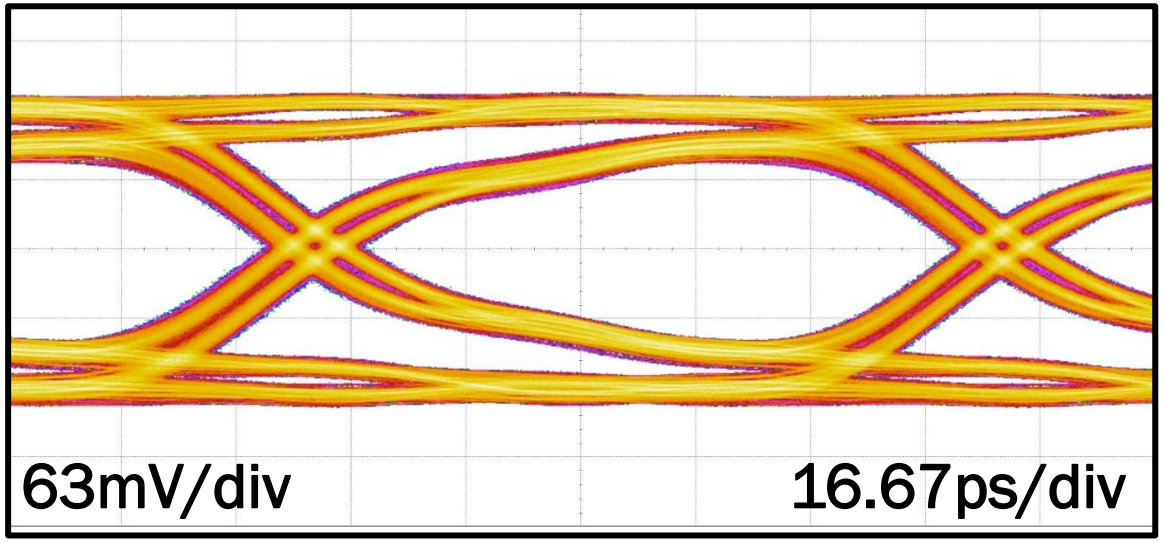
- Integrated recovered clock jitter of 260fs$_{rms}$ for a 10Gb/s PRBS21

Recovered Clock and Data at 4.2K

10/4 = 2.5GHz Recovered Clock

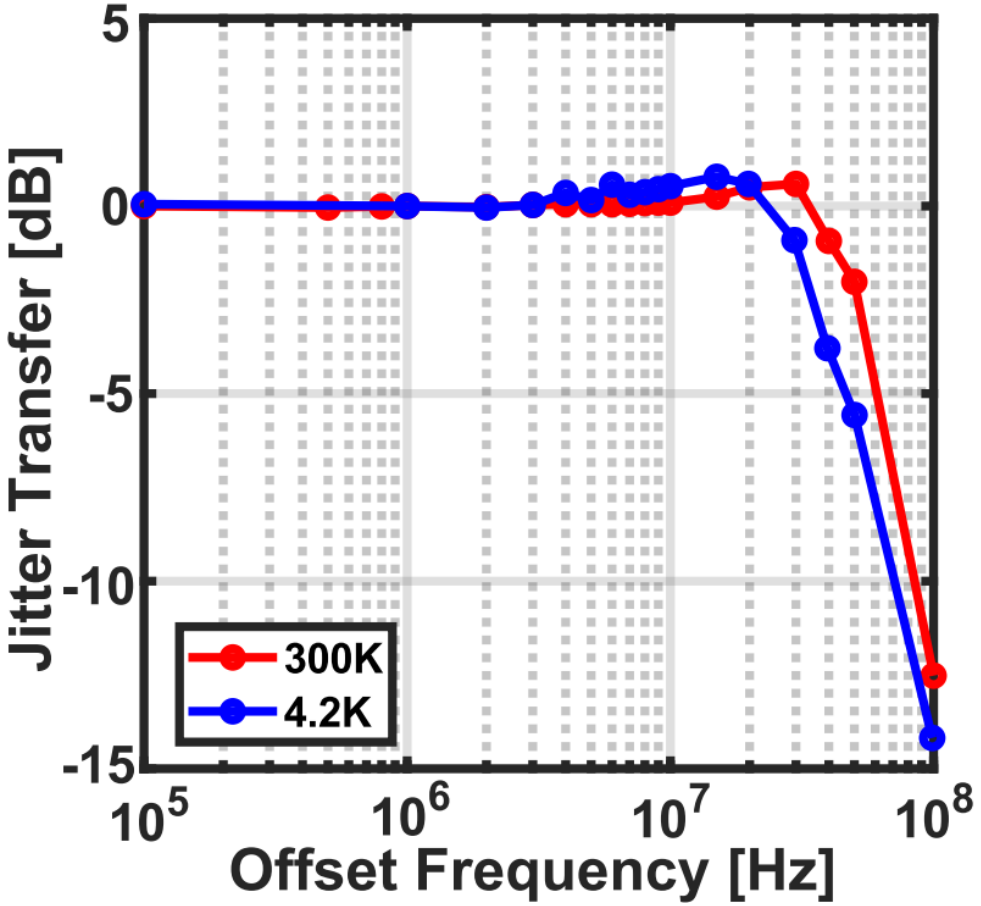


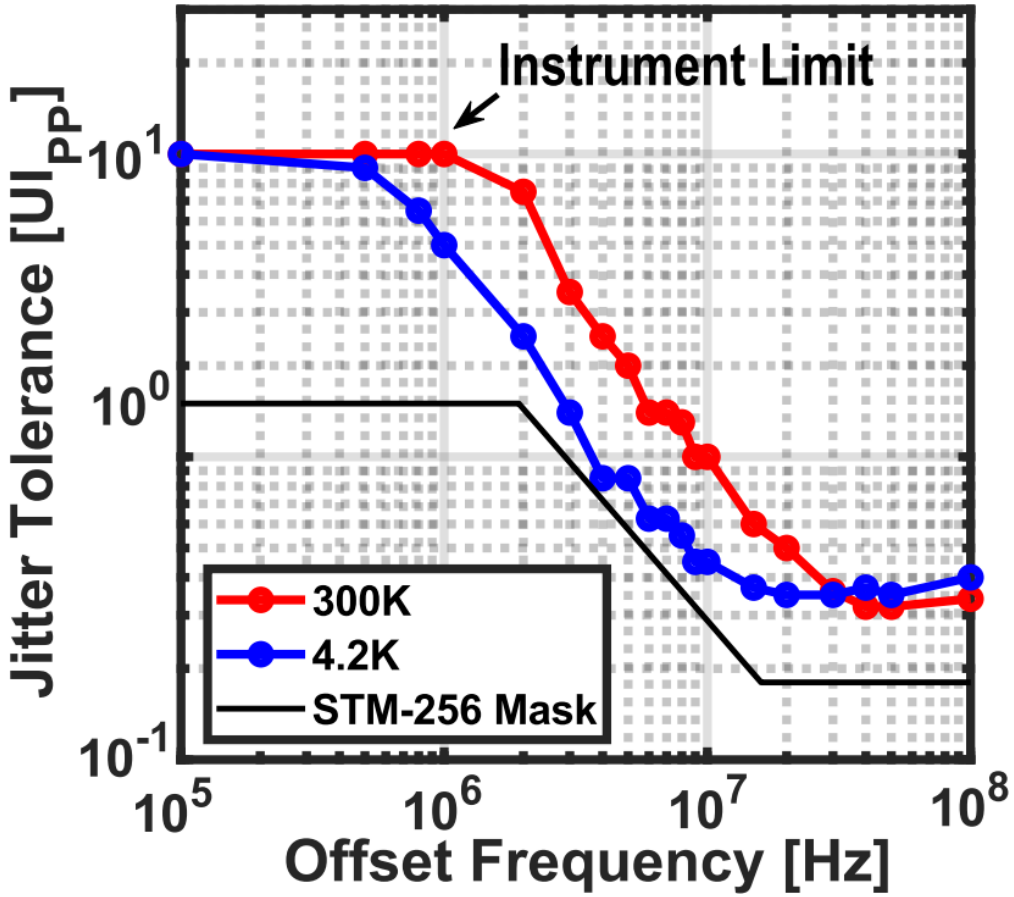
10Gb/s Recovered Data



- Integrated recovered clock jitter of 275fs$_{rms}$ for a 10Gb/s PRBS21

Jitter Transfer & Jitter Tolerance





- High loop bandwidth shows improved jitter tolerance

Comparison Table

	This Work		J. Jung JSSC'13	L. Kong JSSC'19	M. Verbeke JSSC'18	C. Yu JSSC'20
Architecture	**Type-II PLL**		Type-II PLL	Type-I PLL	Type-II AD-PLL	Type-II AD-PLL
Temperature [K]	**300**	**4.2**	300	300	300	300
Jitter Tolerance @ 5MHz [UI_{PP}]	**2**	**0.85#**	0.7	2	1	0.35
Rec. Clock Jitter [ps]	**0.260***	**0.275***	1.5	0.459	1.46	1.15
Power [mW]	**4.7**	**3.1**	5	3	46	21.13
Efficiency [pJ/bit]	**0.47**	**0.31**	0.2	0.15	1.8	2.11
Data Rate [Gb/s]	**10**		25	20	25	10
Area [kum^2]	**130**		39	0.36	50	31
Technology [nm]	**40**		65	45	40	28
Supply [V]	**1.1**		1	1	1.15	1

#measured over 2.5m cable *limited by instrument

Conclusion

- **We introduced two techniques for clock and data recovery systems:**
  - Charge Sampling Phase Detector offering low in-band jitter & data-dependency
  - Phase Alignment to improve jitter tolerance
- **We achieve state-of-the-art performance:**
  - <275fs$_{rms}$ recovered clock jitter at both 300K and 4.2K
  - High power efficiency at both 300K and 4.2K

- **First Cryogenic CDR enabling high-speed communication for Quantum Computing Applications**

Acknowledgement

- The authors thank for funding Intel Corporation and the Netherlands Organization for Scientific Research under the Veni program with number 17303

Backup Slides

Measurement Setup